High-Performance Poly-Si TFTs With Fully Ni-Self-Aligned Silicided S/D and Gate Structure

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***Abstract*—In this letter, fully Ni self-aligned silicided (fully Ni-salicided) source/drain (S/D) and gate polycrystalline silicon thin-film transistors (FSA-TFTs) have been successfully fabricated on a 40-nm-thick channel layer. Experimental results show that the FSA-TFTs give increased ON/OFF current ratio, improved subthreshold characteristics, less threshold voltage rolloff, and larger field-effect mobility compared with conventional TFTs. The FSA-TFTs exhibit small S/D and gate parasitic resistance and effectively suppress the floating-body effect and parasitic bipolar junction transistor action. The characteristics of the FSA-TFTs are suitable for high-performance driving TFTs with good output characteristics and large breakdown voltage.**

***Index Terms*—Floating-body effect, fully salicided, parasitic bipolar junction transistor, polycrystalline silicon thin-film transistors (poly-Si TFTs).**

I. Introduction

RECENTLY, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many applications, particularly as the integrated peripheral driving circuits and addressing elements in active-matrix liquid-crystal displays (AMLCDs) [1], [2]. However, the output characteristics exhibit an anomalous increase of current in the saturation regime, often called the "kink" effect because of an analogy with silicon-on-insulator (SOI) devices [3]–[5]. This phenomenon can be attributed to the floating-body effect [6] and the avalanche multiplication enhanced by grain boundary traps [4]. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [6]. In the floating-body thin-film devices, the improved parasitic BJT effect can be achieved by using deep salicidation and fully silicided source/drain (S/D) structure [7], [8]. Similar to SOI devices, the thin-channel poly-Si TFTs exhibit improved device characteristics such as small leakage current and suppressed floating-body effect compared with the thick-channel poly-Si TFTs [9]. However, parasitic S/D resistances have increasingly become a serious issue in the thin-channel poly-Si TFTs. Several methods such as self-aligned silicide and selective tungsten-clad technology were proposed to reduce parasitic S/D resistance for thin-channel SOI MOSFETs and poly-Si TFTs [8], [10], [11]. In addition, silicided gates have a higher capacitance than poly-Si gates due to the elimination of poly-Si depletion [12].

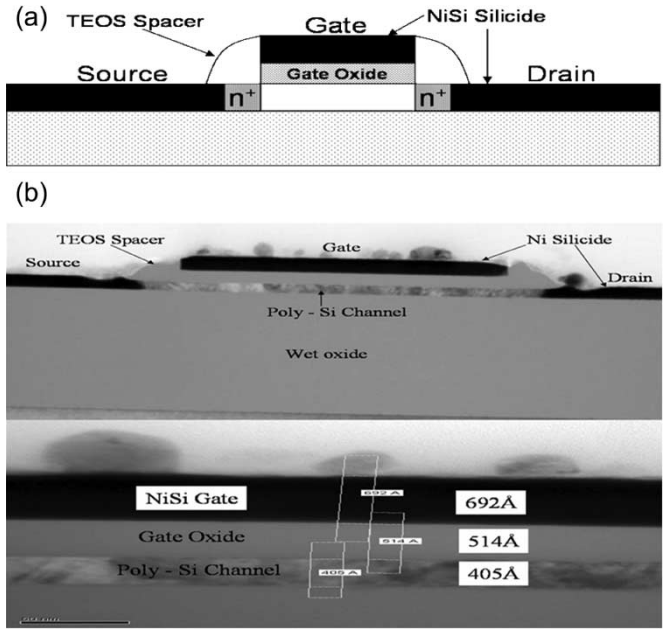

Fig. 1. (a) Schematic device structure and (b) TEM micrograph of the FSA-TFTs with gate length of 0.8 μm and channel thickness of 40 nm.

In this letter, fully Ni self-aligned silicided (fully Ni-salicided) S/D and gate poly-Si thin-film transistors (FSA-TFTs), whose S/D and gate layers are completely silicided with Ni, have been successfully fabricated on a 40-nm-thick channel layer. We found that the measured characteristics of the FSA-TFTs with *in situ* n^+-doped gate or undoped gate significantly suppressed floating-body and parasitic BJT effects.

II. Experiment

The schematic device structure and transmission electron microscopy (TEM) micrograph of the FSA-TFTs is shown in Fig. 1. The FSA-TFTs were fabricated using the following

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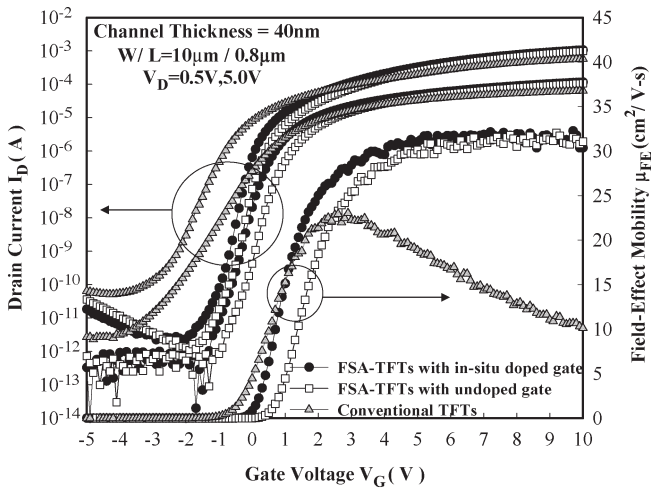

Fig. 2. Measured transfer characteristics and field-effect mobility of the conventional TFTs and the FSA-TFTs with $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$.

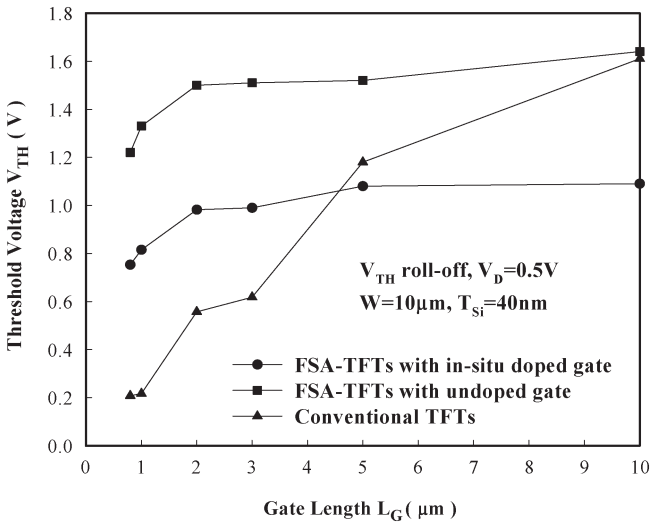

Fig. 3. Extracted threshold voltage V_{TH} of the conventional TFTs and the FSA-TFTs with different gate lengths (defined as $I_{\text{D}} = W/L \times 100$ nA at $V_{\text{DS}} = 0.5$ V).

process steps. First, a 40-nm amorphous-silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. Next, the a-Si layer was crystallized by solid-phase crystallization (SPC) at 600 °C for 24 h. After the active-region patterning, a 50-nm tetraethoxysilane (TEOS) gate oxide layer was deposited by LPCVD. Subsequently, a 50-nm a-Si gate layer and a 150-nm Si_3N_4 layer as the hard mask were deposited by LPCVD. The a-Si gate layers were divided into *in situ* n^+ phosphorus-doped gate or undoped gate. After identifying the gate electrode, a self-aligned implantation was used to form the n^+ S/D with p^+ to dose 5×10^{15} cm^{-2}. Dopants were activated by a furnace at 600 °C for 12 h. A 150-nm TEOS oxide was deposited and etched to form the sidewall spacer. Then, the Si_3N_4 hard-mask layer was selectively etched in a hot phosphoric-acid bath. A Ni film of about 40 nm was deposited by sputtering, and then full Ni salicidation was carried out at 550 °C for 60 s by a one-step rapid thermal annealing (RTA) in the N_2 ambient. The fully Ni-silicided S/D and gate were formed by the full Ni salicidation. After contact and metallization processes, hydrogenation procedures were implemented after sintering at 400 °C for 30 min. Conventional devices with self-aligned n^+ S/D and without Ni salicidation were also fabricated to serve as controls.

III. Results and Discussion

The measured transfer characteristics and field-effect mobility of the conventional TFTs and the FSA-TFTs with $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$ are shown in Fig. 2. The ON-state currents and field-effect mobility in the FSA-TFTs are higher than in the conventional TFTs. The ON-state currents are significantly degraded by the parasitic S/D resistance in short-channel conventional TFTs. The field-effect mobility plotted in Fig. 2 is obtained from the channel conductance. For the conventional TFTs with a short-channel length of 0.8 μm, the field-effect mobility is seriously decreased when gate voltage $V_{\text{G}} > 2.5$ V, but it is not found in short-channel FSA-TFTs. This improvement is due to the fully Ni-salicided S/D and gate structure, which has smaller parasitic S/D resistance, higher capacitance, and superior scalability than the conventional TFTs with poly-Si gates [12]. Furthermore, an anomalous subthreshold swing (SS) and an unstable V_{TH} are observed in conventional TFTs with $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$ at $V_{\text{DS}} = 5.0$ V. Fig. 3 displays the extracted threshold voltage V_{TH} of the conventional TFTs and the FSA-TFTs with different gate lengths (defined as $I_{\text{D}} = W/L \times 100$ nA at $V_{\text{DS}} = 0.5$ V). The rolloff of the threshold voltage V_{TH} is greatly improved in FSA-TFTs. With this fully Ni-salicided structure in FSA-TFTs, the floating-body and parasitic bipolar effects can be suppressed, resulting in a stable V_{TH} and a lower OFF-state leakage current [7], [8], [13], [14]. Therefore, the ON/OFF current ratio $(10^8 - 10^9)$ can be increased by scaling down the channel length in FSA-TFTs. The advantage of FSA-TFTs can be found also on SS. We believe that it may be due to the higher gate capacitance and the fully silicided S/D in the FSA-TFTs.

Fig. 3 also shows the V_{TH} difference (0.5–0.6 V) between *in situ* n^+-doped gate and undoped gate FSA-TFTs. This V_{TH} shift is observed with additional p^+ dopants in the *in situ* n^+-doped gate FSA-TFTs. The silicidation-induced segregation of the impurities from poly-Si to the silicide interface indicated that submonolayer segregation of the dopants causes a change in the apparent Ni/Si work-function shift [12].

Fig. 4 exhibits the measured OFF-state leakage currents of the conventional TFTs and the FSA-TFTs with different channel lengths at $V_{\text{G}} = -5.0$ V. The enhancement of OFF-state leakage currents is observed in short-channel conventional TFTs. These enhanced OFF-state leakage currents are the amplification of gate-induced-drain leakage (GIDL) currents by the parasitic BJT in short-channel devices due to the floating-body effect [15]. Inasmuch as the FSA-TFTs effectively suppress the floating-body effect, the enhancement of GIDL currents is eliminated, and OFF-state leakage currents are almost the same in both long- and short-channel devices. Due to the work-function difference of Ni/Si gates between *in situ* n^+-doped

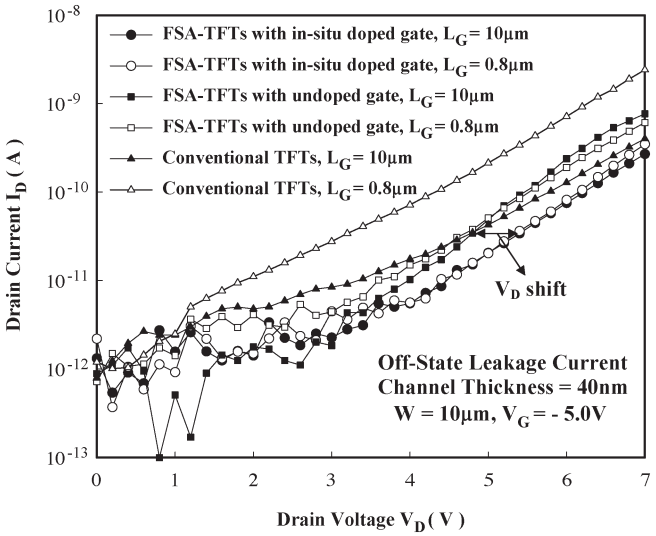

Fig. 4. Measured OFF-state leakage currents of the conventional TFTs and the FSA-TFTs with $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ and $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$ at $V_G = -5.0$ V.

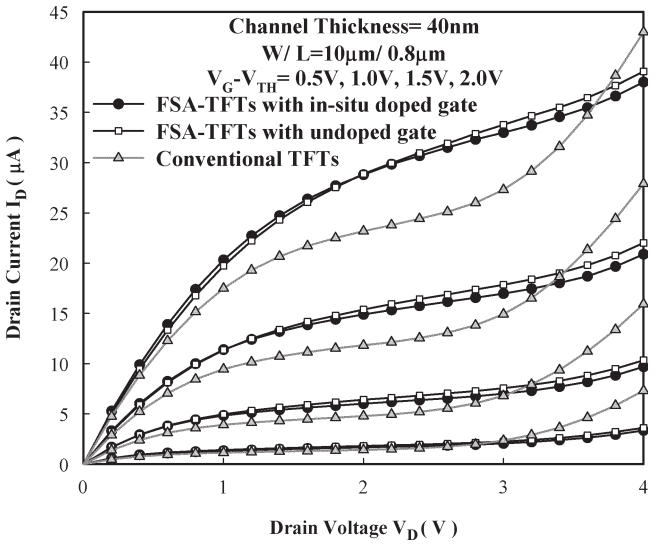

Fig. 5. Measured output characteristics of the conventional TFTs and the FSA-TFTs with $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$.

gate and undoped gate FSA-TFTs, a drain-voltage shift of OFF-state leakage currents is observed [16].

The measured output characteristics of the conventional TFTs and the FSA-TFTs with $W/L = 10\ \mu\text{m}/0.8\ \mu\text{m}$ are shown in Fig. 5. Under high drain voltage, the accumulation of holes in the body causes a profound kink effect and an induced parasitic BJT action, which results in decreased drain breakdown voltage by the floating-body effect in the conventional TFTs [17]–[20]. Salicidation is a well-known method to suppress the floating-body effect, because the silicide layer near the S/D junction works as a sink and an effective lifetime killer for holes [7], [8]. The reduced kink effect and the increased drain breakdown voltage of FSA-TFTs strongly support the idea that floating-body and parasitic BJT effects are significantly suppressed by the fully silicided S/D structure.

IV. Conclusion

We have developed the fully Ni-salicided S/D and gate poly-Si TFTs to suppress the floating-body effect. The enhancement of GIDL currents that occurred in the conventional TFTs is eliminated by the FSA-TFTs. The FSA-TFTs show reduced kink effect, increased breakdown voltage, stable V_{TH}, improved SS, and increased ON/OFF current ratio. The FSA-TFTs are proven to be a very promising structure with low S/D parasitic resistance and high gate capacitance capability fabricated on a thin 40-nm-thick channel layer.

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