

NANO EXPRESS

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A Unique Approach to Generate Self-Aligned SiO₂/Ge/SiO₂/SiGe Gate-Stacking Heterostructures in a Single Fabrication Step

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Abstract

We report a first-of-its-kind, unique approach for generating a self-aligned, gate-stacking heterostructure of Ge quantum dot (QD)/SiO₂/SiGe shell on Si in a single fabrication step. The 4-nm-thick SiO₂ layer between the Ge QD and SiGe shell fabricated during the single-step process is the result of an exquisitely controlled dynamic balance between the fluxes of oxygen and silicon interstitials. The high-quality interface properties of our “designer” heterostructure are evidenced by the low interface trap density of as low as $2\text{--}4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and superior transfer characteristics measured for Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs). Thanks to the very thin interfacial SiO₂ layer, carrier storage within the Ge QDs with good memory endurance was established under relatively low-voltage programming/erasing conditions. We hope that our unique self-aligned, gate-stacking heterostructure provides an effective approach for the production of next-generation, high-performance Ge gate/SiO₂/SiGe channel MOSFETs.

Keywords: Gate-stacking heterostructure; SiGe channel; Self-aligned; Ge quantum dot

Background

Rapid expansion of functional electronic applications for mobile devices and for embedded integrated circuit systems has driven a strong and immediate demand for high-speed, low-power transistors and nonvolatile memories. There is, of course, the relentless reduction of feature sizes for achieving desired device performance. In addition, alternative channel materials with higher carrier mobilities are being sought after as a possible solution for realizing next-generation complementary metal-oxide-semiconductor (CMOS) devices [1–9]. Among the possible choices for high-mobility channel materials, Ge has emerged as a leading contender to replace its well-established counterpart, Si, for post-CMOS transistors. This is thanks to Ge’s superior carrier transport efficiency and enhanced charge confinement capabilities [8–16]. Despite these advantages, the production of Ge MOS field-effect transistors (MOSFETs) has been hampered, in particular, in situations where high-temperature thermal oxidation processes are involved. The key for

implementing Ge MOS structures lies in the growth of high-quality Ge on Si heterostructures. Sufficiently low defect densities [8, 10] coupled with the formation of gate dielectric layers over the Ge with satisfactory interfacial and electrical properties are required [13–16]. Both of the above requirements are extremely challenging. One is because of the large lattice mismatch of 4.2 % that exists between Ge and Si, and the second is the lack of a robust native oxide for Ge. Unlike the relatively stable SiO₂, Ge oxide (GeO_x) is water soluble and thermally unstable. Thus, high densities of interface states (D_{it}) and rough interfaces between the oxide and the Ge are produced, both of which are detrimental for the realization of high-speed Ge MOSFETs.

Recently, we have demonstrated a unique CMOS compatible, self-assembled approach to deliberately grow spherical Ge quantum dots (QDs) of desired sizes. We also place these QDs at desired spatial locations with controlled depths of penetration into Si. This was achieved using the exquisite control available through lithographic nanopatterning and selective oxidation of the nanopatterned SiGe layers [17–20]. Remarkably, such self-aligned heterostructures of SiO₂/Ge QD/SiO₂/SiGe shell over the Si substrate can be created in a single fabrication step. In this work, we constructed Ge QD

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MOS capacitors and Ge floating-dot MOSFETs based on this “designer heterostructure” as well as assessed the interfacial properties of Ge QD/SiO₂/SiGe channel from both structural and electrical perspectives. Our devices exhibit reasonably low interface trap densities, good switching behavior, and excellent charge storage characteristics.

Methods

The fabrication starts with tri-layer, sequential low-pressure chemical vapor deposition of 25-nm-thick Si₃N₄, 70-nm-thick poly-Si_{0.85}Ge_{0.15}, and finally, a capping layer of a 5-nm-thick SiO₂ over a Si substrate. The topmost, capping SiO₂ and the poly-Si_{0.85}Ge_{0.15} layers are lithographically defined to create 240-nm diameter, nanocylindrical pillars. The SiGe pillar density is approximately $1 \times 10^9 \text{ cm}^{-2}$ over the buffer Si₃N₄ layers. Next, the nanopatterned structure is subjected to thermal oxidation at 900 °C within an H₂O ambient producing 90-nm diameter, spherical Ge QDs that migrate into the buffer Si₃N₄ layer [17, 18], as shown in Fig. 1a. Next, an Al top gate (with an area of 75 μm × 75 μm) and substrate electrodes are fabricated over the Ge QD array and the backside of the Si substrate, respectively. A final, forming gas anneal at 400 °C completes the

fabrication of the Al-SiO₂/Ge QD/SiO₂-SiGe MOS capacitors. Additional processes for defining the Al gate and As-doped source/drain (S/D) electrodes are conducted for the fabrication of floating gate MOSFETs. The channel length (L_g) and width (W) are 3 and 50 μm, respectively. High-resolution, cross-sectional transmission electron microscopy (CTEM) and energy dispersive X-ray (EDX) spectroscopy were used to examine the crystallinity, interfacial morphology, and chemical purity of the Ge QD/SiO₂/Si heterostructures. Electrical and interfacial properties of SiO₂/Ge QD/SiO₂/SiGe MOS devices were measured using frequency-dependent capacitance-voltage ($C-V$) and current-voltage ($I-V$) characterization over a range of temperatures. Pulse $I-V$ measurements were also conducted to characterize the floating gate memory devices.

Results and Discussion

A core building block for floating gate MOS devices is a heterostructure stack consisting of metal-control oxide-floating gate-tunneling oxide-semiconductor, which is usually achieved via multiple-layer, sequential deposition and patterning. Instead, we have succeeded in generating complex heterostructure stacks of 70-nm-thick SiO₂/90-

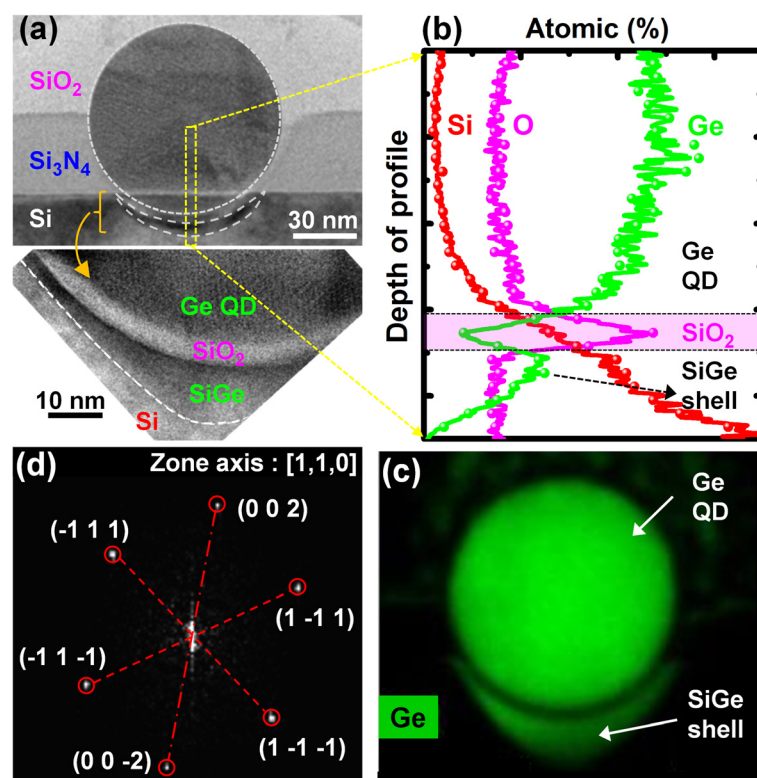


Fig. 1 **a** Cross-sectional transmission electron microscopy (CTEM) images as well as EDX elemental **b** line-scan spectra and **c** X-ray mapping micrographs of a SiO₂/Ge QD/SiO₂/SiGe shell heterostructure over the Si substrate. **d** Selected area diffraction patterns were generated by applying a fast Fourier transform to the local high-resolution CTEM images of the SiGe shell. The interplanar spacing is approximately 3.16 nm, corresponding to Si_{0.28}Ge_{0.72} {111} planes

nm Ge QD/4-nm-thick SiO₂ over a 20-nm-thick Si_{0.28}Ge_{0.72} channel in a single, self-organized nanofabrication step. During the high-temperature oxidation of poly-SiGe nanopillars, the Si content in the nanopillar is preferentially oxidized, squeezing the remaining Ge radially inwards to the centers of the oxidized pillars. Further thermal oxidation resulted in the consolidation of the Ge nanocrystallites in each pillar via Ostwald ripening into single spherical Ge QDs. These QDs also simultaneously migrate through the underlying buffer Si₃N₄ layers and achieve contact with the Si substrate, as shown in Fig. 1a. CTEM-EDX line scanning (Fig. 1b) and mapping (Fig. 1c) examinations confirm the high chemical purity of each Ge QD. Intriguingly, a “cup”-shaped morphology is observed for the Ge QD/Si substrate interface (Fig. 1a). The cup is formed by an approximately 4-nm-thick amorphous interfacial oxide layer, conformal with the QD. Below the interfacial oxide layer, an approximately 20-nm-thick Si_{1-x}Ge_x shell is generated within the Si substrate. A substantial amount ($x \approx 0.72$) of Ge as estimated from the Raman signal at 414 cm⁻¹ for the SiGe shells formed from the 90-nm Ge QDs [21, 22]. Clear lattice fringes are observed in the high-resolution CTEM micrographs (Fig. 1a). Corresponding selected area diffraction patterns (Fig. 1d), obtained by applying a fast Fourier transform locally to the heterostructure images, confirm the good crystallinity of our self-assembled SiGe shells. The {111} interplanar spacing of ~ 3.16 nm, suggests that the Si_{0.28}Ge_{0.72} shell is under a compressive strain of 2.36 %, thus having great promise for possible high-mobility channel p-MOS applications.

As regards the 4-nm interfacial oxide layer separating the Ge QD and the Si substrate, detailed CTEM-EDX examinations reveal that this amorphous interfacial layer is pure SiO₂ instead of GeO_x. A sharp dip in the Ge X-ray signal coupled with a simultaneous increase in the Si X-ray intensity is observed from the EDX line scans in Fig. 1b. We have previously proposed [18, 20] that this thin, interfacial SiO₂ layer between the Ge QD and the SiGe shell is formed by the thermal oxidation of Si interstitials. These interstitials are released from the dissociation of the Si substrate. The SiO₂ thickness is consequently determined by a dynamic equilibrium that exists between the concentration of Si interstitials and the external oxygen flux. From a chemical thermodynamics perspective, oxygen clearly prefers to react with the Si interstitials rather than with the Ge because of the large difference in enthalpies of formation for SiO₂ (-910.9 kJ/mole) and for GeO₂ (-477 kJ/mole) [23]. The clear and abrupt amorphous interfacial SiO₂ layer between the QD and the SiGe shell suggests an absence of structural defects near either interface, i.e., the Ge QD/SiO₂ interface as well as the SiO₂ layer/SiGe shell

interface. Therefore, this thermally grown interfacial SiO₂ layer over the SiGe shell is believed to possess the advantages of robustness, thermal stability, and superior electrical properties. Essentially similar to SiO₂ thermally grown over Si substrates, our Ge QD/SiO₂/SiGe heterostructure is amenable for the production of high-performance SiO₂/SiGe MOS devices.

Fig. 2a shows the cross-sectional schematic of heterostructured SiO₂/Ge QD/SiO₂/SiGe n-MOSFET and MOS capacitor. Notably, the channel of studied heterostructured MOS devices consists of SiGe shell channels below the Ge QDs in series with Si channels with no Ge QDs overhead. The gate dielectric layers of SiO₂ over the SiGe channel and SiO₂/Si₃N₄ over the Si channel have an equivalent gate oxide thickness (EOT) of approximately 15 and 41 nm, respectively, leading to the SiGe shell being the prime channel that is turned on prior to the parasitic Si channel due to a smaller threshold voltage. Meanwhile, it is a known fact that the interfacial property of Si₃N₄/Si channel is not as good as that of SiO₂/Si. Hence, we believe that our heterostructured SiO₂/Ge QD/SiO₂/SiGe MOS devices provide a reasonable platform for the assessment of the interfacial properties of Ge QD/SiO₂/SiGe channel though extracted interfacial trap density from high-/low-frequency *C-V* characteristics of MOS capacitors and from the subthreshold slope (*S.S.*) of transfer (*I_d-V_g*) curves for MOSFETs.

I-V characteristics were measured for the Al-SiO₂/Ge QD/SiO₂-SiGe MOS capacitor we fabricated. The typical features of direct tunneling, Fowler-Nordheim tunneling, and hard breakdown, as indicated by regions I, II, and III, respectively, are shown in the inset of Fig. 2b. We also measured a low leakage current density of about 10⁻⁹ A/cm² and a high breakdown electric field (*E* field) of 8.3 MV/cm. These results verify the electrical robustness of the SiO₂/Ge QD/SiO₂/SiGe shell heterostructure. Good gate oxide integrity is further evidenced by its frequency-dependent *C-V* characteristics. Fig. 2b clearly shows that the gate bias controls the surface charge and minority carriers very well at 500–1 MHz with almost no frequency-induced dispersion observable for both n- and p-MOS capacitors. Values for mid-gap *D_{it}* as low as 2–4 × 10¹¹ cm⁻² eV⁻¹ were extracted from the extensive, variable temperature high-/low-frequency *C-V* characteristics of more than 20 MOS diodes (Fig. 2c). As mentioned previously, the interfacial property of Si₃N₄/Si channel is no better than that of SiO₂/Si, and thereby, the extracted *D_{it}* values of 2–4 × 10¹¹ cm⁻² eV⁻¹ may be overestimated for the solely Ge QD/SiO₂/SiGe channel system. Notably, our results are a sharp contrast to the undesirable frequency- and gate bias-dependent capacitance humps/peaks in the weak inversion region usually observed for conventional GeO₂/Ge n-MOS capacitors due

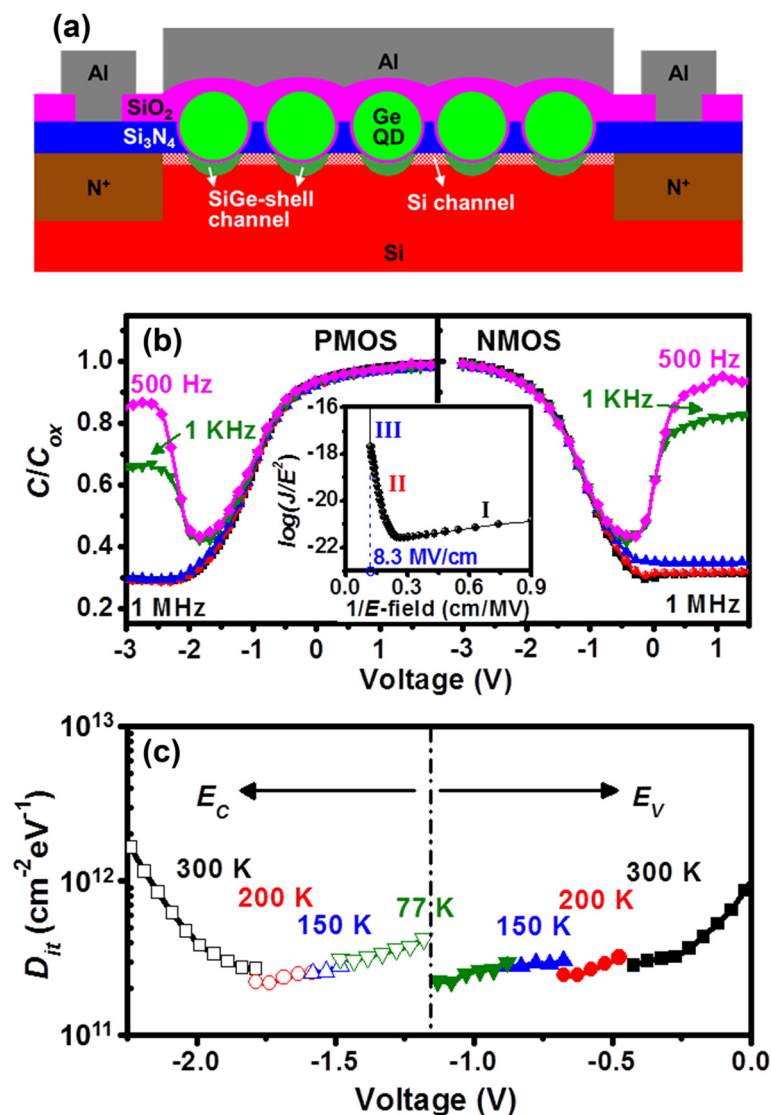


Fig. 2 **a** Cross-sectional schematic of the heterostructured SiO₂/Ge QD/SiO₂/SiGe n-MOSFET. The gate-stacking region also represents the structural core of the heterostructured MOS capacitor. **b** Frequency-dependent C-V characteristics of the heterostructured MOS capacitors, where C/C_{ox} represents the normalized capacitance. The inset in **b** shows the corresponding I - V behavior. **c** D_{it} values extracted from high-/low-frequency C-V curves in the temperature range of 300–77 K

to the high-interface trap density in the upper half of the bandgap of Ge [11, 15]. Also, our experimental electrical data obviously deviates from the frequency-induced dispersion and stretch out in C - V characteristics as well as E field-dependent Frenkel-Pool conduction in I - V characteristics that are commonly observed for Si₃N₄/Si MOS capacitors. Both experimental C - V and I - V data are further evidence to support the superior, device-quality interface properties and excellent gate oxide integrity of the SiO₂/Ge QD/SiO₂/SiGe heterostructure that is applicable for device applications.

I_d - V_g of the heterostructured Ge QD/SiO₂/SiGe channel nMOSFETs show very low off-state leakage of $I_{off} \cong$

10^{-13} A/ μ m. A superior on-off current ratio of $I_{on}/I_{off} > 10^6$ and good switching behavior for S.S. of 195 mV/dec at $T = 300$ K were also measured (Fig. 3a). This low value of I_{off} leakage as well as the high I_{on}/I_{off} ratio is attributable to the high crystalline quality of the SiGe channel and good interface properties for the thin SiO₂ and SiGe channel. The I_d - V_g characteristics were measured at $T = 77$ –300 K to estimate S.S. from its dependence on temperature. Decreasing the operating temperature from 300 to 77 K results in significant, two-fold enhancement of the on-state drive current (Fig. 3b). The S.S. improves from 195 to 105 mV/dec as a result of the suppressed phonon scattering. D_{it} estimated from

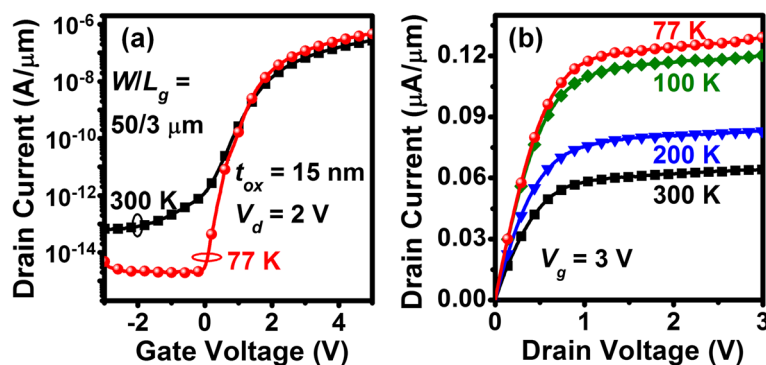


Fig. 3 **a** Transfer and **b** output characteristics of the heterostructured $\text{SiO}_2/\text{Ge QD}/\text{SiO}_2/\text{SiGe}$ n-MOSFETs measured at $T = 77\text{--}300$ K. High $I_{\text{on}}/I_{\text{off}}$ ratio $>10^6$ and low off-state leakage of $I_{\text{off}} < 10^{-13}$ A/ μm are achieved

the $S.S.$ value for n-MOSFETs is approximately $4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $T = 300$ K, which is in good agreement with estimates derived from the high-/low-frequency C - V characteristics. As mentioned previously, the conducting channel connecting source and drain indeed consists of the prime SiGe shell in series with the second Si inversion layer that would be sequentially turned on due to the difference in the EOT of gate dielectric layers. It would require a greater gate voltage swing (i.e., larger $S.S.$) to completely turn on the entire composited channel than the solely SiGe shell. We envisage that significant improvements in $S.S.$ and switching performance are achievable through reducing the parasitic Si channel via shrinking the channel length and increasing the pillar (QD) density within the channel.

Good transfer characteristics such as $S.S.$ of $\sim 100\text{--}150$ mV/dec and low D_{it} of $\sim 1\text{--}5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ have been previously reported for the Ge/GeO₂ or Ge/GeO₂/high- k MOSFETs [9, 11, 14, 15]. However, these characteristics were obtained at the expense of special interfacial treatment prior to and following gate oxidation, such as high-pressure oxidation, two-step oxidation, H₂O oxidant pre-pulsing, and post-oxidation annealing. Additionally, all the processing temperatures were constrained to be below 500 °C in order to prevent GeO desorption that severely deteriorates the Ge/dielectric interface and the thermal stability of the Ge MOSFETs [9, 14, 15]. In order to meet the temperature constraint requirement for the production of Ge/GeO₂ or Ge/GeO₂/high- k MOSFETs, a “gate-last” process is employed. This is because the temperature to activate n-type dopants for source/drain is generally, significantly higher than 500 °C. Finally, in spite of achieving good $S.S.$ and low D_{it} values, the low $I_{\text{on}}/I_{\text{off}}$ ($\sim 10^4$) of Ge/GeO₂/high- k MOSFETs is not practicable for low-power device applications because of the high S/D junction leakage due to insufficient activation and rapid diffusion of n-type dopants in Ge [9, 11, 14, 15]. Thus, as compared to the best Ge/GeO₂ or Ge/GeO₂/high- k MOSFETs, our self-

aligned Ge QD/SiO₂/SiGe gate-stacking heterostructure possesses comparable interfacial properties (D_{it}) and subthreshold swing behavior ($S.S.$). However, the significant advantage of our approach over the conventional state-of-the-art is our fabrication in a single-step, self-organized oxidation process, with the preferred, thermally stable, robust interfacial SiO₂ layer rather than the unstable GeO₂. Most importantly, our high $I_{\text{on}}/I_{\text{off}} > 10^6$ is simultaneously achieved within our designer Ge QD/SiO₂/SiGe channel nMOSFETs with S/D junctions that are n⁺/p Si homojunctions just like in conventional Si MOSFETs.

As mentioned above, our heterostructured Ge QD/SiO₂/SiGe channel also provides an effective building block for the realization of Ge nanocrystal-based floating gate memories. Thanks to the considerable barrier height adjacent the Ge QD for confining both electrons (~ 3.2 eV) and holes (~ 5 eV), significant charge storage stability is achieved within the Ge QDs. This important property was confirmed by counterclockwise and clockwise C - V hysteresis loop measurements in n- and p-MOS capacitors for electron and hole storage, respectively (Fig. 4a). The slopes of C - V curves prior to and following charge injection are nearly unchanged. The nearly indiscernible frequency-induced dispersion and stretch out in C - V characteristics (Fig. 2a), suggests that the charge is primarily stored within the QDs rather than being captured by interface traps or deep traps within Si₃N₄. The Ge QD, floating gate memory effect is further evidenced by a threshold voltage (V_{th}) shift of $\Delta V_{\text{th}} \sim 0.42$ V, which was measured by applying gate voltage pulse under low-voltage programming (+8 V/60 msec) and erasing (−5 V/30 msec) conditions, as shown in Fig. 4b. ΔV_{th} is defined by the difference in gate voltage for these two conditions at a constant drain current value of 1 nA/ μm in channel width. Also, thanks to the very thin, 4-nm-thick tunneling oxide, our Ge QD floating gate memory allows low-voltage programming and erasing at +8 and −5 V, respectively. These voltages are

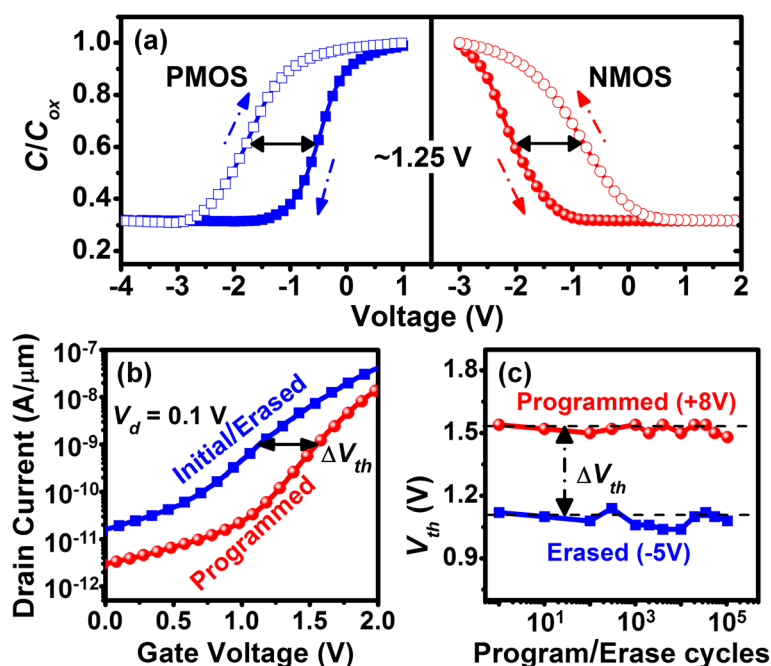


Fig. 4 **a** Hysteresis loop characteristics with voltage shift as large as 1.25 V are observed for both n- and p-MOS capacitors when the gate bias is swept from inversion to accumulation conditions. **b** I_D - V_G and **c** memory endurance characteristics of Ge QD floating gate memories under a +8 V/60 msec pulse programming and a -5 V/30 msec pulse erasing. The I_D - V_G characteristics are swept from 0 to 2 V. ΔV_{th} of ~ 0.42 V is achieved with negligible ΔV_{th} degradation following 10^5 program/erase cycles

almost one half of the corresponding voltages required for state-of-the-art floating gate memory devices [24–26] and definitely very desirable from a reliability perspective. A good memory endurance of more than 10^5 cycles with negligible ΔV_{th} degradation is measured for our Ge QD devices (Fig. 4c) under the programming/erasing conditions of +8 V/-5 V. The above result is a further demonstration of the good charge storage capability and also confirms the electrical robustness of the thin, interfacial SiO_2 layer.

Conclusions

We have demonstrated a unique approach for generating self-aligned $\text{SiO}_2/\text{Ge QD}/\text{SiO}_2/\text{SiGe}$ shell MOS heterostructures using a single oxidation step of SiGe nanopillars over a buffer Si_3N_4 layer on the Si substrate. Further, we have realized Ge QD floating gate memory devices based on this designer heterostructure. Superior interfacial morphologies and high-quality electrical properties of the $\text{SiO}_2/\text{Ge QD}/\text{SiO}_2/\text{SiGe}$ shell heterostructure have been multiply confirmed by extensive TEM, EDX, I - V , and C - V characterization. Thanks to the thin and robust tunneling oxide, charge storage within the Ge QDs produces considerable voltage shifts under relatively low-voltage programming/erasing conditions with good memory endurance characteristics.

Our self-aligned, Ge QD-based, gate-stacking structure is analogous to the prevailing poly-Si/ SiO_2 /Si MOS

structure and indeed provides a practically achievable core building block for Ge-based MOS devices with size-tunable Ge gates, SiO_2 gate oxide, and SiGe channels. It is worthwhile to point out the electronic performance advantages of the single-crystalline SiGe shell arising both from having superior interface properties as well as being in a state of compressive stress inherently generated during the fabrication process, which are favorable for the production of high-performance p-MOSFETs. Further device structure design including the pillar (or QD) density and gate area is undergoing for the optimal performance of n- and p-MOSFETs. Thus, we believe that our self-aligned heterostructure is a very promising functional candidate for the realization of next-generation, high-performance SiGe (or Ge) MOSFETs, using the precise control available through our self-organized, single-step fabrication process.

Competing Interests

The authors declare that they have no competing interests.

Authors' Contributions

WL conceived the experimental work and contributed to data analysis and the manuscript preparation. KY and TH performed structure/device fabrication and characterization. PHL carried out the Raman examination and analysis. TG conceived the mechanism of heterostructure formation and revised the manuscript. PWL conceived the study, revised the manuscript, and supervised the work. All authors read and approved the final manuscript.

Acknowledgements

This work was supported by the Ministry of Science and Technology of Republic of China (MOST-102-2221-E-009-195-MY3) as well as by the Asian Office of Aero-space Research and Development under contract no. FA 2386-14-1-4008.

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Received: 23 March 2015 Accepted: 8 May 2015

Published online: 19 May 2015

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