O_2-Plasma Passivation Effects on Polysilicon Thin Film Transistors Using Ion Plating Method

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ABSTRACT

A novel method has been developed for efficiently reducing defect density in polysilicon thin film transistors using ion plated oxides as capping layers. The characteristics of these novel thin film transistors are superior to those of thin film transistors with plasma-enhanced chemical vapor deposited tetraethylorthosilicate capping oxides due to an in situ O_2-plasma passivation effect during ion plating oxide deposition. The passivation effect of a NH_3 plasma on the novel devices was also studied. The in situ ion plating O_2 plasma shows a better passivation efficiency on trap states than the NH_3 plasma. Polysilicon thin film transistors with ion plating capping oxides are hardly degraded even when stressed with a bias of 20 V at 100°C.

Introduction

It is well known that polycrystalline silicon (poly-Si) films have a high concentration of grain boundary defects as well as intragrain defects. As a result of the high density of trapping states in poly-Si films, it has been found necessary to passivate them to improve poly-Si thin film transistor (TFT) performance.[1,2] Various technologies have been proposed to reduce trapping states in poly-Si films, such as hydrogenation,[1-4] O_2 plasma,[5] and NH_3 plasma.[6] So far, the most popular passivation procedure has been to expose devices to hydrogen plasma. However, it takes a long time to achieve satisfactory performance, and the improvement shows a tendency to saturate.[4] In addition, hydrogenated TFTs are quite prone to reliability problems due to carrier-induced trap states in poly-Si channels.[7,8] These shortcomings greatly limit the practical application of H_2-plasma passivation. In recent years, the passivation effect of an O_2 plasma has attracted much attention because of its better passivation efficiency and stability.[5] It has been suggested that O_2-plasma treatment can improve the performance of poly-Si TFTs by passivating deep states and tail states. Furthermore, it has been reported that after an O_2-plasma treatment, subsequent treatment with a H_2 plasma was even more efficient in passivating trap states in poly-Si films.[5]

Recently, a low-temperature ion plating (IP) method has been proposed to prepare high-performance oxide films. IP oxide has been shown to be feasible for application as a poly-Si TFT gate insulator, and to contribute to excellent device characteristics.[9] Since an O_2 plasma is present in the chamber during IP oxide deposition, it can be expected to have the effect of trap-state passivation on the poly-Si layer. In this paper, we try to apply IP oxides as capping layers on poly-Si TFTs, and investigate passivation effects owing to the in situ O_2 plasma. The passivation of dangling bonds is examined by electron spin resonance (ESR) measurement.[10,11] NH_3-plasma passivation effects and the reliability of the novel poly-Si TFTs are also studied.

Experimental

Preparation of IP oxide.—IP oxide films were prepared using the ion-plating system (Balzers BAP 800),[9,12,13] shown in Fig. 1. The starting silicon material was evaporated using an electron-beam evaporator. Simultaneously the evaporator crucible served as the anode for an argon plasma discharge. The high arc current was 56 A, while the low arc voltage (V_{arc}) was 66 V and the anode-to-ground voltage (V_{anode}) was 46 V. Argon at 3.9 mbar in the plasma source cavity was ionized by the heated filament, and it was at 3.4×10^{-4} mbar in the deposition chamber. Oxygen gas was let directly into the deposition chamber to fix the deposition pressure at 1.1×10^{-3} mbar, while the base pressure was 3.6×10^{-5} mbar. The evaporant (Si) and the reactive gas (O_2) were activated and ionized by the argon plasma. The substrate holder was electrically isolated from the ground chamber without an applied bias, i.e., it was allowed to float. The substrate gathered electrons from the plasma sheath, and then obtained a negative self-bias (V_s) of −10 to −20 V (the body of the plasma). This negative bias accelerated the positive ions of the evaporant (Si), the reactive gas (O_2), and the argon plasma onto the surface of the substrate, and the film formed. The positive ions tended to neutralize the received electrons, but the substrate was able to gather additional electrons from the plasma sheath immediately. The IP oxide film was deposited at a rate of 0.2 nm/s. No heater was applied to the substrate holder during deposition.

In conventional IP system the degree of ionization is too low to effectively deposit film, so the accelerating voltage must be rather high (generally 3 ~ 5 kV with a current density of 0.3 ~ 0.8 mA/cm^2) to supply sufficient energy.[14,15] In addition, the small quantity of ions is also disadvantageous for a reactive gas process. To overcome these prob-

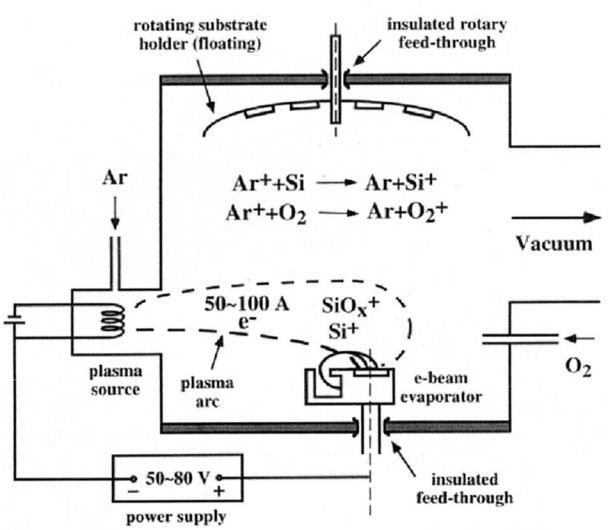

Fig. 1. Schematic diagram of the ion-plating system (Balzers BAP 800).

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lems, a new IP system of BAP 800 has been developed.[16] In this new system the evaporant and the reactive gas can be effectively ionized and activated by a low-voltage (50 ~ 80 V) high-current (50 ~ 100 A) plasma arc. The arc current can be controlled directly, while the resultant arc voltage is also monitored. With respect to ground, a positive potential (V_{anode}) of 40 ~ 60 V is applied to anode. It is recommended to have a potential difference of +20 V between V_{arc} and V_{anode}. Positive ions (Ar, evaporant, and reactive gas) will be accelerated to the substrate holder owing to a negative self-bias (−10 to −20 V) $V_s = V_p - V_f$, where V_p and V_f are the plasma and the substrate floating potential, respectively. The film quality is thus improved because of high-energy atoms and the high-reactivity plasma.[17]

Fabrication of poly-Si TFTs.—Conventional co-planar N-channel poly-Si TFTs were prepared using the following procedures. The cross-sectional structure of the poly-Si TFTs is shown in Fig. 2. A 100 nm thick low-pressure chemical vapor deposition (LPCVD) amorphous Si layer was deposited on thermal oxide at 550°C using SiH_4 gas. Recrystallization was performed at 600°C for 24 h using the solid-phase crystallization (SPC) method. A 40 nm thick liquid-phase deposited (LPD) oxide layer[18] was grown on the island-patterned SPC layer at 18°C, and then densified at 600°C for 1 h in O_2 ambient. A 300 nm thick poly-Si layer was deposited using the LPCVD method at 620°C. After the poly-Si gates were patterned, the source/drain and gate regions were implanted with phosphorus ions (40 keV, 5×10^{15} cm^{-2}) by self-aligned technology. Dopant activation was performed at 600°C for 24 h in N_2 ambient. The 500 nm thick capping layer was deposited at a rate of 0.2 nm/s for about 42 min using the IP method. The temperature of the substrate was 23°C at the beginning of the IP oxide deposition process, and increased to 110°C at its end. After contact holes were opened, aluminum electrodes were prepared and sintered at 400°C for 30 min in N_2 ambient. The maximum processing temperature was 620°C.

For comparison, poly-Si TFTs with 32.5 nm thick LPD gate oxides and 500 nm thick tetraethyl orthosilicate (TEOS) capping oxides were prepared. The TEOS oxide was deposited at 300°C using the plasma-enhanced CVD (PECVD) method. Hydrogenation by the NH_3-plasma treatment was performed in a parallel-plate reactor at 300°C with a power density of 0.7 W/cm^2.

ESR measurements.—The dangling bond density in poly-Si films was measured by room-temperature ESR absorption spectra (X-band) before and after the in situ O_2-plasma treatment. Poly-Si films were prepared by the LPCVD method at 620°C to a thickness of 300 nm onto thermally oxidized Si-wafer. IP oxide was directly deposited on the poly-Si films, and then annealed at 400°C for 30 min in N_2 ambient. This is because devices were sintered after metallization in TFT fabrication processes. The deposition condition of IP oxide was the same as that of the IP capping oxide for poly-Si TFTs. Before ESR measurements, the IP oxide and the back side poly-Si/thermal oxide were removed.

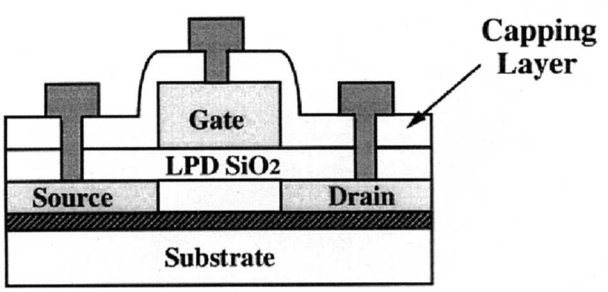

Fig. 2. Cross-sectional structure of the poly-Si TFTs.

Table I. Physicochemical and electrical properties of IP and thermal oxides.

	Ion plating oxide	Thermal oxide
FTIR stretching frequency (cm^{-1})	1056	1076
Refractive index	1.483	1.463
P-etch rate (Å/s)	4.9	2.0
Leakage current density at 4 MV/cm (A/cm^2)	8.5×10^{-10}	1.1×10^{-9}
Dielectric breakdown field (MV/cm)	9.3	9.4
Dielectric constant at 1 MHz	4.5	3.9
Flatband voltage (V)	−0.67	−1.68
Interface state density (eV^{-1} cm^{-2})	1.83×10^{10}	4.50×10^{9}

Results and Discussion

IP oxide characteristics.—Table I summarizes the typical physicochemical and electrical properties of 97 nm thick IP oxide deposited at room temperature. Those of thermal oxide (~97 nm) grown in dry O_2 at 1000°C are also shown for comparison. These two kinds of oxides were all prepared on 3 in. p-type (100)Si substrates. The thickness and the refractive index were measured by ellipsometer, while the chemical structure was analyzed by Fourier transform infrared spectrophotometer (FTIR). The etching rate was examined with P-etch solution (48% HF: 70% HNO_3: H_2O = 3:2:60) at room temperature. To investigate the electrical properties of these oxides, metal-oxide-silicon (MOS) capacitors with aluminum gates were prepared. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics were measured with an HP4145B and a Keithley Package 82 system, respectively.[9] The IP oxides have a lower FTIR stretching frequency, a higher refractive index, a higher P-etch rate, and a higher dielectric constant. These features suggest that IP oxide is a high-density material with strained bonds.[9,19] The electrical properties of IP oxide are comparable to those of thermal oxide, and include low leakage current, high dielectric breakdown field, and few oxide charges. These excellent properties suggest that IP oxide is feasible for application as a capping layer in poly-Si TFTs.

Characteristics of poly-Si TFTs with IP oxides as capping layers.—Figure 3 shows the transfer characteristics of both poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers, respectively. The charac-

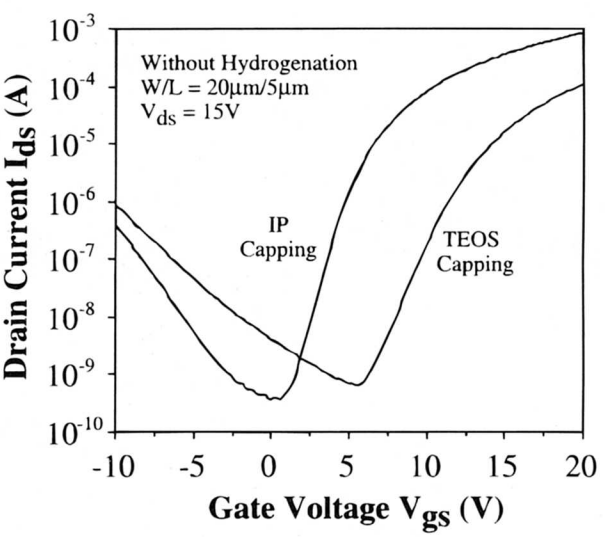

Fig. 3. Typical transfer characteristics (I_{ds}-V_{gs}) at V_{ds} = 15 V for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers without hydrogenation.

Table II. Device characteristic parameters for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS capping layers before and after 8 h NH_3-plasma treatment.

Capping layer	NH_3-plasma treatment	V_{th} (V)	S.S. (V/dec)	I_{on}/I_{off}	μ_{FE} (cm^2/V s)	N_t (cm^{-2})
IP	No	4.23	0.94	4.10×10^6	24.3	1.05×10^{13}
	8 h	2.33	0.77	3.18×10^6	25.6	8.37×10^{12}
TEOS	No	11.0	1.61	2.09×10^6	9.71	2.70×10^{13}
	8 h	5.49	0.84	4.75×10^6	14.4	1.05×10^{13}

teristics were measured at V_{ds} = 15 V before hydrogenation. The IP capped device obviously exhibits better performance than that of the TEOS capped device, even when the TEOS capped device has a thinner LPD gate insulator. The key characteristic parameters of the two samples are summarized in Table II. Compared to the TEOS capped device, the IP capped device shows a smaller threshold voltage (V_{th}) of 4.23 V, a smaller subthreshold swing (S.S.) of 0.94 V/dec, a higher on/off current ratio (I_{on}/I_{off}) of 4.10×10^6, and a higher field-effect mobility (μ_{FE}) of 24.3 cm^2/V s. It is evident that the use of IP capping oxides indeed improves the performance of poly-Si TFTs. The above-mentioned superior device characteristics suggest that the IP capped device has a lower trap-state density (N_t) in the poly-Si channel. We can further calculate the effective trap-state density using the modified Levinson theorem.[20,21] The N_t in the IP capped device is 1.05×10^{13} cm^{-2}, while it is 2.70×10^{13} cm^{-2} in the TEOS capped device. We believe that the decrease in N_t for the IP capped device can be attributed to the effect of in situ O_2-plasma passivation during the deposition of IP capping oxides.

To directly evaluate the variation of defects after the in situ O_2-plasma treatment, dangling bond density in poly-Si films was also measured using ESR. Figure 4 shows the ESR absorption spectra with a resonance at g = 2.0055 for the poly-Si films before and after capping IP oxide. The ESR signal intensity decreases after capping IP oxide, which indicates the reduction of the spin density (N_s) in poly-Si films. N_s is 6.68×10^{18} cm^{-3} for the fresh specimen (before capping IP oxide), while it is 5.32×10^{18} cm^{-3} for the IP capped specimen before annealing. It is evident that Si dangling bonds decrease after capping IP oxide. Moreover, N_s is further reduced to 3.12×10^{18} cm^{-3} for the IP capped specimen after 400°C annealing. The anneal enhances oxygen diffusion and passivation efficiency. Hence, we can demonstrate that IP capping oxide indeed possesses passivation effects.

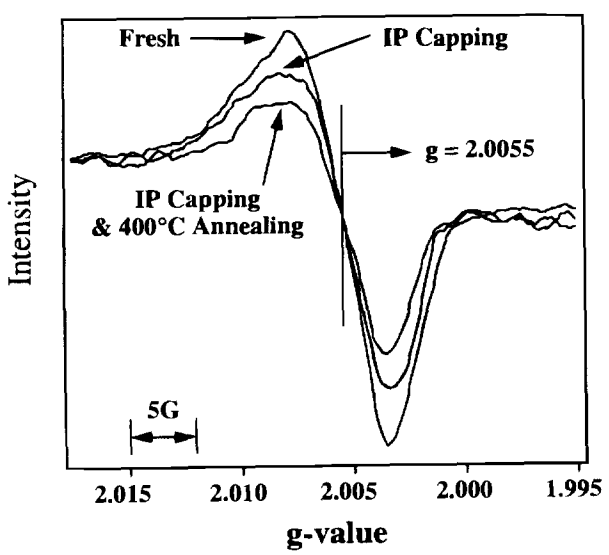

Fig. 4. ESR absorption spectra with a resonance at g = 2.0055 for the poly-Si films before and after capping IP oxide.

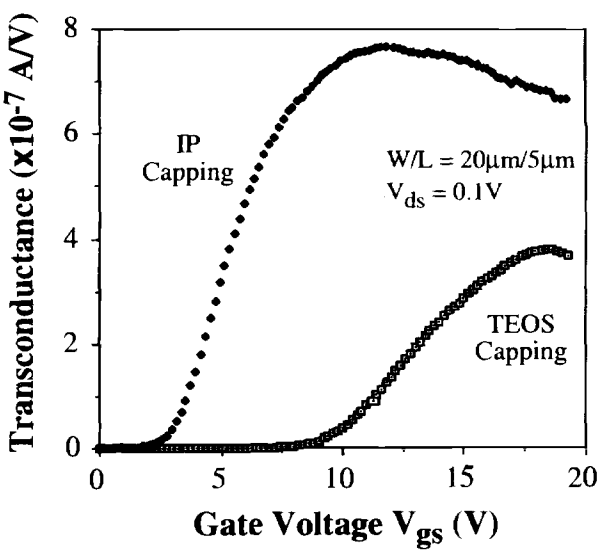

Fig. 5. Transconductance (Gm) as a function of gate bias at V_{ds} = 0.1 V for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers.

Figure 5 shows transconductance (Gm) as a function of gate bias measured at V_{ds} = 0.1 V for both IP capped and TEOS capped poly-Si TFTs (W/L = 20/5 μm). The maximum Gm is 7.6×10^{-7} A/V for the IP capped device, while it is 3.8×10^{-7} A/V for the TEOS capped device. In addition, the gate voltage yielding the maximum Gm is also comparatively small for the IP capped device. Figure 6 shows the output characteristics (I_{ds}-V_{ds}) with V_{gs}-V_{th} = 2 V and 6 V for both IP capped and TEOS capped devices (W/L = 20/10 μm). In the curves of IP capped device, both the high slope in the linear region and the high saturation current imply that channel conductance is high. Generally in poly-Si TFTs, the transport of free carriers between the grains is impeded by the potential barrier owing to the trap states at the grain boundaries.[22,23] The lower barrier height makes On-state performance respond much faster to the applied gate and drain biases. In the IP capped device, the increases in transconductance and channel conductance can be attributed to the lowering of barrier height due to the reduction of trap-state density.

Figure 7 shows the transfer characteristics in the low gate bias region at V_{ds} = 5, 10, and 15 V for both IP capped

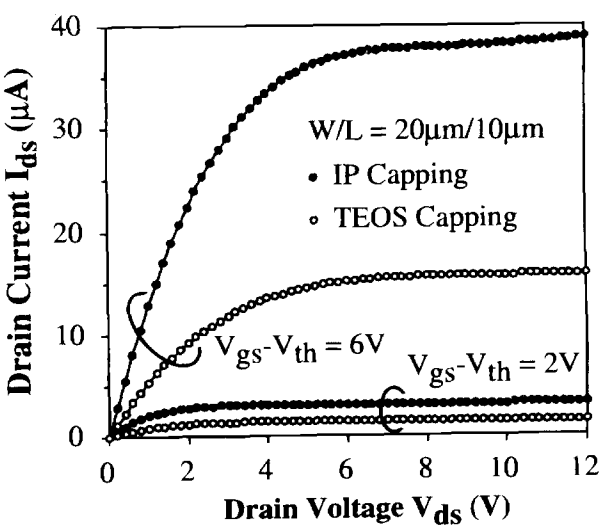

Fig. 6. Output characteristics (I_{ds}-V_{ds}) with $V_{gs}-V_{th}$ as a parameter for poly-Si TFTs (W/L = 20/10 μm) with IP and with TEOS oxides as capping layers.

and TEOS capped poly-Si TFTs without hydrogenation (W/L = 20/5 μm). In the case of V_{ds} = 5 V, the IP capped device shows a rather flat leakage characteristic independent of gate bias except for a higher minimum leakage current (I_{min}). The minimum leakage current is dominated by the channel resistance.[24] In this region, the barrier height that transfer carriers have to surmount at the grain boundary will govern the magnitude of the minimum leakage current. The higher the barrier height, the lower the minimum leakage current observed. Because there is a lower trap-state density in the IP capped device, the barrier height and thus the channel resistance are lower than those in the TEOS capped device. Thus, I_{min} is a little higher in the IP capped device. When the drain voltage was increased to 15 V, I_{min} was dominated by Frenkel-Poole emission in the drain junction depletion region.[24] Frenkel-Poole emission current is contributed by field-enhanced thermal excitation of trapped holes in the valence band. Owing to the lower trap-state density, the IP capped device exhibited a lower leakage current than the TEOS capped device at V_{ds} = 15 V. In addition, when the drain bias was increased, the leakage current in the IP capped device also showed a smaller variation due to its lower trap-state density.

Some authors have reported that for poly-Si TFTs an O_2-plasma-treatment cannot passivate grain boundary defects according to the unchanged ESR signals of defect density. The O_2 plasma can only clean the device surface and grow a thin SiO_2 layer, which can reduce the surface leakage current.[25] However, our studies show that the improvement in IP capped TFTs is assuredly due to the in situ O_2-plasma passivation effect. As shown in Fig. 4, the reduced spin density owing to capping IP oxide indicates that the IP process possesses passivation effects. In addition, to clarify the influences of IP process and surface cleaning, we also prepared a IP/TEOS capped TFT sample. After capping IP oxide on TFTs and annealing at 400°C for 30 min in N_2 ambient, we removed the IP oxide using HF solution and then deposited TEOS capping oxide. For the TEOS capped TFT, we also ever removed the native oxide on the surface before capping TEOS oxide. It means that the IP/TEOS capped TFT and the TEOS capped TFT have the same surface conditions. We found that the IP/TEOS capped TFT and the IP capped TFT exhibit almost the same characteristics. It reveals that for the IP/TEOS capped TFT the trap states have been effectively reduced even though the IP capping oxide is removed. We can conclude that for the IP capped TFTs the improvement is due to the IP plasma treatment instead of the surface cleaning.

It has been reported that the passivation during O_2-plasma treatment is due to the incorporation of hydrogen, which is activated by electron-impact dissociation of water vapor.[26] In the BAP 800 IP system, the residual water pressure is about 10^{-7} mbar at a base pressure of 4×10^{-5} mbar at 23°C, while it is about 10^{-9} mbar at the substrate temperature of 300°C. We also prepared IP capped TFTs with the deposition of IP oxide at 300°C. TFTs with high-temperature IP oxide exhibit more excellent characteristics than those with room-temperature IP oxide. It is hard to believe that the hydrogen passivation will occur in such low residual water pressure. In addition, generally the hydrogen-passivated dangling bonds are easily broken at annealing temperature greater than 400°C.[5,27,28] However, as shown in Fig. 4, the dangling bonds decrease after 400°C annealing. We conclude that the passivation effect during IP process can be attributed to the in situ O_2 plasma.

Effects of NH_3-plasma passivation.—The poly-Si TFTs in this research were exposed to the NH_3 plasma for trap-state passivation to further improve their performance. Figure 8 shows the typical transfer characteristics of both IP capped and TEOS capped poly-Si TFTs before and after an 8 h NH_3-plasma treatment at V_{ds} = 5 V (W/L = 20/5 μm). Device performances were both improved after this 8 h NH_3-plasma treatment. The key characteristic parameters after the NH_3-plasma treatment are also summarized in Table II. Although the improvement in the TEOS capped devices is more apparent after the NH_3-plasma treatment, in total the characteristics of IP capped devices are still superior to those of TEOS capped devices. For both IP capped and TEOS capped TFTs, the minimum leakage current did not well decrease after 8 h NH_3-plasma treatment. It can be attributed to the insufficient passivation time. Generally, I_{min} is dominated by the total resistance in active layer. The total resistance is composed of the junction resistance at the drain junction and the channel resistance. When the passivation is insufficient, I_{min} is dominated by the channel resistance. The decrease of trap states after NH_3-plasma treatment can result in the reduction in barrier height. The lower the barrier height, the lower the channel resistance, and then the higher I_{min} is observed. However, after NH_3-plasma passivation the leaky junction depletion can also be passivated resulting in an increased junction resistance. When the passivation is sufficient, the junction resistance can become larger than the channel resistance. In that case, I_{min} can be dominated by the junction resistance and become reduced.[4,29-31]

Figure 9 shows a comparison of subthreshold swing between IP capped and TEOS capped devices as a function of NH_3-plasma passivation time. It was found that the improvement in the IP capped device saturated after 2 h.

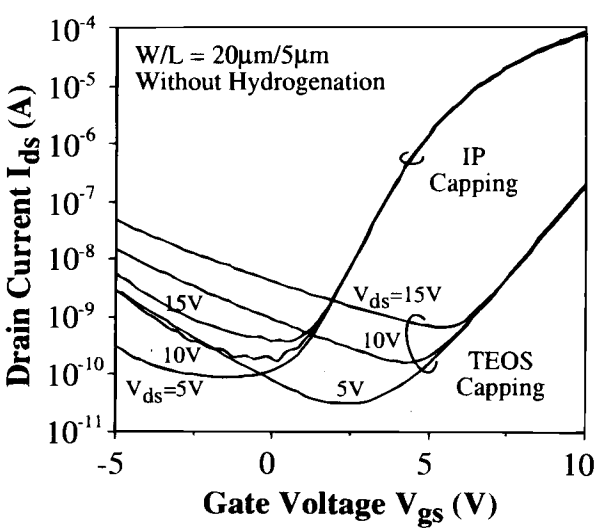

Fig. 7. Transfer characteristics (I_{ds}-V_{gs}) in low gate bias region at V_{ds} = 5, 10, and 15 V for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers without hydrogenation.

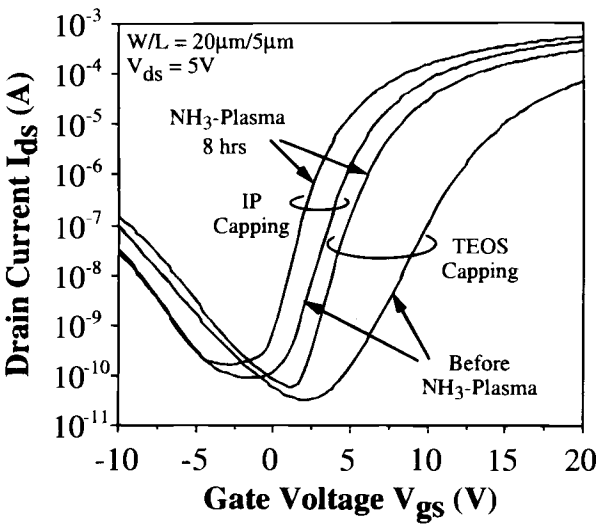

Fig. 8. Transfer characteristics (I_{ds}-V_{gs}) at V_{ds} = 5 V for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers before and after 8 h NH_3-plasma treatment.

However, there was a dramatic improvement in subthreshold swing for the TEOS capped device when the NH_3-plasma passivation time was increased. The threshold voltage change tendencies for both types of device after the NH_3-plasma treatment were similar to those for subthreshold swing. The apparent improvement in S.S. and V_{th} for TEOS capped devices can be attributed to a reduction of midgap deep states after NH_3-plasma passivation.[4,32] The improvement for IP capped devices appears smaller and quickly saturated because many deep states were passivated by the in situ O_2 plasma during IP capping oxide deposition, and only some residual deep states could be further passivated by the NH_3-plasma treatment. Figure 10 shows the changes in field-effect mobility as a function of NH_3-plasma passivation time for IP capped and TEOS capped devices. The gradual increase in μ_{FE} for the TEOS capped devices indicates that some tail states were passivated by the NH_3-plasma treatment.[3,32] However, the improvement saturated after the 8 h NH_3-plasma treatment, and the saturated μ_{FE} was still smaller than that of the as-fabricated IP capped device. This indicates that the in situ O_2-plasma treatment can more effectively passivate the tail states in the poly-Si films than the NH_3-plasma treatment. Hence, the subsequent NH_3-plasma treatment nearly has no influence on μ_{FE} for IP capped devices. The above results support the feasibility of fabricating excellent poly-Si TFTs without additional hydrogenation.

For PECVD TEOS capped TFTs, it must be clarified whether the requirement of more hydrogen passivation is due to PECVD TEOS charge damage. If there is serious charge damage during PECVD TEOS process, the characteristics of IP/TEOS capped TFTs will be worse than those of IP capped TFTs. However, we did not find this phenomenon. Therefore, the PECVD TEOS charge damage can be ignored.

Stability of in situ O_2 plasma passivation.—The stability of poly-Si TFTs is of significant importance from a long-term operation standpoint. It has been reported that H_2-plasma treated devices exhibited higher degradation rates than O_2-plasma treated devices.[5] In this section, the stability of as-fabricated IP capped TFTs and NH_3-plasma treated TEOS capped TFTS is investigated.

To accelerate degradation and investigate thermal stability, both the as-fabricated IP capped devices and the 10 h NH_3-plasma treated TEOS capped devices were stressed with $V_{ds} = V_{gs} = 20$ V at 150°C. Figure 11 (a) and (b) show the changes in transfer characteristics for the two devices before and after stressing for 10^4 s. The degradation of the TEOS capped devices is very noticeable. The S.S. increased from 0.82 to 1.27 V/dec, while the V_{th} increased from 5.30 to 8.87 V because high-temperature dc stressing appears to break the Si-H bonds, resulting in additional trap states generated at grain boundaries.[7,23] Hence, the stressing degrades the S.S. and V_{th} characteristics of the TEOS capped devices toward prehydrogenated values. On the other hand, the degradation of the as-fabricated IP capped devices was slight because of the higher bond strength of Si-O bonds over that of Si-H bonds.[34-36] Hence, fewer additional trap states were generated during high-temperature dc stressing for devices treated with in situ O_2-plasma passivation. Figure 12 shows the subthreshold swing degradation rate (ΔS.S.) as a function of stress temperature for the as-fabricated IP and the NH_3-plasma treated TEOS capped devices under stressing at $V_{ds} = V_{gs} = 20$ V for 10^4 s. ΔS.S. for the NH_3-plasma treated TEOS capped device appears very sensitive to and seriously affected by the stressing temperature. However, ΔS.S. for the IP capped device appears rather stable until the temperature exceeded 100°C. From this result, it can be concluded that the novel poly-Si TFTs with IP capping oxides indeed exhibit good stability even when stressed at high temperatures and high biases.

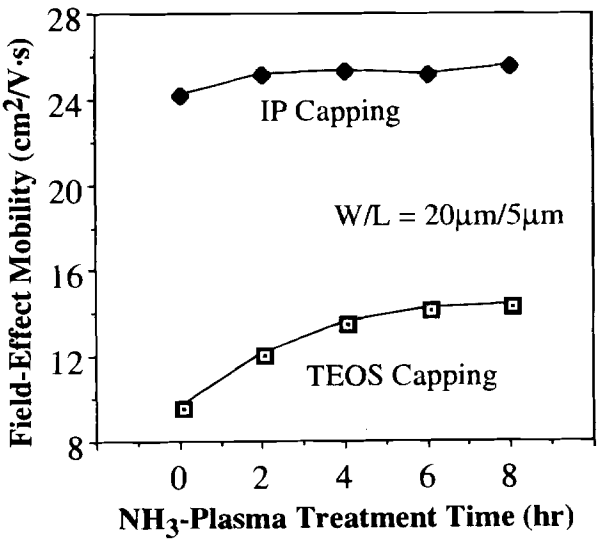

Fig. 10. Field-effect mobility as a function of NH_3-plasma passivation time for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers.

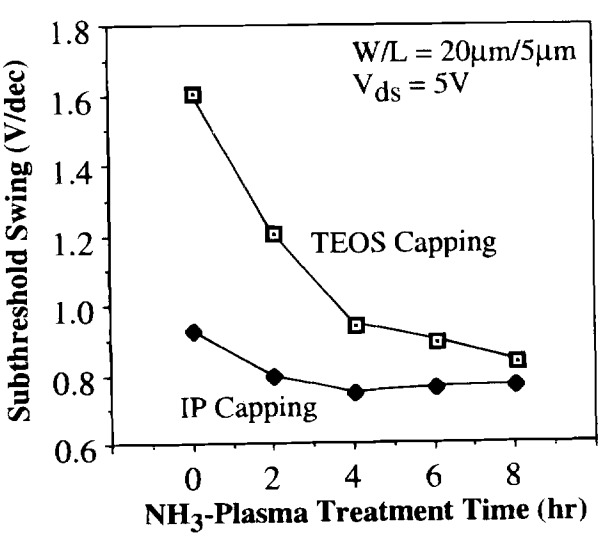

Fig. 9. Subthreshold swing as a function of NH_3-plasma passivation time for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers.

Conclusions

Poly-Si TFTs with IP oxides as capping layers exhibit excellent performance, which is due to in situ O_2-plasma passivation effect during IP process, not the material of IP oxide itself. The in situ O_2-plasma treatment effectively reduces the trap states in poly-Si films, resulting in a threshold voltage of 4.23 V, a subthreshold swing of 0.94 V/dec, a field-effect mobility of 24.3 cm^2/V s, and an On/Off current ratio of 4.10×10^6 without hydrogenation. Poly-Si TFTs with IP capping oxides also show a small increase in leakage current as drain bias is increased. Because most of the trap states (particularly the tail trap states) are passivated by the O_2 plasma, the improvement provided by the NH_3-plasma treatment of poly-Si TFTs with IP capping oxides is not very evident. It is feasible to fabricate these novel poly-Si TFTs without additional hydrogenation. The novel devices also show superior stability even under stressing at 100°C with high V_{gs} and V_{ds}.

Acknowledgment

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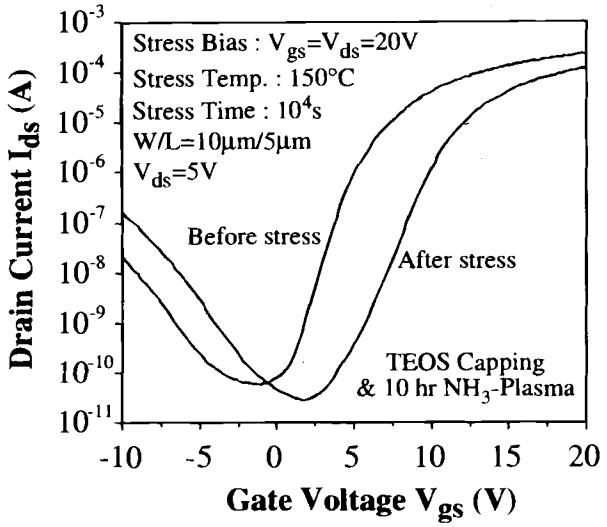
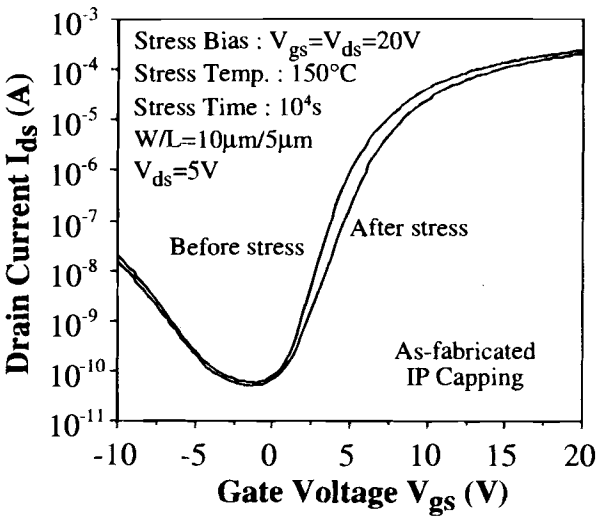


(a)



(b)

Fig. 11. Changes in transfer characteristics (I_{ds}-V_{gs}) under stress of V_{ds} = V_{gs} = 20 V for 10^4 s at 150°C for (a) TEOS capped devices after NH_3-plasma treatment, and (b) as-fabricated IP capped devices (W/L = 10/5 μm).

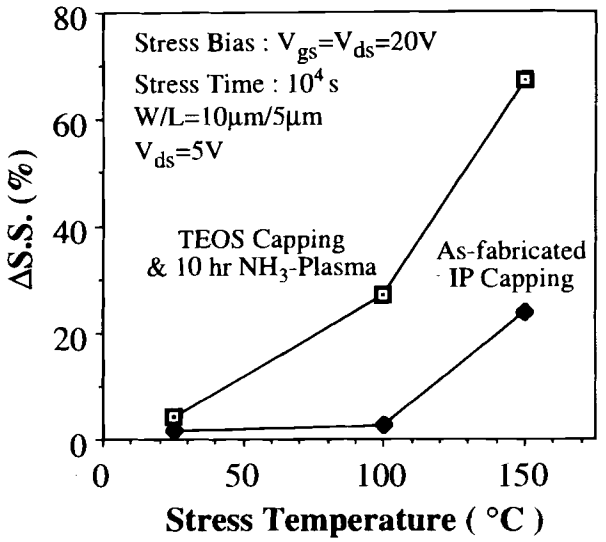


Fig. 12. Subthreshold swing degradation rates (ΔS.S. (%)) under stresses of V_{ds} = V_{gs} = 20 V for 10^4 s at 25, 100, and 150°C for TEOS capped devices after NH_3-plasma treatment and as-fabricated IP capped devices (W/L = 10/5 μm).

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Boron Diffusion in Compressively Stressed Float Zone-Silicon Induced by Si_3N_4 Films

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ABSTRACT

The effect of stress during annealing induced by Si_3N_4 films on boron diffusion in float zone-silicon has been studied and a correlation between vacancy concentration and compressive strain in the substrate has been clarified. From the results of Si_3N_4 film thickness and annealing temperature dependence on both boron diffusivity and stress in the substrates, boron diffusion was found to be retarded and the substrate was found to have high stress, having elastic compressive strain during annealing under Si_3N_4 films. These results indicate that excess vacancies are generated by elastic compressive strain, causing the retardation of interstitial-mediated diffusion of boron.

Introduction

Silicon nitride (Si_3N_4) films have been used as an oxidation mask and passivation materials in ultra-large-scale integration (ULSI) process technology. Si_3N_4 films deposited on Si have high stress and produce effects on Si substrates such as the generation of dislocations[1] during thermal annealing.

With the shrinkage of device dimensions, precise control of dopant profiles in the substrate becomes more and more important. Therefore, it is very important to study the effects of stress in the films on both the Si substrate surface and on dopant diffusion.

It is known that chemical vapor deposition (CVD) silicon nitride films develop intrinsic stress during deposition and thermal stress during annealing, influencing dopant diffusion. Ahn et al.[2] reported retarded diffusion of P, enhanced diffusion of Sb, and an increase in the shrinkage rate of extrinsic stacking faults in float zone (FZ)-Si under the low-pressure CVD (LPCVD) SiN_x films by varying the stress level in the films with different values of x. Osada et al.[3] investigated retarded diffusion of boron in FZ-Si under electron cyclotron resonance (ECR) plasma CVD Si_3N_4 films by changing annealing temperature, annealing time, and the film thickness in detail.

These reports suggest that stress of Si_3N_4 films disturbs the point defect concentration in the silicon substrate during annealing. However, stress of Si_3N_4 films was measured only after the film deposition. The change of the intrinsic stress of the films and the actual stress during annealing have not been taken into consideration.

In this study, we first investigated the stress of Si_3N_4 films deposited by ECR plasma CVD on FZ-Si as a function of the film thickness and the thermal history. Then, the effect of stress induced by Si_3N_4 films on boron diffusion in FZ-Si was studied by changing Si_3N_4 film thickness and annealing temperature. Correlation between the stress at the surface of the Si substrate and the retardation of boron diffusion has been clarified from these results. Retarded diffusion of boron will be discussed in terms of the excess vacancy generation.

Experimental

Substrates used were p-type, 525 μm thick (100) FZ-Si with resistivity of 4 ~ 6 Ω cm for the measurement of boron diffusion and the observation of defects at the surface of the substrates. SiO_2 films with thickness of 50 nm were grown in dry O_2 at 1000°C for 60 min on samples. Boron ions were implanted into samples through SiO_2 with a dose of $3 \times 10^{13}/cm^2$ at 20 keV. This dose affirmed the so-called intrinsic conditions, in which the carrier concentration is smaller than the intrinsic carrier concentration at annealing temperatures. Samples were annealed in N_2 at 900°C for 30 min to remove the ion implantation induced damage. After removing SiO_2 films at the back side and at the top side selectively, Si_3N_4 films were deposited on samples at the top side by ECR plasma CVD at 100°C using SiH_4 and N_2. ECR plasma CVD allows to the deposition of thin films at lower temperature at low gas pressures in the range of 10^{-5} to 10^{-3} Torr, and does not need any thermal reaction.[4] Using this CVD system, high quality Si_3N_4 films can be obtained. The thickness of Si_3N_4 films was set to be 50, 100, 160, 430, and 790 nm. The structure of samples is shown in Fig. 1. The areas masked with SiO_2-Si_3N_4 films and masked with Si_3N_4 films were defined as the ON-area and the N-area, respectively.

Substrates used for the measurement of displacement were p-type, 625 μm thick (100) FZ-Si with resistivity of 11 to 25 Ω cm. They were mirror-polished at both sides and cut into a strip with length of 8 cm and width of 1 cm. Si_3N_4 films were deposited on the Si substrate by ECR plasma CVD with the same conditions mentioned above. The structure of the samples was the same structure as the N area shown in Fig. 1.

Thermal annealing was performed for all samples in N_2 at temperatures ranging from 900 to 1100°C for 360 min. Boron profiles were measured by secondary ion mass spectroscopy (SIMS ATOMIKA 6500). Stressed-induced

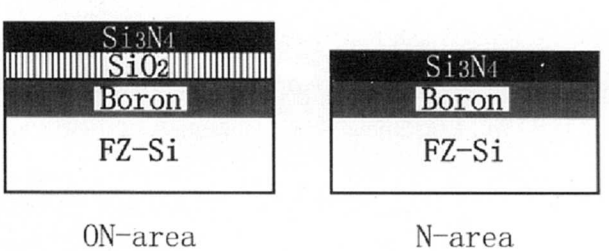

Fig. 1. Cross-sectional view of samples.