Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS

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Abstract

We have, for the first time, experimentally quantified random dopant distribution (RDD) induced V_t standard deviation up to 40mV for 20nm-gate planar CMOS. Discrete dopants have been statistically positioned in the 3D channel region to examine associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". As gate length further scaling down to 15nm, the newly developed discrete-dopant scheme features an effective solution to suppress 3-sigma-edge single digit dopants induced V_t variation by gate work function modulation. The extensive study may postpone the scaling limit projected for planar CMOS.

INTRODUCTION

So far, gate length scaling is still the most effective way to continue Moore's Law for transistor density increase and chip performance enhancement. However, as planar CMOS advances to sub-20nm gates, double-digit channel dopants make transistor behaviors more complicated to be characterized with conventional "continuum modeling", due to every "discrete" dopant has its significant weight to impact the resulted transistor performance. We herein developed a systematic method to experimentally extract the random dopant distribution (RDD) induced V_t fluctuation. Furthermore, a "discrete-dopant simulation", in good agreement with the experimental data, has been carried out to realize statistical analysis and to feature solutions for reducing the RDD induced V_t variation upon L_g scaling.

EXPERIMENTAL and CHARACTERIZATION

As gate length deviation (GLD), line edge roughness (LER), and random dopant distribution (RDD) are the major variation sources of threshold voltage [1-3], we thus can extract RDD induced standard V_t deviation, $\sigma V_{t,RDD}$, from the following approximated equation as $\sigma V_{t,total}$, $\sigma V_{t,GLD}$, and $\sigma V_{t,LER}$ can be directly measured from experimental data:

$$(\sigma V_{t,total})^2 \approx (\sigma V_{t,GLD})^2 + (\sigma V_{t,LER})^2 + (\sigma V_{t,RDD})^2 \quad (1)$$

In this work, excellent short-channel-effect control down to 20nm-gate has been experimentally realized (Fig. 1) with advanced shallow junction technology. We achieve junction depth around one half of gate length to maintain subthreshold leakage at 100nA/μm with channel doping ~5×10^{18}cm^{-3} and gate dielectric of 12Å EOT (equivalent oxide thickness). Furthermore, to have the insights of random-dopants-distribution effects, quantum mechanical transport simulation is performed and compared with experimental data (Fig. 3) by solving a set of calibrated 3D density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations [4]. All statistically generated discrete dopants, as shown in Fig. 5 (details in next paragraph), are advanced and incorporated into the 3D device simulation under our parallel computing system. Such large-scale simulation approach allows us to explore the electrical characteristic fluctuations induced by randomness of dopant number and position in the channel region concurrently. The mobility model, shown in Fig. 4, used in the 3D device simulation is quantified with our device measurements for the best accuracy.

Fig. 5 illustrates how to generate discrete-dopant channel for aforementioned simulation, concurrently capturing randomness of dopant number and dopant position. Fig. 5(a) shows the discrete dopants randomly distributed in $(100nm)^3$ cube with average concentration of 5×10^{18}cm^{-3}. There will be 5000 dopants within the $(100nm)^3$ cube, but dopants vary from 24 to 56 (average number is 40) within its 125 sub-cubes of $(20nm)^3$, as shown in Fig. 5(b), (c) and (e). These 125 sub-cubes are then equivalently mapped into channel region for the discrete dopant simulation (Fig. 5(d)). In principle, device simulation with the 125 channel structures almost covers $\pm3\sigma$ cases, shown in Fig. 5(e), and thus will be fairly meaningful to reflect statistic randomness of dopant number/position in channel region.

RESULTS and DISCUSSION

- **20nm-Gate Planar CMOS.** Fig. 1 and Fig. 2 show the experimental V_t fluctuation and I_{on}-I_{off} characteristics of NMOS transistors down to 20nm gates. As expected, the V_t roll-off characteristics of 20nm-wide devices are much more scattered than that of 200nm-wide devices. $\sigma V_{t,RDD}$ has then been experimentally extracted following the formula (1), as shown in Fig. 3. Discrete-dopant simulation for $L_g = W = 20nm$ (data represented with symbol * in Fig. 3) is in good agreement with the experimental data, which confirms the channel doping is randomly distributed as statistically modeled. Fig. 4(a) shows extracted mobility versus doping concentration from samples of Figs. 3(a) and (b). The low-field electron mobility at 0.3 MV/cm is greatly reduced with increasing doping concentration. That is why we limit our channel doping concentration at 5×10^{18}cm^{-3}, which corresponding to average 40 dopants in $(20nm)^3$ cubes and 17 dopants in $(15nm)^3$ cubes, as shown in Fig. 5 and Fig. 8, respectively. Less channel doping concentration may reduce $\sigma V_{t,RDD}$, but channel dopants will quickly approach to single-digit number, as shown in Fig. 4(b). Figs. 6(a)-(c) show I_{on}, I_{off}, and $V_{t,sat}$ distributions versus channel dopants of these 125 cases. Fig. 7(a) shows its I_{on}-I_{off} characteristics. Figs. 7(b)-(d) disclose 3 different discrete-dopant channels which have similar values of I_{on} or I_{off} but with various dopant distributions. Their corresponding cross-sectional off-state electrostatic potential and on-state current density at 1nm below gate oxide are also presented (Figs. 7(b')-(d'), and 7(b")-(d")), which clearly shows that distributions of the electrostatic potential and current density are closely related to the dopant arrangements within the cross-sectional area beside source side (Figs. 7(b)-(d)).
- **15nm-Gate Planar CMOS.** Based on experimental data and discrete modeling of 20nm gate with 12Å EOT, 8 Å EOT seems a "must" for 15nm-gate CMOS to mitigate the increase of the RDD induced V_t variation. With the same approach shown in Fig. 5 for generating discrete-dopant channels, Fig. 8(a) shows 343 sub-cubes of $(15nm)^3$ derived from $(105nm)^3$ cube with 5×10^{18}cm^{-3} doping. Fig. 9 shows the I_{on}-I_{off} characteristics and V_t distribution of these cases with 12Å and 8Å EOT. 8Å EOT shows tighter V_t scattering. Furthermore, as channel dopants could be only 7 at 3σ edge (Fig. 8(c)), we herein propose using higher work-function gate to increase its intrinsic electrostatic potential barrier height (Fig. 10(c)) to prevent source-to-drain punchthrough at off state (Fig. 10(b)). Thus $\sigma V_{t,RDD}$ can be maintained while L_g scaling down to 15nm from 20nm, as summarized in Table I.

CONCLUSIONS

Random dopant distribution (RDD) induced σV_t for 20nm gate has been experimentally extracted and in good agreement with newly developed 3D discrete-dopant characterization. Average 40 dopants randomly distributed in the channel region give rise to $\sigma V_{t,RDD}$ of 40mV. The developed scheme outlooks that 7 dopants under 15nm gate at 3σ edge will occur and 8Å EOT in addition to work-function-modulated metal gate can suppress the increase of the $\sigma V_{t,RDD}$ for realizing manufacture with such gate length scaling.

Acknowledgements

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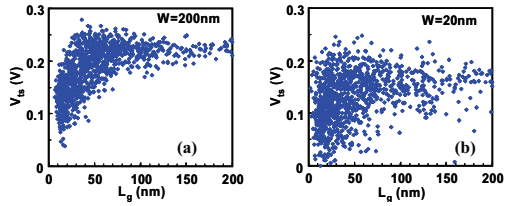


Fig. 1 Experimental saturation threshold voltage, V_{ts}, of NMOS transistors with L_g down to 20nm for (a) width=200nm and (b) width=20nm at V_d=1.0V.

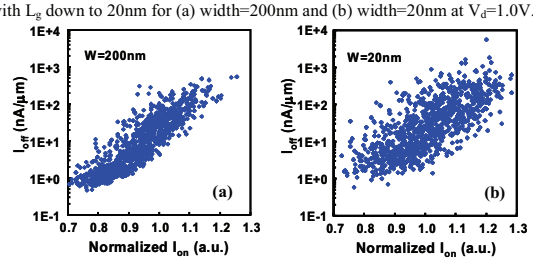
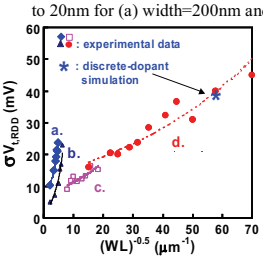


Fig. 2 Experimental I_{on}-I_{off} characteristics of NMOS transistors with L_g down to 20nm for (a) width=200nm and (b) width=20nm at V_d=1.0V.



	EOT (Å)	Channel Doping (cm^{-3})	Nominal L_g (nm)	Width (nm)
a.	24	~1E18	55	1000
b.	18	~3E18	35	1000
c.	12	~5E18	20	200
d.	12	~5E18	20	20

Fig. 3 Experimentally extracted $\sigma V_{t,RDD}$ (random dopant distribution), and discrete-dopant simulation (*, L_g =W=20nm, EOT=12Å) for various devices with nominal L_g from 55nm down to 20nm.

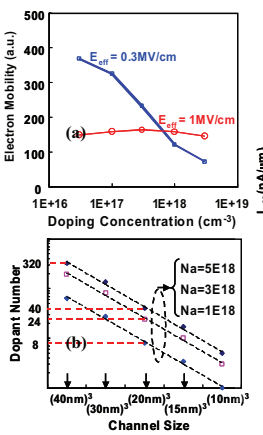


Fig. 4 (a) Extracted non-strain mobility versus doping concentration at 0.3 and 1 MV/cm vertical field, and (b) scaling of average channel dopant numbers versus channel size.

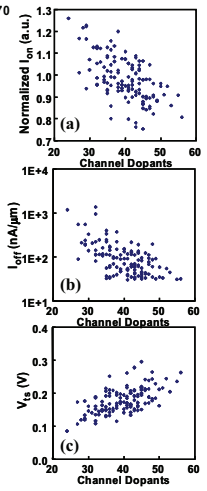


Fig. 6 Distributions of (a) I_{on}, (b) I_{off}, and (c) V_{ts} versus channel dopants for the 125 discrete-dopant 20nm-gate transistors (L_g=W=20nm) shown in Fig. 5(e).

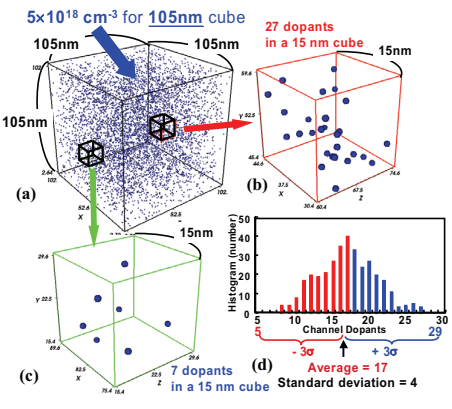


Fig. 8 5×10^{18} cm^{-3} doped $(105nm)^3$ cube, (a), with 343 sub-cubes of $(15nm)^3$. Dopants inside the sub-cubes are ranged from 7, (c), to 27, (b), with average number of 17 and one standard deviation of 4, (d).

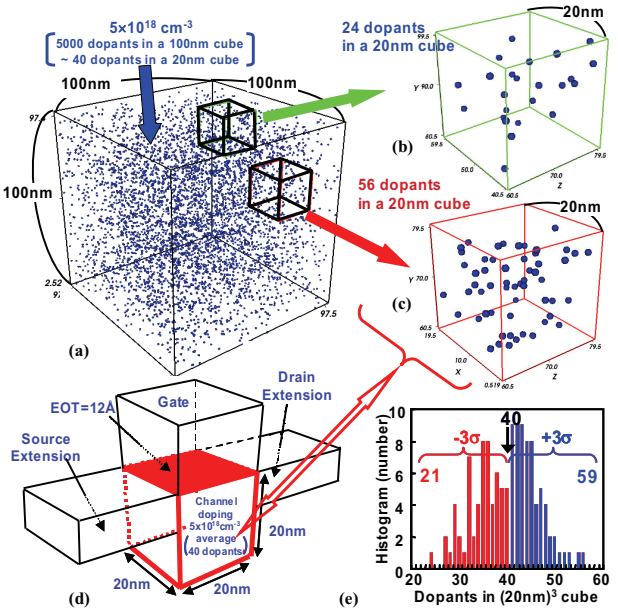


Fig. 5 (a) Discrete dopants randomly distributed in $(100nm)^3$ cube with average concentration of $5\times10^{18}cm^{-3}$. There will be 5000 dopants within the $(100nm)^3$ cube, but dopants vary from 24 to 56 (average number is 40) within its 125 sub-cubes of $(20nm)^3$, ((b), (c), and (e)). These 125 sub-cubes are then equivalently mapped into channel region for dopant position/number-sensitive simulation ((d)). In principle, device simulation with the 125 channel structures almost covers ±3σ cases ((e)), and thus will be fairly meaningful to reflect statistic randomness of dopant number/position.

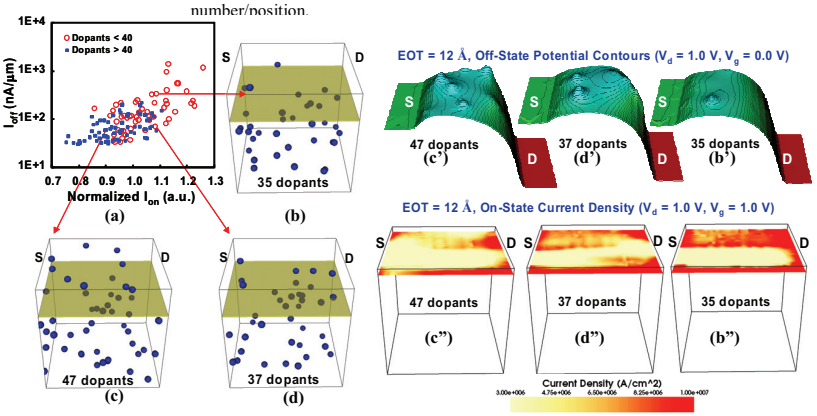


Fig. 7 (a) I_{on}-I_{off} characteristics of the 125 discrete-dopant 20nm-gate transistors (L_g=W=20nm). (b) and (d) represent two cases of channel doping with similar I_{on} but different I_{off}; (c) and (d) represent two cases of channel doping with similar I_{off} but different I_{on}. The corresponding off-state potential contours and on-state current density of (b), (c), and (d) are shown in (b'), (c'), (d') and (b"), (c"), (d"), respectively. All cross-sectional figures of off-state potential contours and on-state current density distributions are extracted at 1nm below 12Å EOT gate oxide.

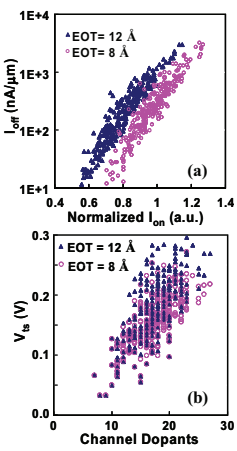


Fig. 9 (a) I_{on}-I_{off} characteristics and (b) V_{ts} versus channel dopants of discrete doped 15nm-gates with EOT=12Å (solid triangle) and 8Å (open circle). Gate work function is 4.22eV in the simulation.

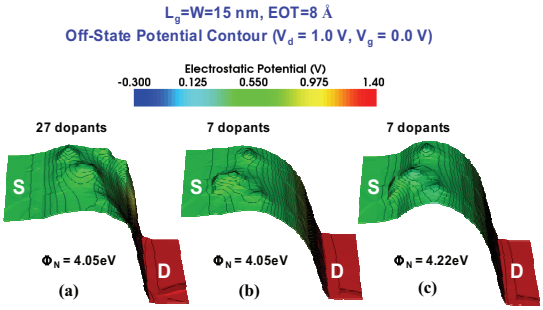


Fig. 10 Cross-sectional off-state electrostatic potential contours of two extreme cases in 15nm channels (EOT=8Å, Fig. 8 (b) and (c)) with (a) 27 dopants/Φ_N=4.05eV, (b) 7 dopants /Φ_N=4.05eV, and (c) 7 dopants/Φ_N= 4.22eV; all at 1nm below gate oxide.

Table I Summary of discrete dopant fluctuated 20nm/15nm-gate planar CMOS transistors.

L_g	Width	Data Source	Gate Work Function	Channel Doping (cm^{-3})	EOT	$\sigma V_{t,RDD}$
20nm	200nm	experimental	band-edge	5E+18	12Å	17mV
	20nm	experimental		5E+18	12Å	40mV
	20nm	discrete simulation		5E+18	12Å	39mV
15nm	15nm	discrete simulation	Φ_N = 4.22eV	5E+18	12Å	54mV
	15nm	discrete simulation	Φ_P = 4.98eV	5E+18	8Å	41mV