ESD Failure Mechanisms of Analog I/O Cells in 0.18-μm CMOS Technology

Ming-Dou Ker, *Senior Member, IEEE*, Shih-Hung Chen, and Che-Hao Chuang

***Abstract*—Different electrostatic discharge (ESD) protection schemes have been investigated to find the optimal ESD protection design for an analog input/output (I/O) buffer in 0.18-μm 1.8- and 3.3-V CMOS technology. Three power-rail ESD clamp devices were used in power-rail ESD clamp circuits to compare the protection efficiency in analog I/O applications, namely: 1) gate-driven NMOS; 2) substrate-triggered field-oxide device, and 3) substrate-triggered NMOS with dummy gate. From the experimental results, the pure-diode ESD protection devices and the power-rail ESD clamp circuit with gate-driven NMOS are the suitable designs for the analog I/O buffer in the 0.18-μm CMOS process. Each ESD failure mechanism was inspected by scanning electron microscopy photograph in all the analog I/O pins. An unexpected failure mechanism was found in the analog I/O pins with pure-diode ESD protection design under ND-mode ESD stress. The parasitic n-p-n bipolar transistor between the ESD clamp device and the guard ring structure was triggered to discharge the ESD current and cause damage under ND-mode ESD stress.**

***Index Terms*—Analog I/O, electrostatic discharge (ESD), failure mechanism, input/output (I/O) cell, power-rail ESD clamp device.**

I. Introduction

IN DEEP submicrometer CMOS technology, electrostatic discharge (ESD) protection has been an important concern on the reliability of IC products [1]–[3]. Due to the low breakdown voltage (BV) of the thinner gate oxide, an efficient ESD protection circuit must be designed to clamp the overstress voltage across the gate oxide of internal circuits. A conventional ESD protection design for the digital input pin is shown in Fig. 1. The gate-grounded NMOS (GGNMOS) and the gate-VDD PMOS (GDPMOS) are often designed with a large device dimension and a wider drain-contact-to-polygate layout spacing to sustain the desired ESD level [4], [5]. The resistor R in the digital input ESD protection circuit is usually included to effectively protect the gate oxide of the input stage. However, the series resistance between the input pad and the input stage is forbidden for current-mode input signals or high-frequency applications. Furthermore, the series resistance and the large junction capacitance of ESD clamp devices cause a long resistance–capacitance (RC) delay to the input signals; therefore, such an ESD protection circuit is not suitable for analog pins [6].

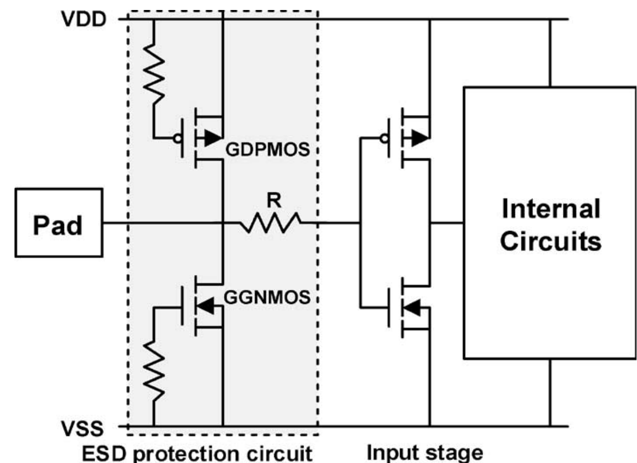

Fig. 1. Conventional ESD protection circuit for a digital input pin. GGNMOS and GDPMOS are designed with a large device dimension to sustain the requested ESD robustness.

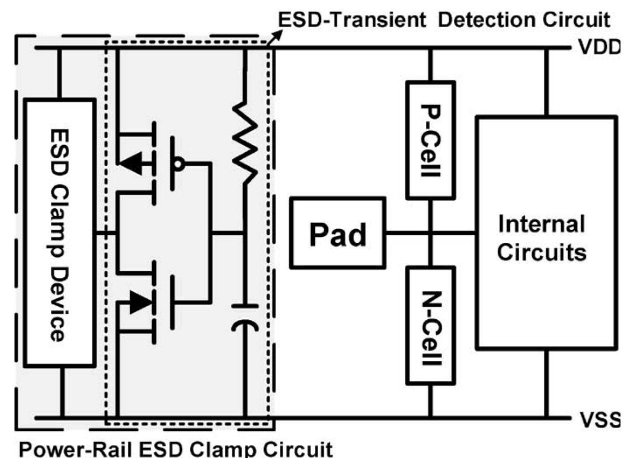

Fig. 2. ESD protection circuit for an analog I/O pin. The protection circuit includes the P-cell, N-cell, and power-rail ESD clamp circuit.

An ESD protection design for analog pins in 0.35-μm CMOS technology has been reported [6]. The basic ESD protection scheme for the analog input/output (I/O) pin is shown in Fig. 2. To reduce the input capacitance of the analog pin, N-cell and P-cell are designed with smaller device dimensions. However,

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TABLE I
DIFFERENT ESD PROTECTION DESIGNS FOR 1.8- AND 3.3-V ANALOG I/O PINS

Designs		N-cell & P-cell	Power-rail ESD clamp device
AIO_1	1.8-V	GGNMOS: W/L= 50/0.25 µm GDPMOS: W/L= 50/0.25 µm	Gate-driven NMOS [9] W/L= 290/0.25 µm
	3.3-V	GGNMOS: W/L= 50/0.44 µm GDPMOS: W/L= 50/0.44 µm	Gate-driven NMOS [9] W/L= 290/0.44 µm
AIO_2	1.8-V	GGNMOS: W/L= 50/0.25 µm GDPMOS: W/L= 50/0.25 µm	STFOD [13] W/L= 180/0.28 µm
	3.3-V	GGNMOS: W/L= 50/0.44 µm GDPMOS: W/L= 50/0.44 µm	STFOD [13] W/L= 180/0.28 µm
AIO_3	1.8-V	GGNMOS: W/L= 50/0.25 µm GDPMOS: W/L= 50/0.25 µm	STNMOS with dummy gate[14] W/L= 180/0.28 µm
	3.3-V	GGNMOS: W/L= 50/0.44 µm GDPMOS: W/L= 50/0.44 µm	STNMOS with dummy gate[14] W/L= 180/0.34 µm
AIO_4	1.8-V	Pure N+ diode: P/D= 50/0.44 µm Pure P+ diode: P/D= 50/0.44 µm	STFOD [13] W/L= 180/0.28 µm
	3.3-V	Pure N+ diode: P/D= 50/0.44 µm Pure P+ diode: P/D= 50/0.44 µm	STFOD [13] W/L= 180/0.28 µm

* P/D = Perimeter of the diode / Distance between anode and cathode of the diode.

such small devices cannot sustain a high enough ESD level, whereas the analog pin is zapped in the positive-to-VSS (PS-mode) or the negative-to-VDD (ND-mode) ESD stress (the devices operated in the breakdown condition). Therefore, an efficient power-rail ESD clamp circuit between VDD and VSS was co-constructed into the analog ESD protection circuit to improve the overall ESD level of the analog I/O pin.

In this paper, different ESD protection designs for the analog I/O pin were compared to find the optimal ESD protection circuit for the analog I/O pin in 0.18-μm 1.8-V/3.3-V CMOS technology. In addition, failure analyses on both 1.8- and 3.3-V analog I/O pins are presented after ND-mode and PS-mode ESD stresses [7]. In ESD protection designs with MOS devices, ESD robustness is dominated by the ESD levels of GGNMOS or GDPMOS under PS-mode or ND-mode ESD stresses. However, the failure mechanism is different from the ESD protection design with pure diodes under PS-mode or ND-mode ESD stresses. Besides, an unexpected failure mechanism has been found in the analog I/O pin with the pure-diode ESD protection circuit. The parasitic n-p-n bipolar transistor formed by the N+ diode and the N-well (NW) guard ring structure provides the ESD current path during ND-mode ESD stress, which causes a low ESD level to the analog I/O pin.

II. ESD PROTECTION SCHEMES FOR ANALOG I/O PIN

A. ESD Protection Circuit

Four ESD protection designs for analog I/O pins with 1.8- and 3.3-V devices in a 0.18-μm CMOS process are compared in this paper, as listed in Table I. GGNMOS and GDPMOS with channel widths of 50 μm are used for pad-to-VSS (N-cell) and pad-to-VDD (P-cell) ESD protection, respectively. The silicide-blocking widths on the drain side are 1.5 and 1.91 μm in all 1.8- and 3.3-V MOS protection devices, respectively. The source sides of all 1.8-V (3.3-V) MOS protection devices were formed

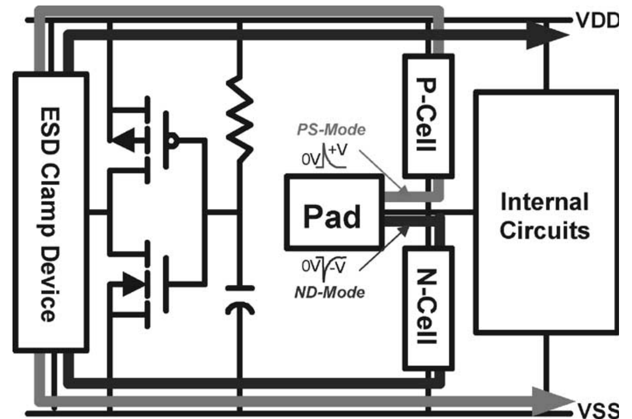


Fig. 3. Power-rail ESD clamp circuit can provide a low-impedance path between VDD and VSS to discharge the ESD current under the PS-mode and ND-mode ESD stresses. The ESD currents discharge through the P-cell (N-cell) and power-rail ESD clamp device during the PS-mode (ND-mode) ESD stress.

with silicidation. The human body model (HBM) ESD robustness of the standalone GGNMOS or GDPMOS with such small dimension (50 μm) is less than 500 V in the given 0.18-μm CMOS process when GGNMOS or GDPMOS is zapped in PS-mode or ND-mode ESD stresses (the devices in the drain breakdown condition). However, the 50-μm-wide GGNMOS or GDPMOS can sustain an HBM ESD level of 6000 V in the same 0.18-μm CMOS process when GGNMOS or GDPMOS is zapped in negative-to-VSS (NS-mode) or positive-to-VDD (PD-mode) ESD stresses (the devices operated in the drain diode forward-biased condition). To avoid GGNMOS and GDPMOS in the drain breakdown condition, an efficient power-rail ESD clamp circuit is constructed in analog I/O ESD protection circuits. In Fig. 2, the RC-based ESD-transient detection circuit [8], [9] is applied to trigger the ESD clamp device to provide a low-impedance path between VDD and VSS, whereas the pad is zapped in PS-mode or ND-mode ESD stresses.

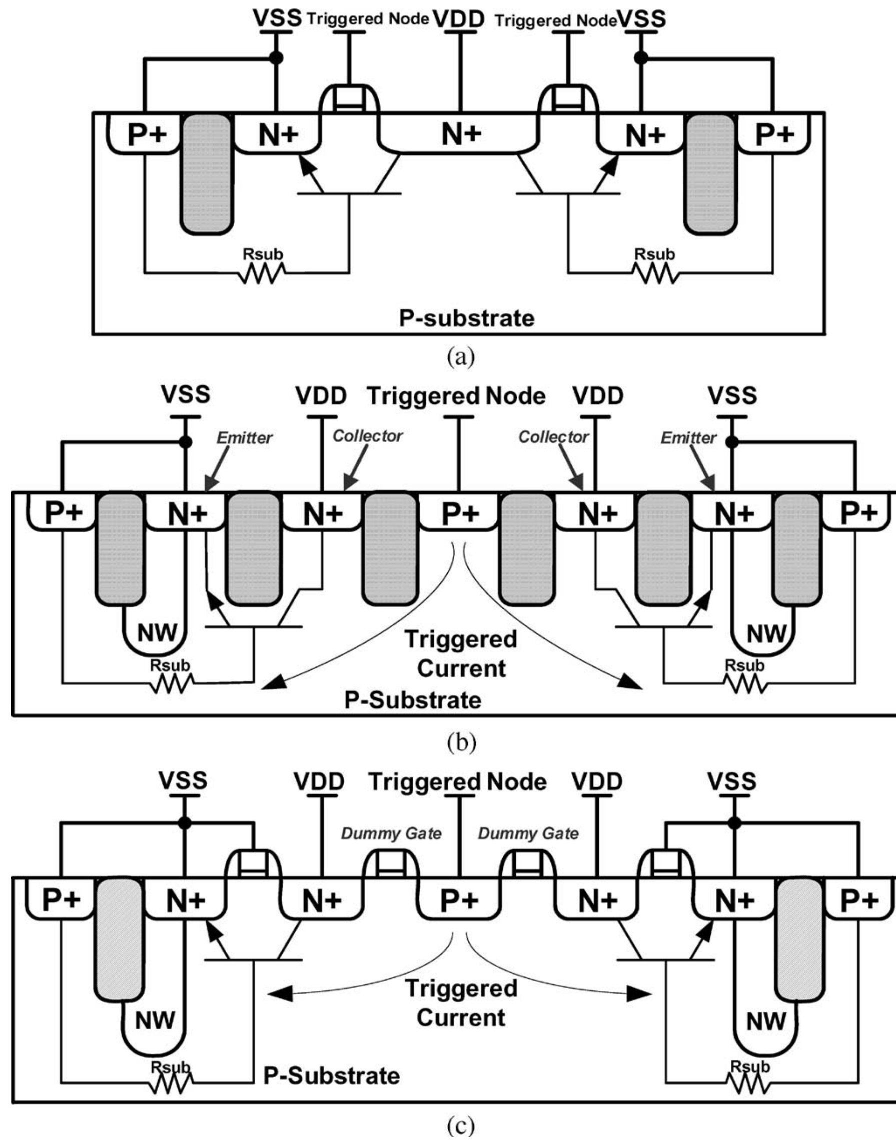


Fig. 4. Cross-sectional views of (a) gate-driven NMOS, (b) STFOD, and (c) STNMOS with dummy gate.

Because the power-rail ESD clamp device can be turned on under PS-mode or ND-mode ESD stresses, the ESD current is discharged through the forward-biased drain diode and the turned-on power-rail ESD clamp device, as illustrated in Fig. 3. The power-rail ESD clamp device is usually designed with a large device dimension to provide higher ESD robustness and lower impedance path between VDD and VSS to effectively discharge the ESD current under PS-mode or ND-mode ESD stresses. Because the ESD clamp device is added between VDD and VSS, the large parasitic junction capacitance of the ESD clamp device does not contribute to the analog pin. Therefore, this ESD protection design for the analog pin can sustain high ESD robustness but only with a low parasitic input capacitance.

In high-frequency analog circuit applications, the parasitic effects of ESD protection devices often play a critical factor to influence the circuit performance. Due to the smaller parasitic effect in the pure-diode structure, the ESD protection design with pure diodes in the input stage is more suitable than the ESD protection design with MOS devices in high-frequency circuit applications [10], [11]. In Table I, the pure-diode ESD protection design between the pad and VDD (VSS) is also designed to compare with the MOS protection circuit. The pure N+ diode and the pure P+ diode are constructed by the N+/P-well (PW) junction diode and the P+/NW junction diode, respectively. The pure-diode ESD protection designs are drawn with the same equivalent perimeters as the channel width of the MOS devices in the test chip. In Table I, "P/D" pertains to the perimeter (P) of the diode structures and the distance (D) between the N+ and the P+ diffusions in N+ diodes and between the P+ and the N+ diffusions in P+ diodes in pure-diode structures.

The turn-on efficiency of the ESD clamp devices with gate-driven and substrate-triggered designs had been studied in 0.35-μm CMOS technology [12]. In this paper, gate-driven NMOS [9], substrate-triggered field-oxide device (STFOD) [13], and substrate-triggered NMOS (STNMOS) with dummy gate [14] are used as power-rail ESD clamp devices to verify the utility for the analog I/O pins in 0.18-μm CMOS technology,

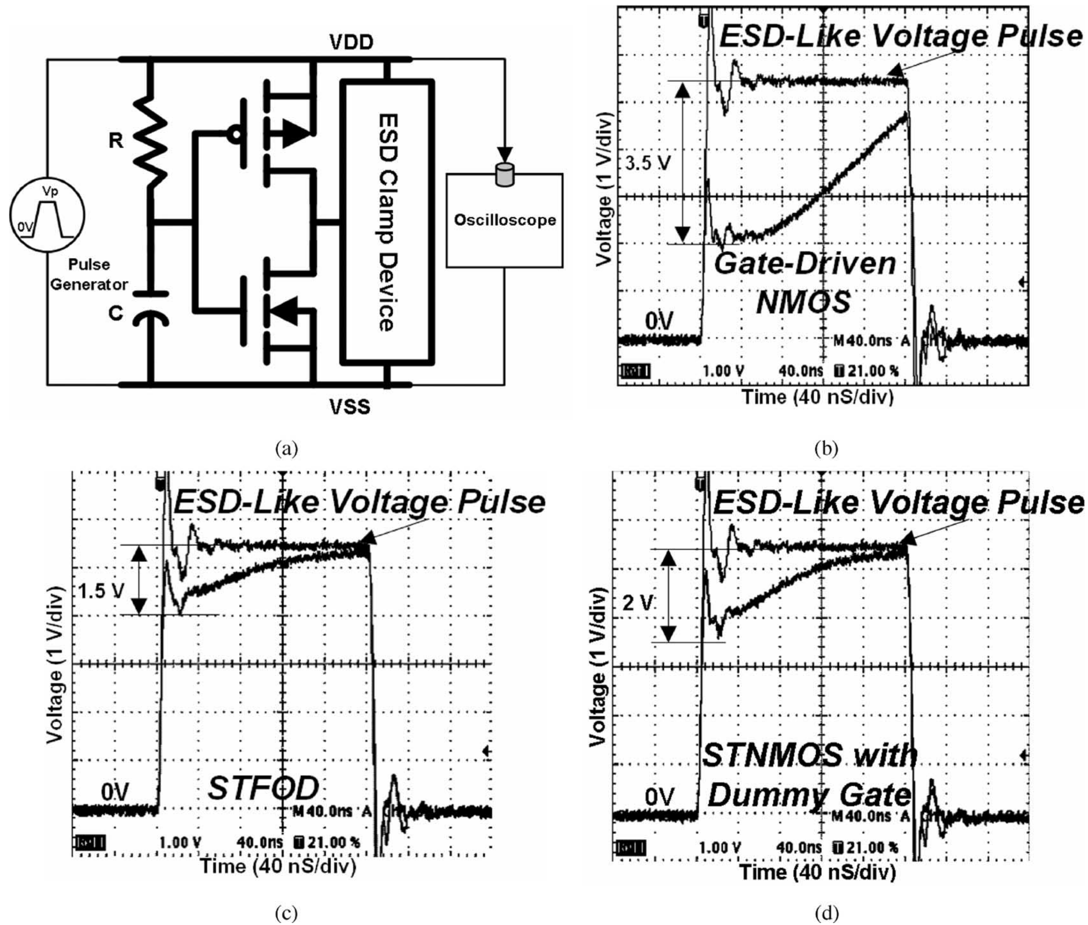


Fig. 5. (a) Experimental setup to measure the turn-on efficiency of power-rail ESD clamp circuits. Measured voltage waveforms of the 3.3-V analog I/O pins on the VDD node, which are clamped by (b) gate-driven NMOS, (c) STFOD, and (d) STNMOS with dummy gate, under ESD-like stress condition.

as shown in Table I. In Table I, "W/L" in STFOD pertains to the perimeter (W) of the parasitic n-p-n bipolar transistors in STFOD and the distance (L) between the collector and the emitter of the parasitic n-p-n bipolar transistors in STFOD. The STNMOS with dummy gate is a newly proposed power-rail ESD clamp device that has been drawn in the test chip and compared with the gate-driven NMOS and STFOD. The device structures of the gate-driven NMOS, STFOD, and STNMOS with dummy gate are shown in Fig. 4(a)–(c), respectively. In Fig. 4(c), the dummy gate is used to reduce the distance between the triggered node and the base of the parasitic n-p-n bipolar transistor in the NMOS structure. It can improve the turn-on efficiency of STNMOS by enhancing the triggered current to achieve the base region of the n-p-n bipolar transistor, as illustrated in Fig. 4(c). The silicide-blocking widths on the collector side are 1.5 and 1.5 μm in 1.8- and 3.3-V STFOD and STNMOS, respectively. Each analog I/O cell has been drawn in the same silicon area of an I/O cell with the power-rail ESD clamp device and ESD-transient detection circuit. Therefore, all analog I/O cells have the same cell height of 89 μm (excluding the bonding pad) and cell pitch of 65 μm. In addition, each analog I/O pin was connected to the input stage of an inverter in the silicon chip to evaluate the core-circuit protection efficiency in each ESD test condition. Due to the transient gate oxide BVs as a function of the physical gate oxide thickness, the transmission line pulse (TLP) measurement results of the transient gate oxide BVs are 10–12 and 16–18 V in the 1.8- and 3.3-V processes, respectively.

B. Turn-On Efficiency of Power-Rail ESD Clamp Circuit

Due to the difference in the rise time between the ESD voltage and the VDD power-on voltage, the power-rail ESD clamp circuit provides a low-impedance path between the VDD and VSS power lines during the ESD-stress condition, but it becomes an open circuit between the power lines in the VDD power-on condition. To meet these requirements, the RC time constant of the ESD-transient detection circuit is designed to be about 0.1–1 μs to achieve the desired operations. To verify the aforementioned ESD-transient detection function, an experimental setup is shown in Fig. 5(a) [9]. To simulate the HBM ESD pulse, a voltage pulse with a rise time of about 5 ns is generated from a pulse generator (HP8110A) and applied to the VDD power line with the VSS grounded. The sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD clamp device to degrade the voltage waveform on the VDD power line.

The measured voltage waveforms, which are clamped by the gate-driven NMOS, the STFOD, and the STNMOS with dummy gate, under the ESD-like voltage stress of the 3.3- and 1.8-V analog I/O pins on the VDD power line are shown in

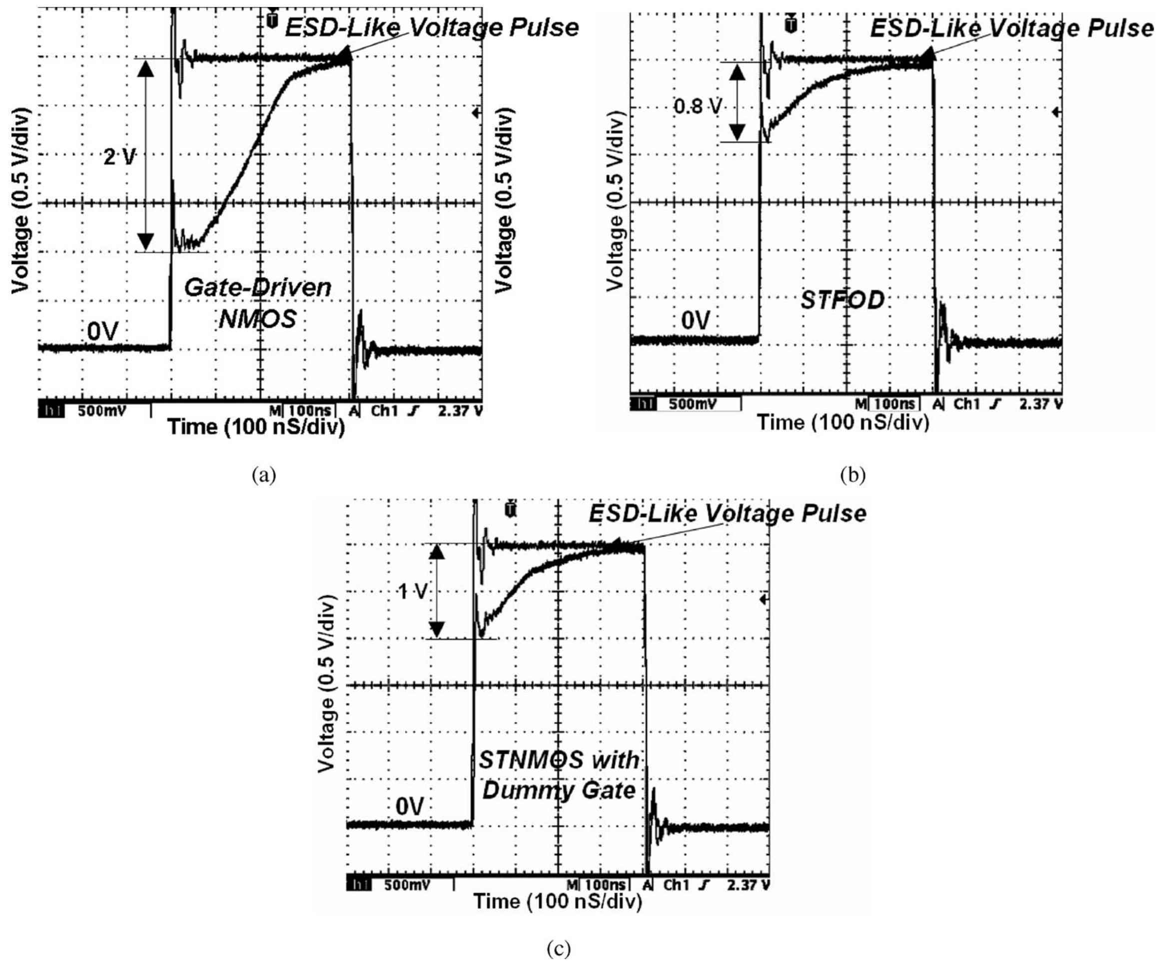


Fig. 6. Measured voltage waveforms of the 1.8-V analog I/O pins on the VDD node, which are clamped by (a) gate-driven NMOS, (b) STFOD, and (c) STNMOS with dummy gate, under ESD-like stress condition.

TABLE II
TRANSIENT CHARACTERISTICS OF DIFFERENT ESD PROTECTION DEVICES

N-cell and P-cell		MOS Transistors		Diode Devices	
		GGNMOS	GDNMOS	N+ Diode	P+ Diode
Junction Breakdown (Reverse-Biased Condition)	1.8-V	5~6 V	6 V	11 V	10 V
	3.3-V	7.5 V	7.5 V	16 V	16 V
Turn-On Resistance (Forward-Biased Condition)	1.8-V	~ 2.67 Ω		~ 2.24 Ω	
	3.3-V	~ 2.7 Ω		~ 2.19 Ω	

Power-Rail ESD Clamp Circuits		Gate-Driven NMOS	STFOD	STNMOS
Trigger Voltage	1.8-V	5 V	6 V	4 V
	3.3-V	7.5 V	7.3 V	5 V
Holding Voltage	1.8-V	5 V	6 V	4 V
	3.3-V	6 V	7.3 V	5 V
VDD-to-VSS Turn-On Resistance	1.8-V	~ 1.78 Ω	~ 1.85 Ω	~ 2.52 Ω
	3.3-V	~ 1.65 Ω	~ 2.47 Ω	~ 2.25 Ω

Figs. 5(b)–(d) and 6(a)–(c), respectively. The maximum voltage degradations of the gate-driven NMOS, the STFOD, and the STNMOS with dummy gate are 2, 0.8, and 1 V, respectively, in 1.8-V analog I/O pins, and 3.5, 1.5, and 2 V, respectively, in 3.3-V analog I/O pins. According to the measured results, the gate-driven NMOS has significant voltage degradation to effectively clamp the ESD-like voltage pulse in both 3.3- and 1.8-V analog I/O pins in the given 0.18-μm CMOS process.

TABLE III
HBM ESD ROBUSTNESS OF 1.8-V ANALOG I/O PINS

Designs	PS-mode	NS-mode	PD-mode	ND-mode
AIO_1	0.5 kV	-3.5 kV	7.5 kV	-2.5 kV
AIO_2	< 0.5 kV	-3.5 kV	7.5 kV	-1.0 kV
AIO_3	0.5 kV	-3.5 kV	7.5 kV	-2.5 kV
AIO_4	3.0 kV	-5.5 kV	6.0 kV	-2.0 kV

TABLE IV
HBM ESD ROBUSTNESS OF 3.3-V ANALOG I/O PINS

Designs	PS-mode	NS-mode	PD-mode	ND-mode
AIO_1	1.5 kV	-3.5 kV	7.5 kV	-2.0 kV
AIO_2	< 0.5 kV	-3.5 kV	7.5 kV	-0.5 kV
AIO_3	1.5 kV	-3.5 kV	7.5 kV	-2.0 kV
AIO_4	2.0 kV	-5.5 kV	6.5 kV	-1.5 kV

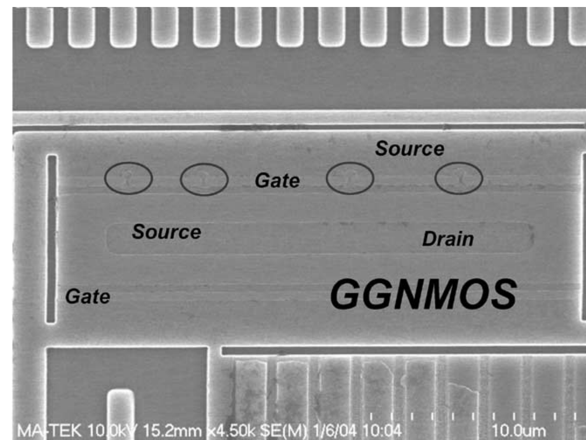
TABLE V
FAILURES ON THE 1.8- AND 3.3-V ANALOG I/O PINS AFTER PS-MODE ESD STRESS

1.8-V Designs	Shorting Path	3.3-V Designs	Shorting Path
AIO_1	Pad-to-VSS	AIO_1	Pad-to-VSS
AIO_2	Pad-to-VSS	AIO_2	Pad-to-VSS
AIO_3	Pad-to-VSS	AIO_3	Pad-to-VSS
AIO_4	VDD-to-VSS	AIO_4	VDD-to-VSS

Therefore, the gate-driven NMOS could be more suitable in the power-rail ESD clamp design for 1.8- and 3.3-V analog I/O pins in the subquarter micrometer CMOS technology, which has a shallow trench isolation (STI) structure. On the other hand, the difference of the maximum voltage drops in STFOD and STNMOS with dummy gate is caused by the difference of the base width of the parasitic lateral n-p-n bipolar transistors in the ESD clamp device. The current gain (β) of the STNMOS with dummy gate can be increased by reducing the distance from the two separated N+ regions. The ESD robustness of the power-rail ESD clamp circuits with the gate-driven NMOS, the STFOD, and the STNMOS with dummy gate are 5.5, 3.0, and 3.0 kV, respectively, in the 1.8-V process (which are 2.5, 1.5, and 2.0 kV, respectively, in the 3.3-V process). The transient characteristics of the power-rail ESD clamp circuits, such as trigger voltage and turn-on resistance, are also shown in Table II. According to the measured results, the power-rail ESD clamp circuits with gate-driven NMOS have the lowest turn-on resistance and fastest turn-on speed, therefore providing the best turn-on efficiency and ESD robustness in the subquarter micrometer CMOS technology, which has an STI structure.

TABLE VI
FAILURES ON THE 1.8- AND 3.3-V ANALOG I/O PINS AFTER ND-MODE ESD STRESS

1.8-V Designs	Shorting Path	3.3-V Designs	Shorting Path
AIO_1	Pad-to-VDD	AIO_1	Pad-to-VDD
AIO_2	Pad-to-VDD	AIO_2	Pad-to-VDD
AIO_3	Pad-to-VDD	AIO_3	Pad-to-VDD
AIO_4	VDD-to-VSS	AIO_4	VDD-to-VSS



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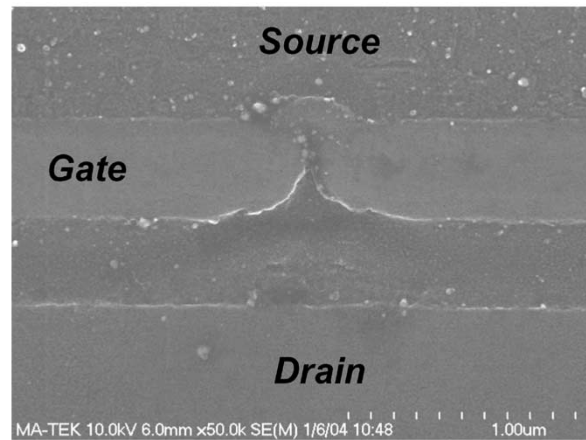
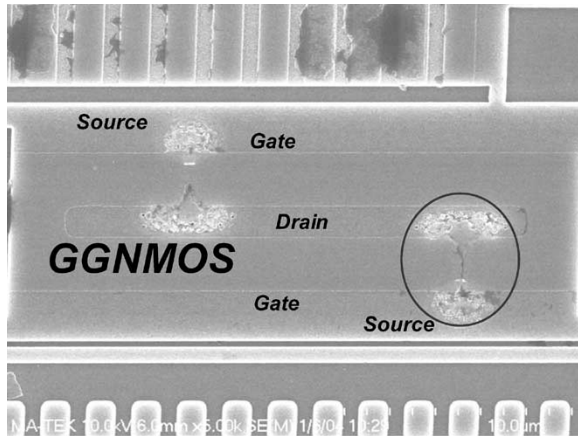


(b)

Fig. 7. (a) Failure spot located at the GGNMOS in 1.8-V analog I/O pins with MOS ESD protection design of AIO_2 after a 0.5-kV PS-mode ESD stress. (b) Zoomed-in view of the failure spot.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The device characteristics, such as junction BVs (reverse-biased condition) and turn-on resistances (forward-biased condition) of GGNMOS and GDPMOS in 1.8- and 3.3-V devices, are shown in Table II. In 1.8- and 3.3-V devices, the junction BVs of pure-diode structures are higher than those of the MOS transistors. The turn-on resistances of the pure-diode structures and MOS transistors in N-cells and P-cells were measured in the ESD currents discharged by the forward-biased pure-diode structures or forward-biased drain diodes. However, the slightly



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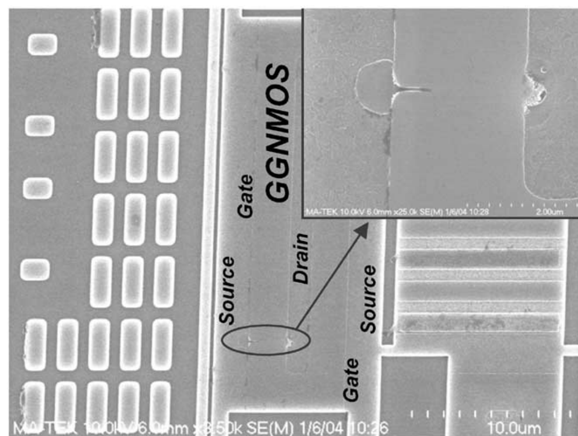
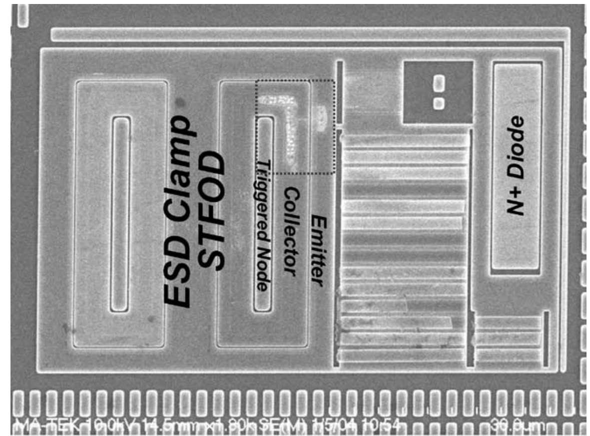


(b)

Fig. 8. (a) Failure spot located at the GGNMOS in 3.3-V analog I/O pins with MOS ESD protection design of AIO_3 after a 2.0-kV PS-mode ESD stress. (b) Failure spot located at the GGNMOS in 3.3-V analog I/O pins with MOS ESD protection design of AIO_2 after a 0.5-kV PS-mode ESD stress.



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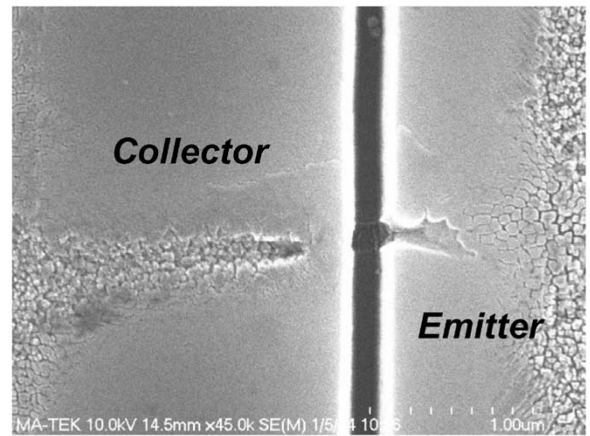


(b)

Fig. 9. (a) Failure spot located at the ESD clamp FOD in 1.8-V analog I/O pins with pure-diode ESD protection design of AIO_4 after a 3.5-kV PS-mode ESD stress. (b) Zoomed-in view of the failure spot.

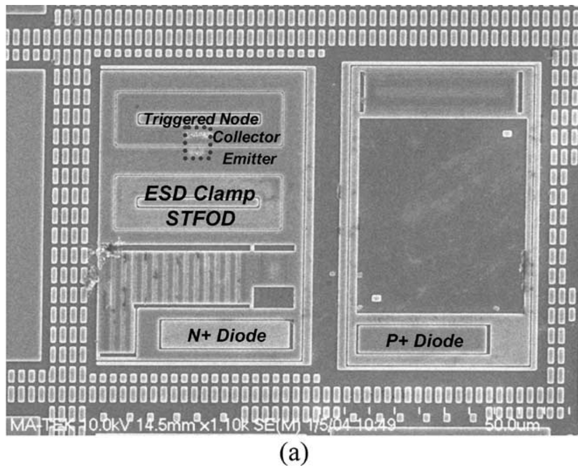
lower turn-on resistances of the pure-diode structures can be attributed to the fully silicided process in N+ (P+) diffusions and the P+ (N+) diffusions in pure N+ diodes (P+ diodes).

A. HBM ESD Robustness

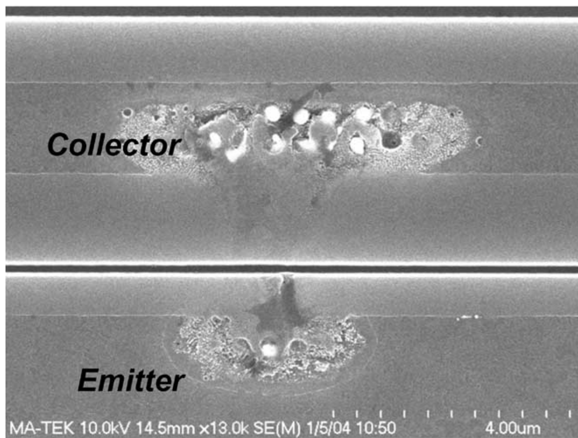
The HBM ESD robustness of the 1.8- and 3.3-V analog I/O pins are shown in Tables III and IV, respectively. In 1.8-V analog I/O pins, the ESD levels of AIO_1, AIO_2, AIO_3, and AIO_4 are 0.5, smaller than 0.5, 0.5, and 3.0 kV, respectively, in PS-mode ESD stress. The PS-mode ESD levels of AIO_1, AIO_2, AIO_3, and AIO_4 in 3.3-V analog I/O pins are 1.5, smaller than 0.5, 1.5, and 2.0 kV, respectively. Analog I/O pins with pure-diode protection have higher ESD level among all the ESD test modes. In 1.8-V analog I/O pins, the ESD levels of the analog I/O pins with the MOS devices are much weaker than that with the diode devices during a PS-mode ESD stress. On the other hand, the ND-mode ESD levels do not achieve the general specification (2 kV) in AIO_2 of 1.8-V analog I/O pins, and in AIO_2 and AIO_4 of 3.3-V analog I/O pins. The ESD robustness of 1.8- and 3.3-V analog I/O pins with MOS protection circuits are dominated by PS-mode ESD levels, but analog pins with pure-diode protection circuits are dominated by ND-mode ESD levels. The difference in ESD robustness among analog I/O pins was inspected by failure analysis after the PS-mode and ND-mode ESD stresses.

B. Failure Analysis

The current–voltage $(I–V)$ curves of the 3.3- and 1.8-V analog I/O pins were measured to identify which device or junction was damaged after the PS-mode and ND-mode ESD stresses. The results are listed in Tables V and VI. The analog pins with GGNMOS and GDPMOS were shorted to ground after PS-mode ESD stress. The 1.8- and 3.3-V GGNMOS devices of AIO_1, AIO_2, and AIO_3 were damaged to cause the short circuit between the analog pin and VSS. The failure spot of 1.8-V analog I/O pins after PS-mode ESD stress is shown in Fig. 7(a) and (b). After 0.5- or 1-kV ESD stresses, AIO_1, AIO_2, and AIO_3 show local damage in GGNMOS. The local damage is located under the polygate oxide to cause the short circuit between the analog pin and VSS, as shown in Fig. 7. On the other hand, the failure spots of the 3.3-V analog I/O pins after PS-mode ESD stresses are shown in Fig. 8(a) and (b). In Fig. 8(a), the huge ESD current discharged through the parasitic n-p-n bipolar transistor of the GGNMOS of AIO_3

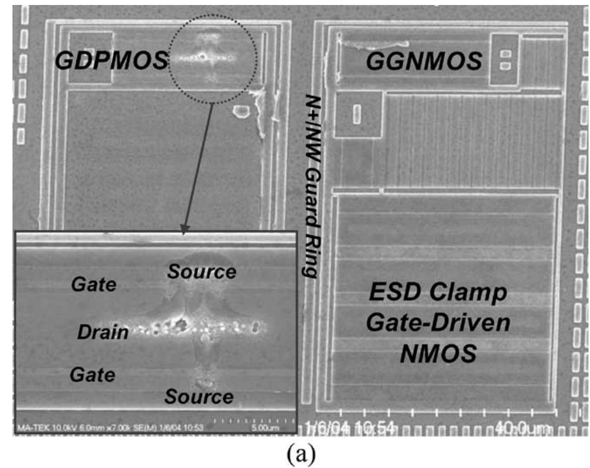


(a)

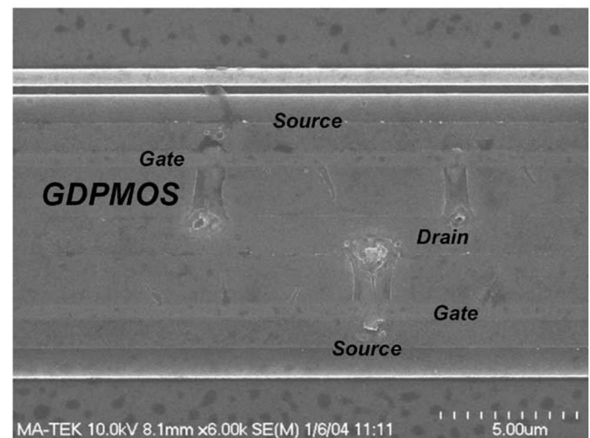


(b)

Fig. 10. (a) Failure spot located at the ESD clamp FOD in 3.3-V analog I/O pins with pure-diode ESD protection design of AIO_4 after a 2.5-kV PS-mode ESD stress. (b) Zoomed-in view of the failure spot.



(a)



(b)

Fig. 11. (a) Failure spot located at the GDPMOS in 1.8-V analog I/O pins with MOS ESD protection design of AIO_1 after a 3.0-kV ND-mode ESD stress. (b) Failure spot located at the GDPMOS in 1.8-V analog I/O pins with MOS ESD protection design of AIO_2 after a 1.5-kV ND-mode ESD stress.

to violently destroy the silicon substrate after a 2-kV PS-mode ESD stress. The GGNMOS of AIO_2 shows only a slight damage after a 0.5-kV PS-mode ESD stress, as shown in Fig. 8(b). Due to the difference in the turned-on efficiency of the power-rail ESD clamp circuit of AIO_1, AIO_2, and AIO_3, the distributions of the ESD current are also different in AIO_1, AIO_2, and AIO_3 of the 3.3-V analog I/O pins. In AIO_1 and AIO_3, the ESD current majority discharged through the drain diode of the P-cell and the turned-on power-rail ESD clamp circuit to the grounded VSS under the PS-mode ESD stress. The parasitic n-p-n bipolar transistor of the small GGNMOS would be turned on by the increasing voltage drop between the analog pin and VSS and destroyed to cause serious damages under higher ESD stresses. However, the small GGNMOS of AIO_2 was unexpectedly turned on to discharge the ESD current and cause slight damage under a lower ESD level because the ineffective power-rail ESD clamp circuit did not provide the low-impedance discharging path. In addition, due to the lower drain-breakdown voltage and thinner gate oxide in the 1.8-V analog pins, the GGNMOS would be damaged to cause a regional failure spot under about 0.5- to 1-kV PS-mode ESD stress, as presented in Fig. 7(a) and (b).

However, the measured results of the analog pins with pure diodes to implement N-cell and P-cell are obviously different. The I–V curves show the VDD shorting to ground after the PS-mode ESD stress. The power-rail ESD clamp devices are damaged to cause the short circuit between VDD and VSS in 1.8- and 3.3-V analog I/O pins, as shown in Figs. 9(a) and (b) and 10(a) and (b), respectively. In these scanning electron microscopy (SEM) photographs, the failure spots are located at the parasitic n-p-n transistors of the STFODs. The clearly destroyed path occurred between the collector and the emitter of the parasitic n-p-n bipolar transistor in the STFOD, as shown in Figs. 9(b) and 10(b). Therefore, the power-rail ESD clamp device will dominate the ESD levels of these analog I/O pins with the pure-diode structure under the PS-mode ESD stress. The failures on the analog I/O pins after PS-mode ESD stress are summarized in Table V.

On the other hand, the failures on the analog I/O pins after ND-mode ESD stress are listed in Table VI. After ND-mode ESD stress, GDPMOS is damaged in the analog pins of AIO_1, AIO_2, or AIO_3 in 1.8- and 3.3-V applications, as illustrated in Fig. 11(a) and (b). The parasitic p-n-p bipolar transistor of GDPMOS was also turned on by the increased voltage drop between the VDD and the analog pin to seriously destroy

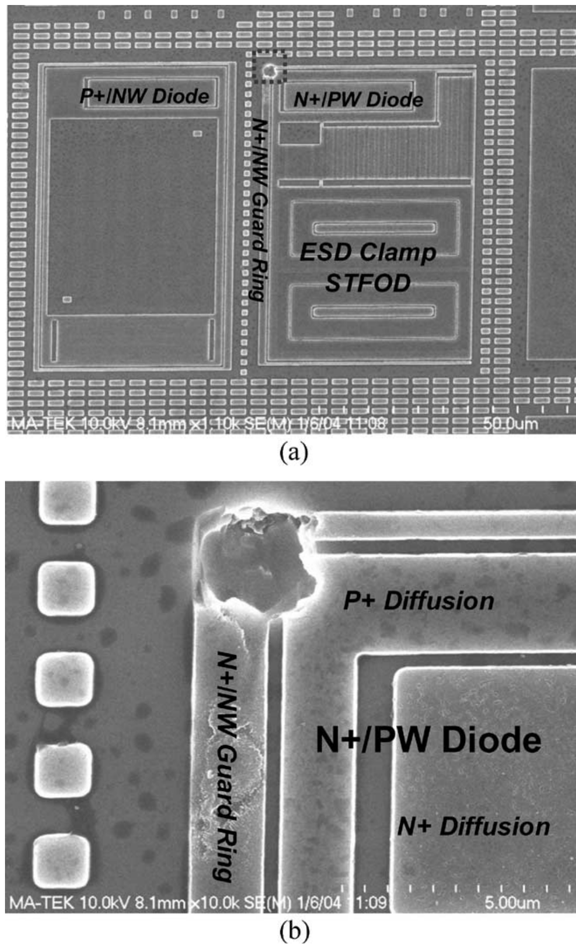


Fig. 12. (a) After a 2.5-kV ND-mode ESD stress, the failure spot is located at the guard ring in AIO_4 of the 1.8-V process. (b) Zoomed-in view of the failure spot at the guard ring corner.

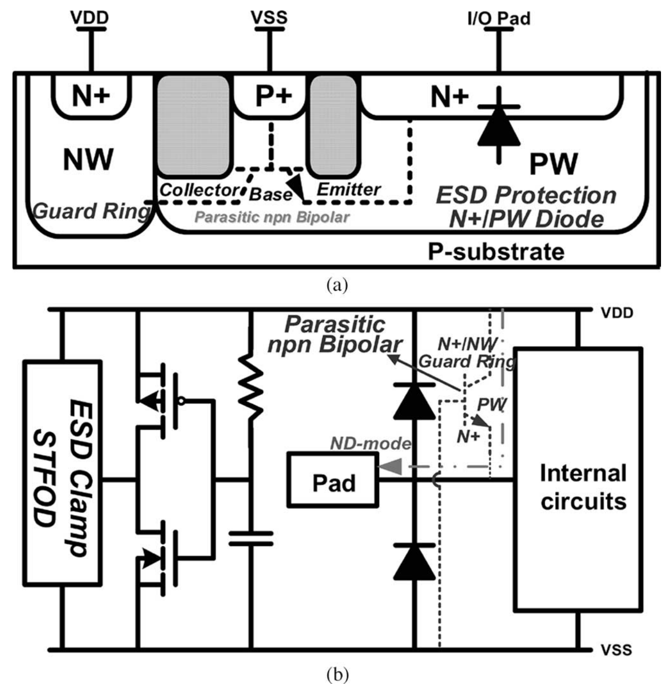


Fig. 13. (a) Parasitic n-p-n bipolar transistor constructed between the N+/PW diode and the N+/NW guard ring. (b) ESD current discharged through the parasitic n-p-n bipolar transistor to the grounded VDD during ND-mode ESD stress causes unexpected ESD failure.

under a higher ND-mode ESD stress in AIO_1 and AIO_3 of 1.8- and 3.3-V analog I/O pins. However, the AIO_2 with a lower ESD level should also be attributed to the ineffective power-rail ESD clamp circuit. According to the turn-on verification on the power-rail ESD clamp circuit, STFOD could not rapidly discharge the ESD current to result in GDPMOS conducting the huge current through the drain breakdown condition under lower ESD stresses, as shown in Fig. 11(b). Therefore, the ESD levels of the analog I/O pins with MOS ESD protection design are dominated by the ESD robustness of GGNMOS and GDPMOS under PS-mode and ND-mode ESD stresses, respectively.

C. Unexpected Failure Spot in ND-Mode ESD Stress

In Tables III and IV, the lowest ESD robustness in both AIO_4 designs is dominated by the ND-mode ESD stress. To identify the failure location for further improving its ESD level, the sample of AIO_4 after the ND-mode ESD failure was delayered. The unexpected ESD failure was located at the guard ring structure of the analog I/O pin with pure-diode ESD protection design after the ND-mode ESD stress, as shown in Fig. 12(a) and (b). The interaction between the N+/PW diode and the N+/NW guard ring was determined to be the cause of the failure under ND-mode ESD stress, as shown in Fig. 12(b). To overcome latchup issues, ESD protection devices are often surrounded by guard rings, which are commonly connected to VDD or VSS. These guard rings could interact with ESD protection devices to degrade the ESD robustness of protection circuits [15]. As shown in Fig. 3, the ND-mode ESD current should be discharged through the forward-biased diode between the I/O pad and VSS, and the power-rail ESD clamp device and the grounded VDD. However, the parasitic n-p-n bipolar transistor, which was formed between the N+/PW diode and the N+/NW guard ring, was triggered on to form a direct discharging path between the I/O pad and the grounded VDD during ND-mode ESD stress, as the dashed lines illustrated in Fig. 13(a). Fig. 13(b) explains that the ND-mode ESD current is discharged through this parasitic bipolar transistor to cause damage at the corner of the guard ring due to the localized heat. In addition, the current gain (β) and the avalanche multiplication factor of the parasitic bipolar transistor are important parameters contributing to this failure mechanism. To overcome this failure, the spacing between the N+/NW guard ring and the N+/PW diode should be increased to eliminate the parasitic n-p-n bipolar junction transistor (BJT) effect. On the other hand, replacing the power-rail ESD clamp circuit with higher turn-on efficiency can avoid the turn-on of the parasitic n-p-n BJT to degrade the ESD robustness under ND-mode ESD stress. In addition, the power-rail ESD clamp circuit with high turn-on efficiency can also improve the ESD robustness of the PS-mode ESD stress by providing an efficient and low-impedance discharging path between VDD and VSS.

A successful modification with the optimal power-rail ESD clamp circuit has been practically verified in a 0.13-μm CMOS process to achieve an HBM ESD level of 7.0 kV for the analog I/O cell.

IV. Conclusion

Different ESD protection schemes for analog I/O cells have been investigated to find the optimal analog ESD protection design for deep submicrometer CMOS technology. According to the experimental results, GGNMOS was not a suitable ESD protection device for analog I/O cells in a deep submicrometer CMOS process, such as 0.18 μm and below. The pure-diode ESD protection device between the pad and VDD (VSS) would be an optimal design for the analog I/O pins. In addition, the gate-driven NMOS for power-rail ESD clamp circuit also performs a higher ESD robustness for analog I/O pins in deep submicrometer CMOS technology with STI structure. Finally, layout optimization with a wider spacing between N+/PW diode and N+/NW guard ring, as well as improvement on the power-rail ESD clamp circuit with higher turn-on efficiency, should be used to avoid the unexpected ESD failure under ND-mode ESD stress in such analog I/O cells.

References

[1] S. Voldman, "The state of the art of electrostatic discharge protection: Physics, technology, circuits, design, simulation, and scaling," *IEEE J. Solid-State Circuits*, vol. 34, no. 9, pp. 1272–1282, Sep. 1999.

[2] C. Duvvury and A. Amerasekera, "ESD: A pervasive reliability concern for IC technologies," *Proc. IEEE*, vol. 81, no. 5, pp. 690–702, May 1993.

[3] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *Proc. EOS/ESD*, 1994, pp. 237–245.

[4] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *Proc. EOS/ESD*, 1990, pp. 206–213.

[5] R. N. Rountree, "ESD protection for submicron CMOS circuits: Issues and solutions," in *IEDM Tech. Dig.*, 1988, pp. 580–583.

[6] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD protection design on analog pin with very low input capacitance for high-frequency or current-mode applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1194–1199, Aug. 2000.

[7] S.-H. Chen, M.-D. Ker, and C.-H. Chuang, "A new failure mechanism of analog I/O cell under ND-mode ESD stress in deep-submicron CMOS technology," in *Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits*, 2005, pp. 209–212.

[8] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. EOS/ESD*, 1993, pp. 233–237.

[9] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[10] C. Ito, K. Banerjee, and R. W. Dutton, "Analysis and design of distributed ESD protection circuits for high-speed mixed-signal and RF ICs," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1444–1454, Aug. 2002.

[11] M.-D. Ker and B.-J. Kuo, "Optimization of broadband RF performance and ESD robustness by π-model distributed ESD protection scheme," in *Proc. EOS/ESD*, 2004, pp. 32–39.

[12] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS device," *IEEE Trans. Device Mater. Rel.*, vol. 1, no. 4, pp. 190–203, Dec. 2001.

[13] M.-D. Ker, "Area-efficient VDD-to-VSS ESD protection circuit," U.S. Patent 5 744 842, Apr. 28, 1998.

[14] M.-D. Ker, C.-H. Chuang, and H.-C. Jiang, "ESD protection circuit sustaining high ESD stress," U.S. Patent 6 690 067, Feb. 10, 2004.

[15] D. Tremouilles, G. Bertrand, M. Bafleur, F. Beaudoin, P. Prerdu, N. Guitard, and L. Lescouzeres, "TCAD and SPICE modeling help solve ESD protection issues in analog CMOS technology," *Microelectron. Reliab.*, vol. 43, no. 1, pp. 71–79, Jan. 2003.

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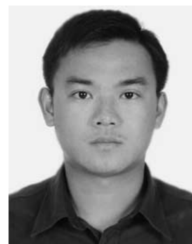

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