Impact of STI on the Reliability of Narrow-Width pMOSFETs With Advanced ALD N/O Gate Stack

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***Abstract*—For the first time, a shallow trench isolation (STI)-induced enhanced degradation in pMOSFETs for ultrathin gate oxide devices has been observed. The I_D degradation is enhanced as a reduction in the gate width and the hot carrier (HC) or negative bias temperature instability (NBTI) effect. Extensive studies have been compared for atomic layer deposition (ALD)-grown and plasma-treated oxide pMOSFETs. Different temperature dependences were observed. At room temperature, hole trap is dominant for the device degradation, in which hole-trap-induced V_T is significant, whereas at high temperature under NBTI stress, interface trap becomes more significant, which dominates the device I_D degradation. In addition, the V_T rolloff can be modeled as a width narrowing effect specifically for STI. More importantly, the NBTI-induced interface/oxide traps are strongly related to the hydrogen and N_2 content in the gate oxide formation process. The interface trap generation is suppressed efficiently using the ALD-grown gate oxide. These results provide a valuable guideline for the understanding of the HC and NBTI reliabilities in an advanced ALD-grown gate oxide processes/devices.**

***Index Terms*—Atomic layer deposition (ALD), gate stack, narrow-width effect, negative bias temperature instability (NBTI), shallow trench isolation (STI).**

I. Introduction

IN PREVIOUS studies [1], for the previous-generation quarter-micrometer CMOS technology, in which the gate oxide is larger than 30 Å, narrow-width shallow trench isolation (STI) exhibits severe degradation after hot-carrier (HC) stress with a reducing gate width. The degradation of pMOSFETs was attributed to an off-state leakage current increase [2] and channel-length shortening [3] because electron trapping exists for a thicker gate oxide. In comparison, for a very thin gate oxide (< 20 Å), the hole trap is the dominant mechanism instead, which leads to an off-state current reduction which is good. However, there are several other issues that become significant with device scaling. According to experimental observations, devices with the STI structure exhibit different degradation mechanisms at various temperatures. Generally, the negative bias temperature instability (NBTI) in pMOSFETs is attributed to the generation of interface traps and oxide trap charges [4]. So far, none has been reported on the enhanced degradation of narrow-width devices in relation to the NBTI effect, especially for a very high-end atomic layer deposition (ALD) gate oxide stack.

In this paper, the aforementioned enhanced degradation at both room temperature (HC effect) and high-temperature stressing (NBTI) has been demonstrated on an advanced ultrathin ALD gate nitride/oxide (N/O) stack. Furthermore, to get more insight into the detailed degradation mechanism, a unique neutralization technique on the oxide charges has been provided, which allows us to identify the generation of interface traps and oxide trap charges. Various experiments have been conducted to confirm that ALD is effective in suppressing the enhanced degradation effect.

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II. Device Preparation

The devices were prepared based on the 90-nm foundry technology. The ALD N/O gate stack was prepared by an advanced remote plasma-enhanced ALD (RPEALD) technique with less H-precursor and N_2 content [5]. The control sample with a heavily plasma-nitrided oxide served as a reference. The ALD and plasma samples have an equivalent oxide thickness (EOT) of 15.4 and 15.5 Å, respectively. The devices with a masked gate length of 0.15 μm and various gate widths were used for the reliability measurement.

III. Results and Discussion

A. Narrow-Width Effect at Room Temperature

Fig. 1 shows the measured device drain–current degradation after the HC stress for pMOSFETs, including $I_{G,\max}$, $I_{B,\max}$, and $V_G = V_D$ stress conditions, respectively. It is generally known that the largest degradation in the ultrathin gate oxide thickness device occurs at $V_G = V_D$ stress as expected. Fig. 2 shows one set of measured drain–current at $V_G = -2$ V for a device with a width $W = 2$ μm before and after $V_G = V_D = -2$ V stresses. The fresh device curve is represented by curve (1), whereas a decrease of the current is represented by curve (2) for the device after the stress. The decrease of the drain–current for devices after the stress can be regarded as an increase of the threshold voltage with the generation of interface trap $N_{\rm it}$ and hole trap $Q_{\rm ot}$. The steps in Fig. 3 will help us clarify the generation of either $N_{\rm it}$ or $Q_{\rm ot}$. First, for a fresh device, the drain–current at $V_G = -2$ V (curve (1) in Fig. 2) and the gate-induced drain leakage (GIDL) current (curve (1)

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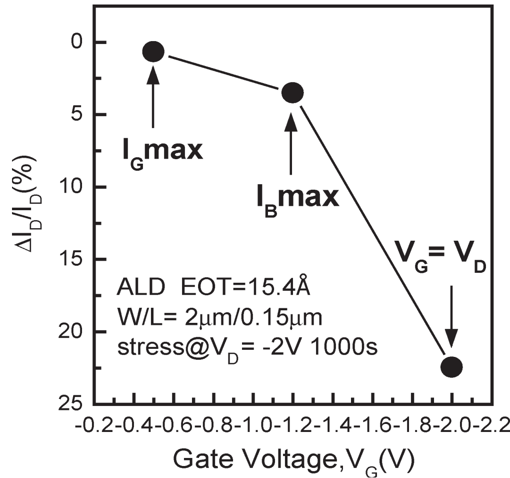

Fig. 1. Drain–current degradation of the thin oxide ALD device under $I_{G,\max}$, $I_{B,\max}$, and $V_G = V_D$ stresses, respectively.

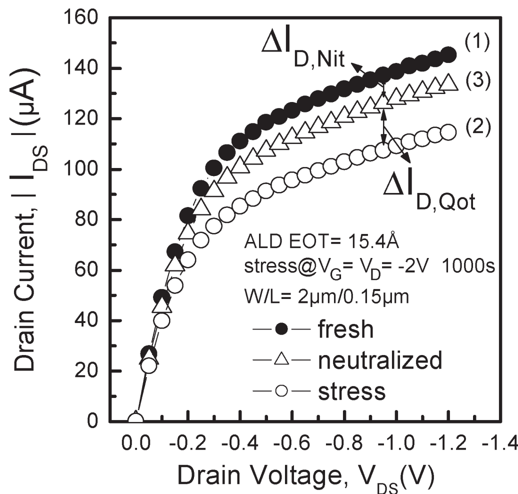

Fig. 2. Drain–current at $V_G = -2$ V for the device before stress [curve (1)], after stress [curve (2)], and after neutralization is completed [curve (3)]. The stress condition is given at $V_G = V_D = -2$ V. Note that the ΔI_D caused by $Q_{\rm ot}$ is larger than that due to $N_{\rm it}$.

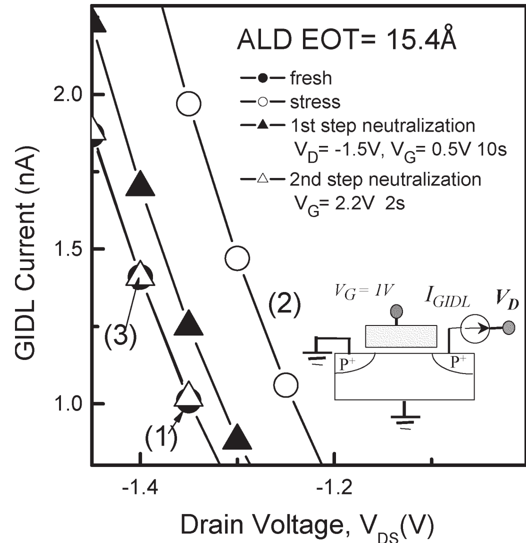

Fig. 3. GIDL currents for the fresh, stressed, and after neutralized. A two-step neutralization is achieved by hot-electron injection to eliminate hole traps.

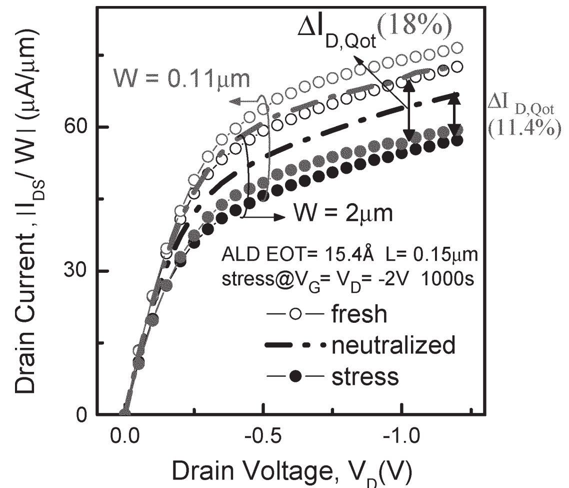

Fig. 4. Comparison of the measured drain–currents for devices with $W = 0.11$ and 2 μm. Note that the generated $Q_{\rm ot}$ is enhanced for narrow-width devices.

in Fig. 3) are measured. Then, both currents are measured after the device was stressed for 1000 s under $V_G = V_D = -2$ V.

Here, we see a clear shift of the GIDL curve to the right, i.e., curve (2). This shift corresponds to a positive threshold voltage shift V_T, caused by $Q_{\rm ot}$, which is an indication of the positive oxide trap. Consequently, a neutralization process is performed by injecting electrons from the substrate into the gate oxide as shown in two steps [6] and with bias conditions given in the figure to fill those positive traps. Here, we see that a shift of the GIDL current, curve (2), will be moved back to curve (3) and then aligned with the fresh one, curve (1). In Fig. 2, the difference of I_D between curves (1) and (3) shows the effect of the generated $N_{\rm it}$, whereas the difference between curves (2) and (3) gives the effect of the generated $Q_{\rm ot}$. From the aforementioned GIDL measurement technique, we can accurately separate the contribution of the interface trap and oxide trap to the drain–current degradations. In a similar manner, we can obtain the same set of curves for narrower width devices, and their comparison with a wide device is given in Fig. 4. In Fig. 3, the contribution of oxide traps $Q_{\rm ot}$ to the drain–current degradation $\Delta I_{D,Q_{\rm ot}}$ is much larger when compared with that contributed from the generation of interface traps $\Delta I_{D,N_{\rm it}}$. These results show that the HC degradation depends mostly on the oxide traps, whereas it depends weakly on the generated interface traps with reducing gate width. It is believed that there are only few oxide traps in the ultrathin gate oxide device. Consequently, a much larger generated $Q_{\rm ot}$ found here should mainly depend on the high nitride density in the gate oxide. Obviously, we can see an enhancement of the $Q_{\rm ot}$ with reducing channel width, i.e., a device with $W = 0.11$ μm has a larger shift (18%) of $I_{D,Q_{\rm ot}}$ as compared with that with $W = 2$ μm (11.4%).

To further study the variation of the threshold voltage with the device gate width, we plotted ΔV_T as a function of the channel width (solid circles) in Fig. 5, from which we can see a large enhancement of the narrow-width effect. This is attributed to the STI mechanical stress as reported in [3]. We know that the STI-enhanced HC stress degradation area is

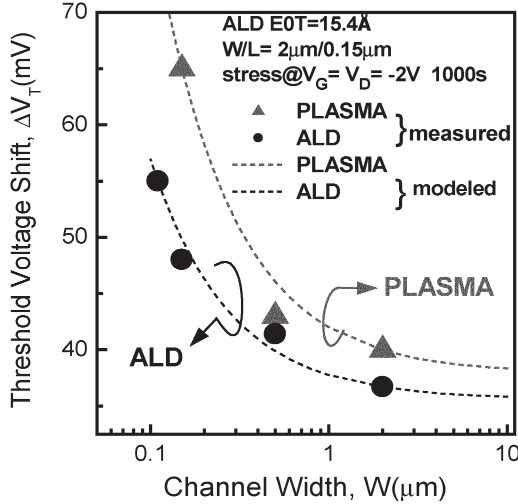

Fig. 5. Calculated threshold voltage shift as a function of width, where the comparison between two different gate oxide processes is also shown.

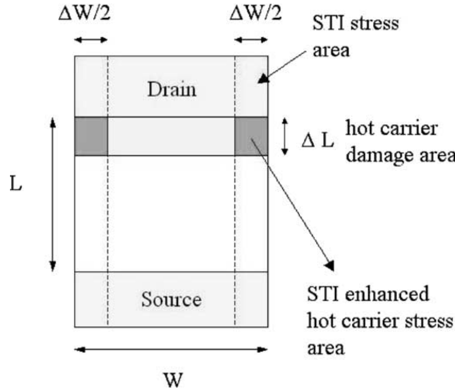

Fig. 6. Model to show the STI damage area, which can be used to predict the V_T shift for devices over a wide range of gate widths.

confined in the edge region of the STI such that the STI edge ratio (i.e., the ratio of the edge region to the total gate width) of a narrower width device is larger. In other words, the threshold voltage shift at the STI edge as caused by the quality of the STI or the mechanical stress is believed to be much larger than that at the channel center, as shown in Fig. 6. Therefore, HC stress degradation is enhanced for a reduction of the channel width and hence induces a larger threshold voltage shift.

To predict the STI effect for the different channel-width devices, from more than two sets of measured V_T and calculated V_T (solid symbols in Fig. 5) for different widths and from the following equation, we can calculate the V_T at another gate width. Here, the total variation of the threshold is given by

$$\{\Delta V_{\rm te} \times \Delta W + \Delta V_{\rm tc} \times (W - \Delta W)\} \times \frac{\left(\frac{\Delta L}{L}\right)}{W} = \Delta V_T \tag{1}$$

where

- $\Delta V_{\rm te}$ threshold voltage shift in the STI edge;
- $\Delta V_{\rm tc}$ threshold voltage shift in the channel center;
- ΔV_T total threshold voltage shift in the whole channel;
- ΔL length of the HC damage area;
- ΔW STI edge width;
- L, W device channel length and width.

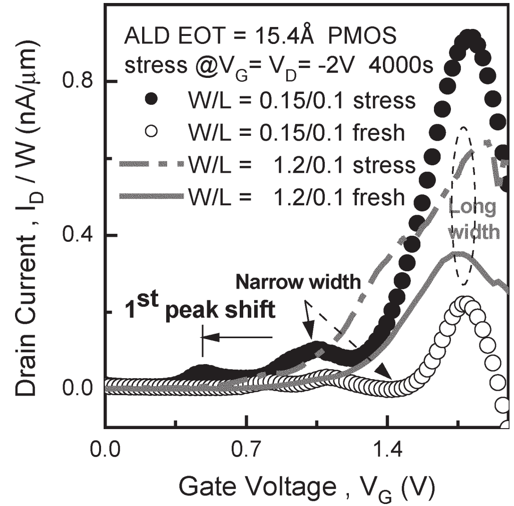

Fig. 7. Measured gated-diode currents for two different gate widths, where the first peak shift in the gated-diode currents shows the generation of more oxide traps for a narrow-width device.

In the preceding equation, the total threshold voltage shift ΔV_T is a combination of $\Delta V_{\rm tc}$ from the channel center region and $\Delta V_{\rm te}$ from the gate edge region. Assume ΔL and ΔW are the same for two different gate-width devices, and from two known values of ΔV_T measured at two different gate widths, we may calculate $\Delta V_{\rm te}$ and $\Delta V_{\rm tc}$ for any gate width according to (1) such that the total ΔV_T can be calculated.

The aforementioned method has an advantage of predicting the degradation V_T for devices over a wide range of gate widths. To further identify whether this V_T is caused by the STI effect, we measured the gated-diode currents [7] for two different gate-width devices as shown in Fig. 7. The first peak shift to the left is a result of width reduction because the first peak in the gated-diode measurement is an indication of the generated $Q_{\rm ot}$, which causes the threshold voltage shift. As commonly known, the increase of the peak currents (the difference between the fresh and stressed ones, e.g., the peaks at $V_G = 1.7$ V) implies the generation of $N_{\rm it}$ after the HC stress. According to the results of the gated-diode measurement in this figure, obviously, the increment of the gated-diode current is larger for narrow-gate-width devices. This further shows that not only $Q_{\rm ot}$ was generated but also $N_{\rm it}$ was increased as a result of width reduction. Therefore, the STI-enhanced degradation in narrow-width devices can be further justified via this gated-diode measurement.

To show a higher gate oxide quality of ALD, the result for the control sample (plasma-treated device) is also shown for comparison in Fig. 5. Note that the V_T rolloff is much worse for the plasma-treated sample. It is commonly believed to be due to a much higher density of the nitrogen in the gate oxide, which induces much larger degradation of oxide traps after the HC stress.

B. Observation of Narrow-Width-Dependent NBTI Effect

To investigate the width dependence of the NBTI effect, Fig. 8 shows the measured drain–currents for two different gate-width devices, where the measurement step is similar to

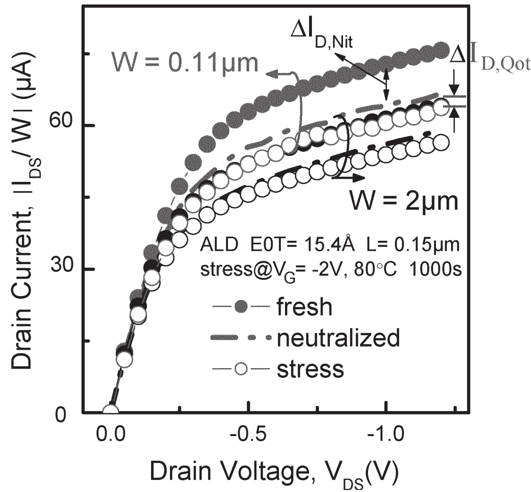

Fig. 8. NBTI measurement. The drain–current for the device with $W = 0.11$ and 2 μm before stress, after stress, and after neutralization are completed. Note that the ΔI_D caused by N_{it} is dominant.

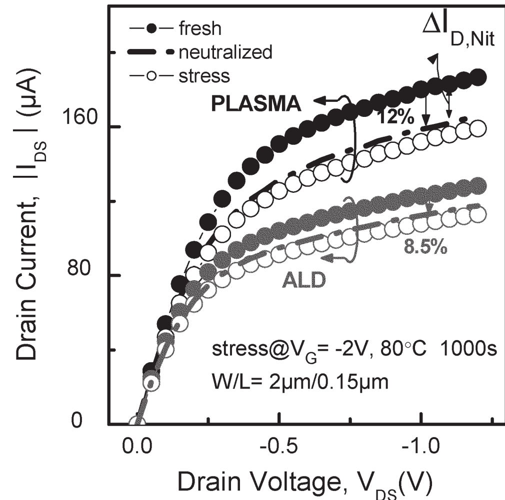

Fig. 10. Drain–current before and after NBTI stress and the comparison for two different gate oxide processes. ALD has much better reliability.

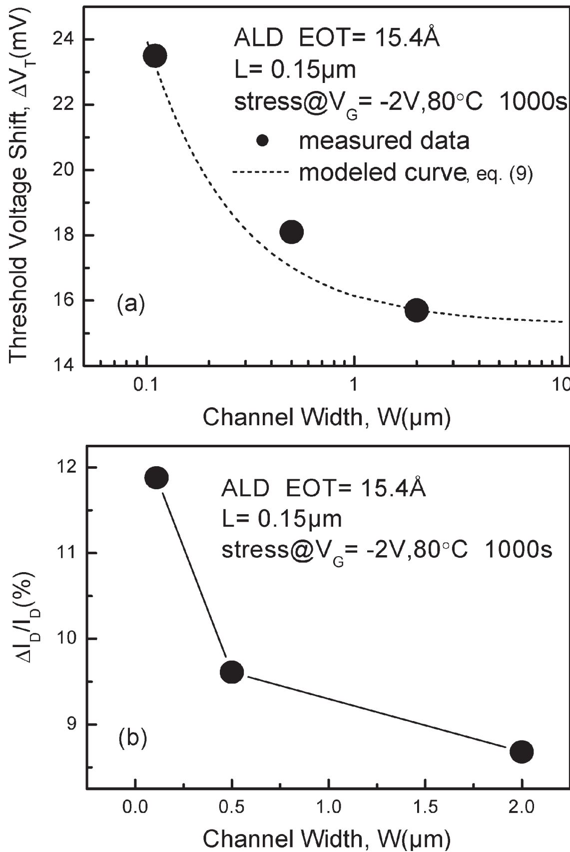

Fig. 9. (a) Threshold voltage shift caused by the NBTI-induced interface traps. (b) I_D degradation caused by the NBTI-induced interface traps.

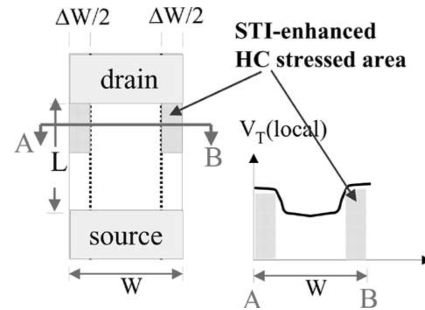

Fig. 11. Illustration of the width narrowing model, in which the shaded area is still OFF when the channel begins to conduct.

that given in Fig. 2. As a result of the recovery of V_T after turning off the NBTI stress, it was found by comparing the data with the dashed lines and the open circles that Q_{ot} becomes smaller. Therefore, N_{it} will become the dominant factor of the drain–current degradation as well as the V_T shift. Here, the drain–current degradation $\Delta I_{D,N_{\mathrm{it}}}$ becomes much larger from the comparison of the dashed lines and solid circles. Q_{ot} is nearly negligible here. It is attributed to the near interface oxide traps, which are recovered in a very thin gate oxide. Therefore, we plot in Fig. 9(a) and (b) the enhancement of the V_T rolloff and I_D due to the generated N_{it} only. In other words, the observed Q_{ot} after NBTI becomes weaker compared with the generated N_{it} at an elevated temperature, and the interface traps become the dominant mechanism for the I_D degradation. The narrow-width-dependent NBTI degradations for two different gate oxide processes are shown in Fig. 10.

C. Further Insight of the Trap Generation and the Model

To reasonably explain the observed enhancement effect caused by the STI, for the first time, a model called width narrowing, which is different from that in [3], is proposed in Fig. 11. In a comparison between a wide- and a narrow-width device, after the HC stress, the STI corner exhibits an area where the channel beneath this region has a larger local threshold voltage due to the positive hole trap (Q_{ot})-induced damage, in which a larger local threshold voltage is observed at the gate edge. If the local threshold voltage shift is sufficiently high, it results in an effective width, $W - \Delta W$, such that ΔV_T is enhanced for a narrower width device [Figs. 5 and 9(a)]. Another most important implication from Fig. 8 is showing that the NBTI effect will generate more interface traps N_{it} for a narrower device as a result of the STI effect. By combining the two preceding factors, the result and physical mechanism

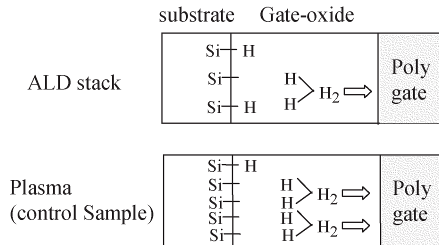

Fig. 12. Comparison of the hydrogen release between ALD and plasma samples. Note that ALD has lower H_2 content and hence a slower H_2 removal rate.

in an ultrathin gate oxide device are quite different from the last-generation quarter-micrometer generation devices in that the degradation comes from the channel shortening [3] or electron traps.

The mechanisms related to an $N_{\rm it}$ increase and a $Q_{\rm ot}$ relaxation after NBTI are more interesting and can be drawn as follows.

1) Both $N_{\rm it}$ and $Q_{\rm ot}$ are caused by the hydrogen release from the surface toward the polygate [8], [9]. The generation of $N_{\rm it}$ is smaller for ALD because ALD has less hydrogen content (see the comparison in Fig. 12) and hence a slower release rate of H_2.
2) The hole trap generation can be measured by the low-voltage stress-induced leakage current (LV-SILC) method [10] with results given in Fig. 13, where we see that ALD exhibits smaller SILC and hence smaller hole traps, smaller SILC, and V_T (Fig. 5).
3) Resulting from the recovery of V_T or $Q_{\rm ot}$ (Fig. 10, especially under NBTI), the $N_{\rm it}$ in the plasma sample is aggravated due to a heavier N_2 content at the interface as hole traps are moved back to the substrate.

We therefore have the following conclusions.

1) NBTI and HCI device degradations are enhanced with reducing gate width, which show the STI effect.
2) Under NBTI stress, ALD exhibits much less $N_{\rm it}$ generation and hence much better reliability compared with plasma film.
3) Gate oxide formation process with ALD is proved to be more reliable than that of the plasma film in terms of the HC stress effect (at room temperature) and NBTI reliabilities (at high temperature).

IV. Conclusion

The origins of enhanced drain–current degradation and its dependence on the narrow-width effect in pMOSFETs have been extensively studied. New results on the HC- and NBTI-stress-induced device degradations in scaled STI pMOSFETs have been reported. The separation of the degradation type, including interface trap and oxide trap via a so-called neutralization step and GIDL measurement, is proposed to verify the generated oxide trap and interface trap.

For the evaluation of the HC and NBTI reliabilities, different temperature dependences are observed. At room temperature, from the HC test, the hole trap is dominant for the device V_T shift, whereas the interface trap is more significant and

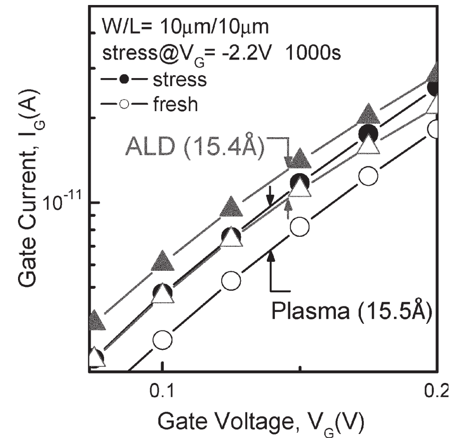

Fig. 13. LV-SILC measurement at low V_G, which shows that much more $N_{\rm it}$'s are generated near the conduction band for plasma-treated sample.

responsible for the I_D degradation after NBTI stress at high temperature. Moreover, the V_T rolloff can be well explained by a width narrowing effect physically, and a quantitative model is further proposed. Results have clearly shown that the generated interface/oxide traps are strongly related to the hydrogen and N_2 content in the gate oxide formation process. Therefore, the results provide us a useful guideline for understanding the HC- and NBTI-related reliabilities in an advanced gate N/O stack 60 nm and beyond CMOS processes/devices.

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