Sub-mW 5-GHz Receiver Front-End Circuit Design

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Abstract **— In this work a 5-GHz receiver front-end is designed for the application of wireless sensor networks. The circuit topology is chosen available for low supply voltage below 1V. The stability condition of the LNA circuit is ensured by adding reactive components. Total power consumption of the fabricated circuit is 0.86mW, of which 0.7mW goes to the LNA stage. The measured return loss and conversion gain are 11dB and 25dB, respectively. The noise figure is 12dB and the IIP3 is around -6.5dBm.**

Index Terms **— Low power design, low-noise amplifier, single-balanced mixer.**

I. Introduction

Ultra-low power consumption is critical to the emerging application of wireless sensor networks. It allows long lasting use of sensor nodes, fixed or portable, without battery replacement. This helps ubiquity in data collection, such as bio-medical monitoring in body-area networks or alarm sensing in intelligent buildings. As pointed out in [1], it requires average power consumption in the order of 10μW to ensure appropriate lifetime extension. This results in less than few milli-watts in low duty-cycle wireless data transmissions [2]. As far as power consumption is concerned, RF front-end circuits typically consume much more than that of the other circuit blocks. It is therefore worth of great effort on power reduction in the RF circuits.

Low supply voltage is an effective method to reduce power consumption. It directly reduces the voltage-current product if the total current remains in a similar level. It also meets the technology trend of scaling down. Besides, it lifts up the possibility of using a single solar-cell source if the supply voltage could be as low as 400mV [1].

In this work a receiver front-end is designed in 0.18um CMOS technology with a supply voltage chosen as 1V. The power consumption level is limited below 1mW for operation longer than months in low duty cycle systems. The popular cascode topology that utilizes current reuse is not employed, neither the folded topology that requires two DC current paths. Instead, the low-noise amplifier (LNA) makes use of a single transistor according to microwave amplifier design. The mixer transistors are operated in the subthreshold region. All the design efforts successfully ensure low power consumption.

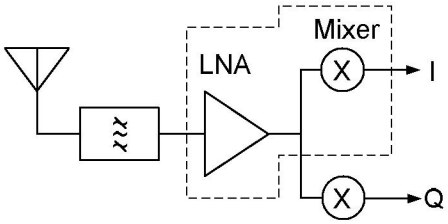

Fig. 1. The receiver front-circuit under consideration, including the LNA and mixer circuits in the dashed box.

II. Design Consideration

The receiver front-end circuits under consideration include a low-noise amplifier (LNA) and a mixer, as shown in Fig. 1, designed to operate in the 5-GHz ISM unlicensed frequency band. Applied to the sensor nodes of short distance body-area networks, circuit performance requires no distinguished dynamic range. Acceptable trade-off between linearity and noise figure call for the condition that most power shall be assigned to the LNA stage for better overall performance.

A. *LNA Circuit Design*

The proposed circuit schematic is as shown in Fig. 2. The circuit topology is chosen to allow a low supply voltage below 1V. The LNA stage is implemented by a single transistor M3 biased in the saturation region to provide sufficient signal gain. The biasing point and the transistor size are chosen to achieve good compromise among those parameters of the gain, the minimum noise figure, and the power consumption.

The major issue is the stability condition. In the single MOS transistor amplifier, the electrical feedback due to the gate-drain capacitance Cgd must be taken into account such that bilateral amplifier design is required. As can be found, this causes the amplifier appear as conditionally stable. The load stability circle typically cuts into the upper region of the Smith chart, which means a capacitive load is preferred to avoid instability. An inductive load, however, is necessary to conjugately match the capacitive output impedance at the drain port. In the popular cascode configuration [3], this is not an issue at all since the load

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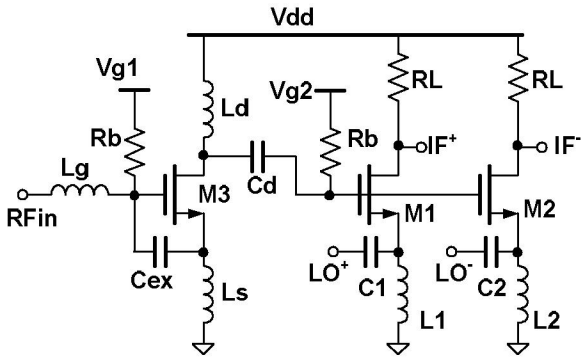

Fig. 2. Circuit schematic of the receiver front-end. The LNA circuit is a single-transistor amplifier (M3) with inductive source degeneration to improve stability. The mixer circuit consists of a transistor pair biased in the subthreshold region for low power consumption.

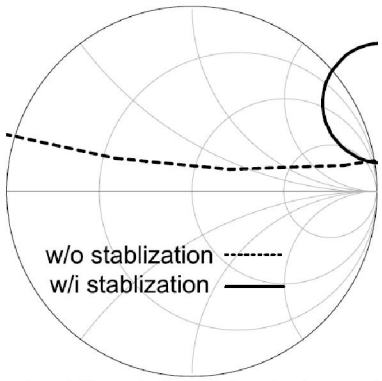

Fig. 3. Load stability circles of the single-transistor LNA at 5GHz with and without reactive stabilization.

impedance presented to the common-source configured transistor is low and capacitive. Not only the Miller feedback of Cgd is decreased, but also the load impedance sits in the stable region. To alleviate the issue, the transistor shall be stabilized by adding external components without much degradation to noise performance. As such, two reactive components, gate-source capacitor Cex and source inductor Ls, are added, instead of resistive elements at the input or the output ports as in the conventional microwave amplifier design [4]. Essentially the two components reduce the available gain somewhat. The Ls also helps simultaneously noise and impedance matching [5]. Fig. 3 shows that the load stability circles at 5GHz moves out of the Smith chart after stabilization. The gives room for impedance matching. Actually the stability condition shall be inspected over the frequency range from very low at 100MHz to 10GHz.

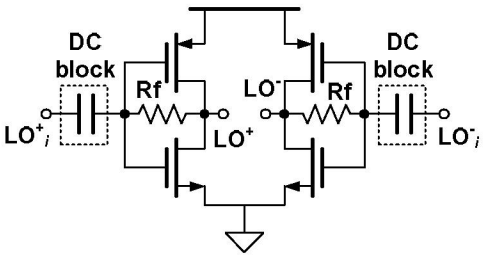

Fig. 4. LO differential signal is buffered by on-chip inverters. External bias-tees are used for DC blocking.

In bilateral amplifier design, the optimal source and the load impedance meet the condition of both simultaneous conjugate matching for matched gain [6]. The condition can be expressed as

$$\Gamma_s = \Gamma_{in}^* \text{ and } \Gamma_L = \Gamma_{out}^*, \quad (1)$$

where Γ_{in} and Γ_{out} are characterized with added Cex and Ls. As Ls already gives a real part to the input impedance, it turns out that only Lg and Ld are used. Such simple matching provides sufficient input return loss, or Γ_s, but not the output return loss. Nevertheless this fully integrated LNA and mixer circuits can tolerate the unmatched load impedance without too much degradation to the gain level.

B. Mixer Circuit Design

The mixer circuit is implemented by the transistor pair M1 and M2 in the single-balanced configuration, as in Fig. 2. It shall provide frequency mixing and the required load impedance to LNA. Since the output impedance of M3 is high, the mixer is better to exhibit high impedance to ease impedance matching. Consequently the RF signal is connected to the gate ports of M1 and M2, while the LO signal to the source ports. Frequency downconversion is different from that in the traditional Gilbert-cell circuit, which, consisting of a transconductance stage and a switching stage, utilizes current commutating. Even though the IF output current could be large, the transconductance stage is very power-consuming, and the DC biasing current in operation will increase dramatically if the switching transistors are driven on-and-off by a large LO voltage swing.

To sustain low power consumption, the transistors are biased in the subthreshold region without large LO swing. The exponential I/V characteristic of a MOS device carries out the nonlinearity that generates frequency mixing. It can be expressed as

$$I_{ds} = I_o \exp(\frac{V_{gs}}{\eta V_T}), \quad (2)$$

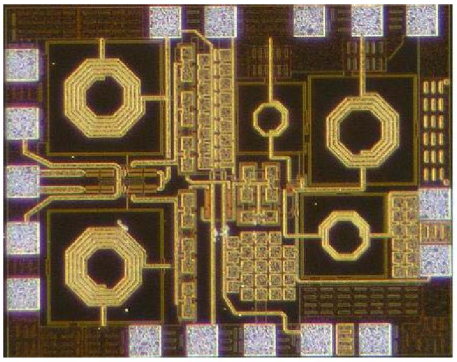

Fig. 5. The micrograph of the fabricated low-power receiver front-end circuit in 0.18um RF CMOS technology.

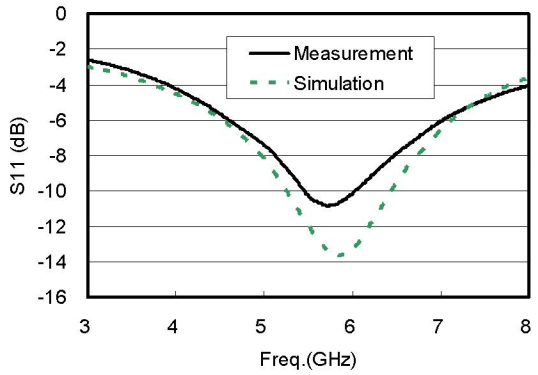

Fig. 6. Input return loss of measured and simulated data.

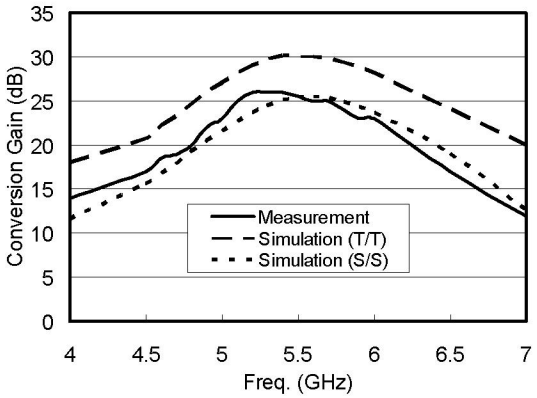

Fig. 7. Conversion gain of measured and simulated data, including both corner cases at typical/typical and slow/slow.

where

$$V_{gs} = V_{GS} + v_{gs} = V_{GS} + (v_{RF} - v_{LO}). \quad (3)$$

The second-order nonlinear term in Eq. (2) results in the desired IF output current but no significant DC current because the LO swing is small due to the low node impedance at the source port. Although large LO swing improves the conversion gain, large voltage conversion gain is still available in this mixer if the output load resistance RL is chosen as large as possible. The largest value of RL is actually limited by the output parasitics. Combined with the output parasitic capacitance, the corner frequency in the low-pass response must be larger than the IF signal bandwidth. A few hundred ohms of RL resistance gives sufficient gain and more than 10 MHz of signal bandwidth. As the bias current is very low, RL does not cause much DC voltage drop. The IF load impedance is typically up to the order of 10K ohms and causes no significant loading effect on the RF resistance.

The LO differential signal is buffered by CMOS inverters, as shown in Fig. 4. The C1-L1 and C2-L2 sections form a high-pass filter and provide DC blocking between the inverters and the mixer core circuit.

III. Measurement Results

The front-end circuit is fabricated in 0.18um RF CMOS technology. The micrograph is shown in Fig. 5. The die size is 1.16 x 0.98 mm^2, including bonding pads. Measurements were conducted by chip-on-board setup. DC pads are wire-bonded on a PCB board. All the signals are through on-wafer probing with a GSG probe to the RF input and GSGSG probes to the LO and IF ports. The differential IF signal is buffered by an on-board OP amplifier of unit gain to convert to a single-ended form. The differential input impedance of the OP amplifier is chosen as 16 Kohms to emulate a high IF loading impedance. A 50-ohm resistor is added in series at the OP amplifier output for impedance matching to 50-ohm measurement systems such that 6dB voltage gain shall be compensated in all the gain measurements.

The supply voltage Vdd is set as 1V in the measurements. The total DC power is about 0.87mW, of which 0.7mW goes to the LNA stage and the rest to the mixer and the LO buffer. Even if both I/Q mixers are fabricated, the total front-end power consumption is still within 1mW. The measured input return loss, plotted in Fig. 6, is centered at the simulated frequency around 5.5GHz with the magnitude better than 10dB but somewhat worse than the simulated data. It is found on the Smith chart that the input impedance is lower than 50 ohms. This could be further improved by enlarging the source inductor Ls to increase the real part under the penalty of gain degradation. The measured conversion gain is about 25dB, as shown in Fig. 7. It is about 5dB short as compared to the simulation. Further analysis indicates that the result is approaching to the slow/slow corner case. However, another uncertainty factor, the modeling accuracy of MOS devices in the subthreshold

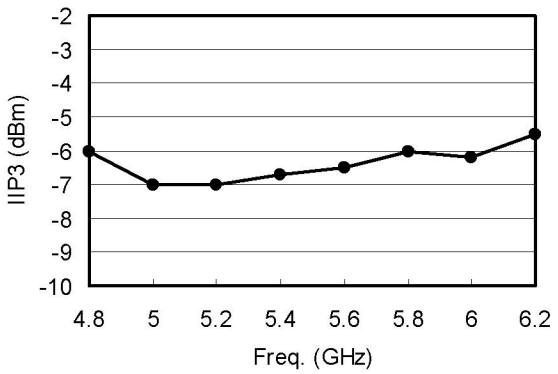

Fig. 8. Measured IIP3.

region, might also contribute to this discrepancy. The measured NF and IIP3 are 12 dB and -6.5 dBm, respectively, as shown in Fig. 8 and Fig. 9. The noise figure is worse than the simulated data in both corner cases.

IV. Conclusion

A low-power receiver front-end circuit is designed and fabricated in 0.18um CMOS technology, with power consumption less than 1mW for applications of wireless sensor networks. Measurement circuit performance is applicable to low duty-cycle data transmission. Although the supply voltage is set as 1V, it can be further lowered down for the circuit topology chosen.

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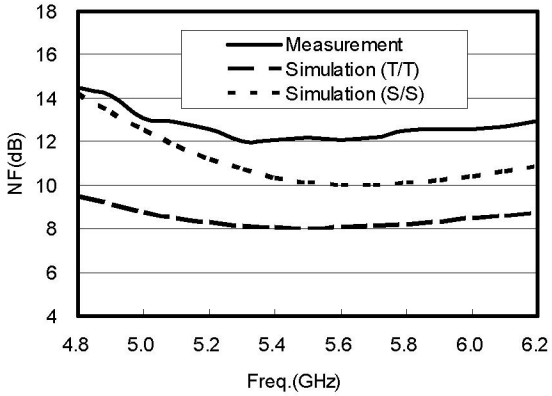

Fig. 9. Measured noise figure (in solid line), higher than simulation data of both corner cases (in dashed lines).

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