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Comparison of characteristics and integration of copper diffusion-barrier dielectrics

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Abstract

The characteristics of various copper (Cu) barrier layers, including SiN, SiCN, and SiCO, were investigated in this work. Carbon-based barrier films (SiCN and SiCO) improved the dielectric constant and line-to-line capacitance, but led to sacrifice in film deposition rate, diffusion-barrier performance, and adhesion strength to Cu in comparison with SiN films. In addition, SiN and SiCO films showed the superior electromigration (EM) performance and stress-induced void migration (SM) performance, respectively. Furthermore, the reliability results of SM and EM are strongly related to the barrier film stress characteristics and the adhesion strength between Cu layers. Therefore, optimization of the barrier layer stress and the enhancement of the interfacial condition between Cu and barrier films are crucial to significantly improve reliability.

Keywords: Barrier layer; Low dielectric constant; Adhesion strength; Capacitance

1. Introduction

The interconnect resistance–capacitance (RC) delay is a dominant factor in determining the performance of ultra large-scale integrated circuits as minimum device shrinks below 180 nm. Although many low-k ($k<3$) materials has been used as interlayer dielectrics (ILD), high dielectric constant ($k=7\sim8$) of silicon nitride (SiN) film is still the primary candidate for the Cu cap barrier and etch stop layer (ESL) required in the Cu damascene process [1–3]. Thus, this increases the effective k value of stack dielectric films, and limits the reduction of the RC delay in ultra large-scale integration [4,5]. As a result, amorphous silicon carbide (SiC), amorphous silicon nitricarbide (SiCN), and amorphous silicon oxycarbide (SiCO) deposited using a plasma-enhanced chemical vapor deposition (PECVD) system have received much attention for applications as Cu cap barrier and ESL in Cu damascene process [6–9]. The intrinsic properties of carbon-doped barrier films (SiCN and SiCO) have been extensively investigated by many researchers [10–12]. However, very few papers have studied the integration and reliability of barrier dielectrics in the Cu dual damascene process [13,14].

In this work, we investigated the physical properties, thermal stability, and integrated electrical performance for SiN, SiCN and SiCO dielectric barrier films. Furthermore, reliability results of electromigration (EM) and stress-induced voiding migration (SM) related to the deposited film's properties were also studied.

2. Experiment

All thin film deposition was performed on an Applied Materials Producer system with a 200 mm DxZ chamber. The thin film was deposited on a p-type (100) silicon substrate by using radio frequency (13.56 MHz) PECVD. A gas mixture of trimethylsilane (3MS) and helium (He) were employed with either NH_3 or CO_2, which were used to deposit SiCN or SiCO films, respectively. The detailed process conditions for different Cu barrier dielectrics are listed in Table 1.

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Table 1
The process conditions of various Cu barrier dielectrics

	SiCN	SiCO	SiN
Chemical source	3MS+NH_3+He	3MS+CO_2+He	SiH_4+NH_3+N_2
Gas ratio	1:2:5	1:4:2.5	3:1:80
Deposition temperature (°C)	350	350	350
Deposition pressure (Pa)	400	400	560
RF power (W)	300	300	450

Film thickness and refractive index (RI, at 633 nm wavelength) of all as-deposited films were analyzed by reflectometer and/or ellipsometer using the Nano-Spec® 9100. The chemical composition was investigated using Rutherford Back-scattering Spectroscopy (RBS). The dielectric constant and leakage current of the barrier dielectric were measured by mercury (Hg) probe using current–voltage (I–V) and capacitance–voltage (C–V) method (5100 CV system) on 300-nm-thick films. The dielectric constant (k) was measured at 1 MHz.

The line-to-line leakage current was measured using a comb-type capacitor, which is a single damascene Cu interconnection with a line spacing of 180 nm. The line-to-line leakage current was measured with a DC source/monitor system by applying 1 V.

EM studies were carried out on wafers with the 2-level metallization architecture at a temperature of 300 °C, applying a current density with 2 MA/cm^2. The failure criterion was a 10% relative increase in resistance. The EM test pattern consisted of 20 contact vias linked with an underlying metal line, with a length of 1000 μm.

In SM testing, the samples were stored in a vacuum oven at a temperature of 175 °C for 500 h. The resistance measurement was performed at room temperature after thermal stress test. The SM failure criterion was 100% relative increase in resistance.

3. Results and discussions

3.1. Physical properties

Table 2 shows the basic film properties of different barrier dielectrics studied in this study. From the results, the deposition rates of SiCN and SiCO films range from 120 to 150 nm/min, about half of that of the SiN film. For all barrier dielectrics in this study, the deposition rate is favorable and well controlled for thin film deposition, as the barrier dielectric film used in the inter-layer dielectric (ILD) is around 50 nm thick.

The dielectric constant at 1 MHz consists of three components arising from electronic (k_e), ionic (k_{ion}), and orientational (k_{ori}) polarizations [6,10] is governed by the following relation,

$$k(1\ \mathrm{MHz}) = k_e\left(n^2\right) + k_{ion} + k_{ori} \quad (1)$$

The electronic polarization is the square of the refractive index (n) at 633 nm wavelength arising from the displacement of the electron shell relative to a nucleus. The ionic polarization results from the displacement of a charged ion with respect to other ions, and the orientation polarization arises from the change of orientation for the molecules with a permanent electric dipole moment in an applied electric field. As seen in Table 2, carbon-doped barrier dielectrics (SiCO and SiCN) exhibit lower dielectric constants related to SiN films, which is mainly contributed to the occurrence of alkyl groups (Si–CH_3) groups, which reduce ionic (k_{ion}) and orientational (k_{ori}) polarizations. Thus, this helps to reduce the dielectric constant. Furthermore, the refractive index of the SiCO is the lowest, resulting in lower electronic dielectric constant, and thus lower dielectric constant at 1 MHz. This is because of the replacement of Si–C with Si–O bond in the SiCO film and the higher electronegativity of oxygen atom.

The stress of SiN, SiCN, and SiCO films at room temperature was 1.29×10^9, 2.96×10^9, and 2.26×10^9 dyne/cm^2 in compressive, respectively. The compressive stress in these three barrier dielectrics is high enough to achieve a robust stack stability [11,15]. However, the largest stress change after the 420 °C annealing temperature was observed in SiCN films. The shift magnitude of the SiCN film after the 420 °C thermal cycle was about 1.26×10^9 dyne/cm^2, which is significantly higher than that of SiN (1.02×10^9 dyne/cm^2) and SiCO (1.20×10^9 dyne/cm^2). It is speculated to the higher degree of porosity because of the presence of spacially occupied Si–CH_3 groups. Although the stress change of the SiCO film is higher than that of the SiN film, the stress of the SiCO film remains stable during thermal treatment process. This implies that SiCO films have excellent stress stability during thermal annealing.

3.2. Capacitance reduction

In order to investigate the barrier dielectric effect on the interconnect capacitance, the Cu wiring capacitance struc-

Table 2
Film properties of various Cu barrier dielectrics

	SiCN	SiCO	SiN
Deposition rate (nm/min)	153.1	133.8	326.7
RI (633 mm)	1.946	1.8183	1.9126
Dielectric constant	5.27	4.555	7.26
Electronic (k_e)	3.79	3.31	3.66
Ionic (k_{ion}), and orientational (k_{ori})	1.48	1.25	3.60
RBS (Si/O/C/H/N)	26:0:18:37:19	28:13:26.5:32.5:0	45:0:0:12.5:42.5
Leakage current density (10^{-9} A/cm^2 at 1 MV/cm)	22.90	8.97	1.48
Intrinsic stress (10^{-9} dyne/cm^2)	−2.69	−2.26	−1.26
Stress change after 450 °C annealing (10^{-9} dyne/cm^2)	1.26	1.20	1.02

ture illustrated in Fig. 1(a), which follows standard 0.13 μm node design rules, was simulated using Raphael analysis. Fig. 1(b) shows the simulation results of wiring capacitance for different barrier dielectric/low-k dielectric structures. The total capacitance of the low-k (OSG; $k=3.0$)/SiCO structure can be reduced by about 16% compared to the FSG ($k=3.5$)/SiN structure. On the other hand, the total capacitance of the FSG/SiCO structure can also be reduced by about 10%. However, if we change the ILD layer from FSG film ($k=3.5$) to OSG film ($k=3.0$), the total capacitance reduction is only 8%. As a result, it can be seen that the option of a low-dielectric constant barrier dielectric is essential in reducing the total capacitance of interconnects.

3.3. Cu barrier ability against the Cu penetration

The effect of various barrier dielectrics on the barrier ability against the Cu penetration was evaluated using secondary ion mass spectroscopy (SIMS) analysis. Thin Cu films were deposited on p-type wafers using electroplating. Following the 600-nm-thick Cu deposition, a barrier layer (SiN, SiCN, or SiCO) with a 50-nm-thick film was deposited using a PECVD method. Finally, a layer of 50-nm-thick low-k (organo-silicate-glass; OSG) film was deposited to complete the test structure. The samples were then conducted by thermal annealing. The annealing condition was 400 °C for 1 h in a nitrogen atmosphere and the annealing process required 7 heating/cooling cycles in total. Next, analytical characterization was performed using SIMS to trace the Cu intensity within the test structure. A noticeable difference in the diffusion of Cu was observed as shown in Fig. 2, where SiCO films have a poor Cu barrier efficiency. The poor barrier properties of the SiCO film against Cu penetration may be attributed to a higher percentage of micro-voids. Since SiCO films contain a rich carbon content, the molecular structure of SiCO film becomes more like a polymer, with less cross-linking, and an enhanced film porosity [12,15]. As a result, Cu atoms easily penetrate into the film. When the Cu diffusion depth is defined as the region with a three-order reduction in Cu concentration, the Cu diffusion depth for SiN, SiCN, and SiCO can be calculated as approximately 12, 25, and 35 nm. This indicates that when the thickness of a barrier layer is

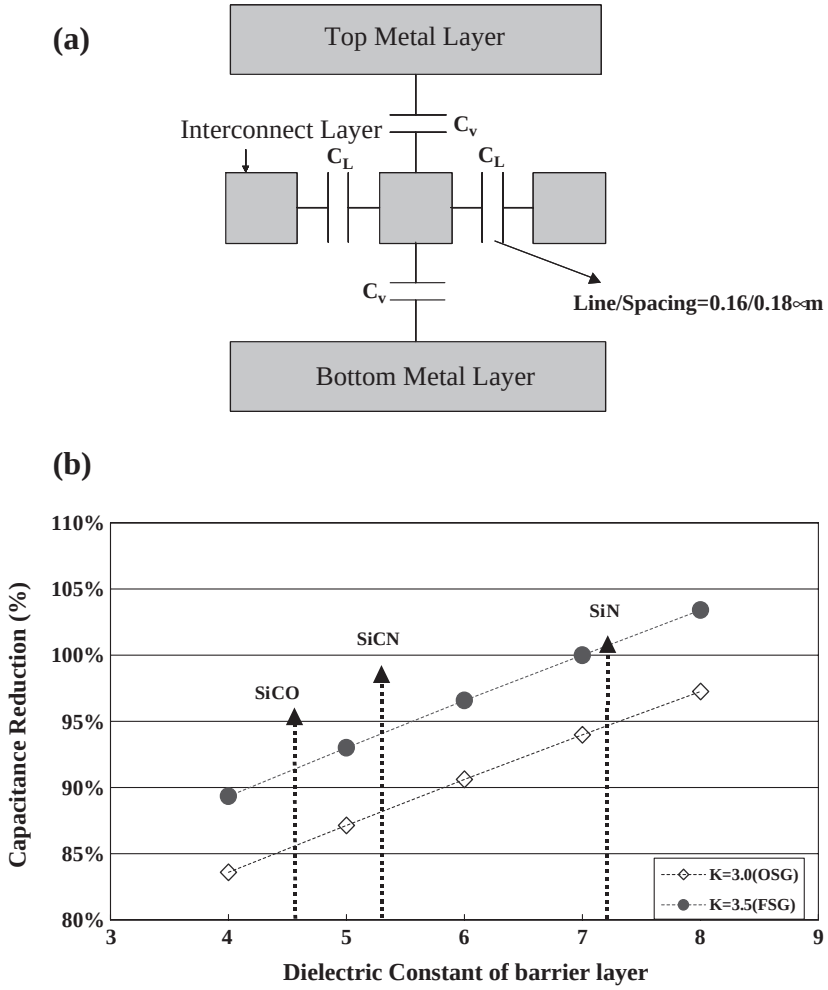

Fig. 1. (a) Schematic view of two-dimensional wring capacitance simulation structure. (b) Simulation results of wring capacitance dependence of the dielectric constant of low-k/barrier films (FSG/SiN=1).

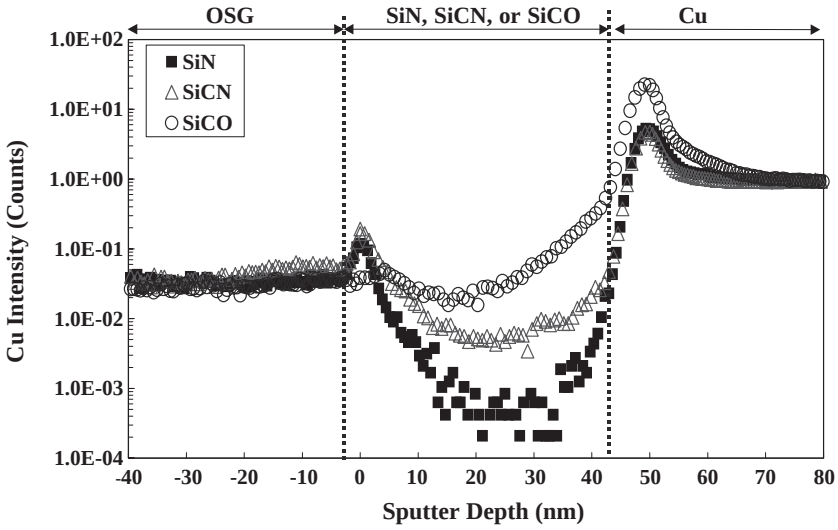

Fig. 2. SIMS profile of copper obtained with OSG/SiN, SiCN, and SiCO/Cu/TaN/Si structure.

higher than 50 nm, this layer could efficiently prevent the Cu drift into the low-*k* dielectrics.

3.4. Adhesion strength between Cu and low-dielectric film

Fig. 3 shows the adhesion strength dependence for various barrier dielectrics with Cu and low-*k* films (FSG and OSG). The adhesion strength is in order of SiCO < SiCN < SiN for both low-*k* film cases. Additionally, the adhesion strength of barrier dielectrics with Cu is lower than that of barrier dielectrics with low-*k* films for these three types of barrier films. This indicates that the interface between the Cu and the barrier layers may be the weak point, which induces reliability issues. Notably, N-doped barrier dielectrics have the superior adhesion ability, indicating that the nitrogen element in the barrier film may provide a new chemical bonding with adjacent layers, which results in an increase of the adhesion strength.

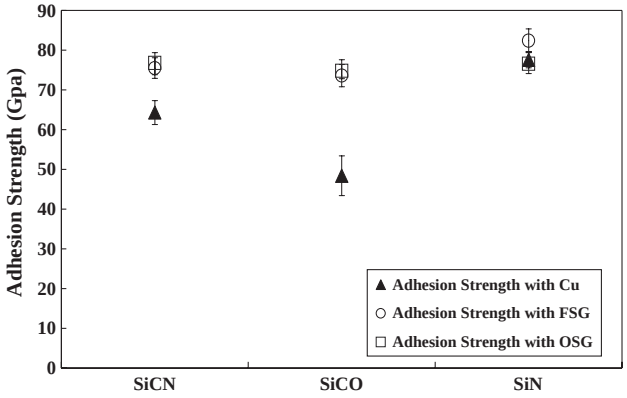

Fig. 3. Adhesion strength with Cu, OSG, and FSG for SiN, SiCN, and SiCO barrier films.

3.5. Electrical performance

Fig. 4 shows the cumulative probability of 20 *k* via-chain resistance for three types of barrier dielectrics. The FSG/SiCO scheme shows a higher resistance and wider distribution than that of the FSG/SiN scheme. The possible explanation for this is that as the via etch extends into the barrier layer, the rich carbon content of the SiCO film enhances the polymer formation on the via-bottom. This contamination can outgass during metal deposition, resulting in metal–oxide reaction products, and higher via resistance. As shown in Fig. 4, it is clear that there are no significant changes of via resistance after thermal stress (400 °C, 2 h), indicating a notable thermal stability for these barrier dielectrics.

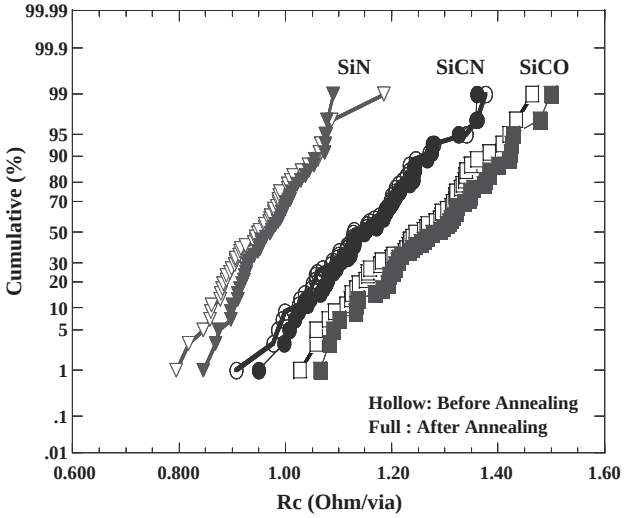

Fig. 4. Via chain resistance distribution before and after annealing for SiN, SiCN, and SiCO barrier films.

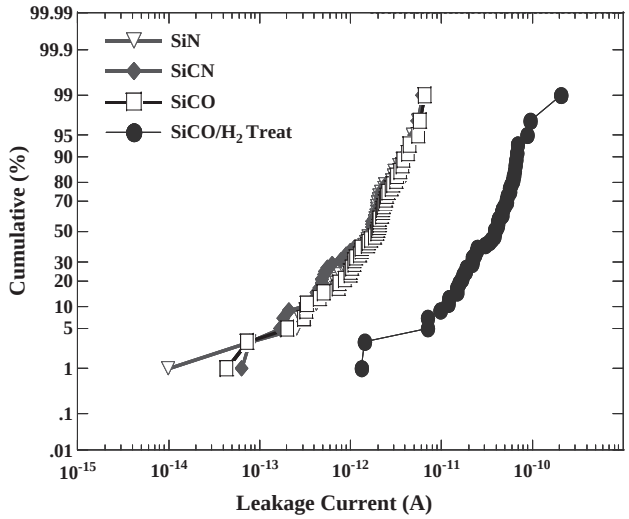

Fig. 5. Metal line-to-line leakage current distribution for SiN, SiCN, and SiCO barrier films.

3.6. Metal line-to-line leakage current

The leakage current distribution for various barrier dielectrics is compared in Fig. 5. Although the SiN film has the lowest blanket film leakage current at 2 MV/cm (shown in Table 2), Fig. 5 reveals that the line-to-line leakage current for these barrier dielectrics has no significant difference under a NH_3 plasma pre-treatment prior to barrier layer deposition. In the case of an H_2 pre-treatment, the line-to-line leakage current is one order of magnitude larger than that of the NH_3 plasma pre-treatment. This result implies that the migration of the Cu atom is on the interface between the Cu and the barrier dielectric. A higher line-to-line leakage current for the H_2 pre-treatment is the result of the weak adhesion strength between the Cu and the SiCO film. Therefore, it is concluded that the pre-treatment modifies the surface condition between the Cu and the barrier dielectric, leading to excellent adhesion and a reduced amount of CuO at the Cu interface.

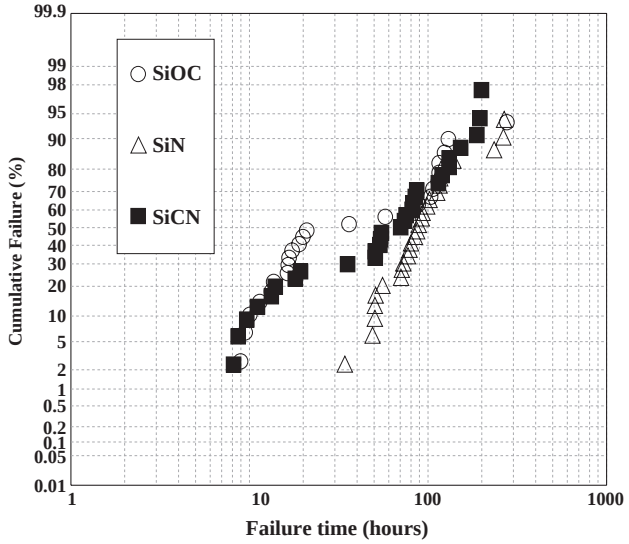

Fig. 6. Time to failure distribution for contact-via for SiN, SiCN, and SiCO barrier films.

Table 3
Electromigration results in the contact-via of various Cu barrier dielectrics

	SiCN	SiCO	SiN
MTF (h)	51.39	21.58	74.18
σ	1.01	1.08	0.43
Initial failure time ($T_{0.1}$)	2.27	0.76	19.93

MTF is the measured median time to failure, and σ is the standard deviation of natural log of the failure times.

3.7. Electromigration (EM)

Fig. 6 shows the time to failure distribution of electromigration plotted in a lognormal scale for SiN, SiCN and SiCO structures, respectively. Median Time to Failure (MTF) and standard deviations deduced from lognormal plots are reported in Table 3. The MTF of the SiCO structure was about 21.58 h, whereas in the SiN structure, the failure did not occur until 74.18 h. This result reveals that the electromigration resistance of Cu with SiN is much better than that with SiCN or SiCO film, where the SiCO structure shows the worst results. From the SEM analysis shown in Fig. 7, the extent and location of the voids were significantly different for three kinds of samples. There are two typical mode of the void formation. In the case of SiCN films, most voids were formed at the interface between the Cu and the SiCN film. For SiN films, voids were formed under the via-bottom. On the other hand, in case of SiCO film structures, both types of voids were observed.

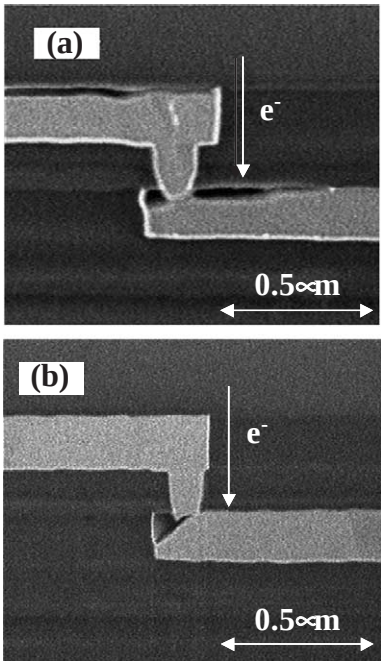

Fig. 7. TEM images of EM failure on contact-via: (a) SiCO and (b) SiN.

The possible reason for these behaviors is the higher residual tensile stress of Cu line with the barrier dielectric, which induces a higher stress on the Cu line. As a result, the void nucleates due to higher residual tensile stress of Cu line with the barrier dielectric. As the voids form at the Cu/TaN surface, it results in the stress gradient as a chemical potential gradient, which in turn, leads to the diffusion of the Cu atoms. Consequently, as the interface weakens as with the Cu/SiCO interface, the voids grow along the Cu/SiCO interface (Fig. 7(a)). Since the implementation of SiN film as a Cu barrier layer can improve the adhesion ability between the Cu/SiN interface, most voids are constrained on the via-bottom (Fig. 7(b)). On the other hand, the higher residual compressive stress of SiCN film induces a high stress gradient on the via-bottom, which inhibits the electron migration along the grain boundary. Therefore, Cu atoms would migrate along the interface between Cu and SiCN films, which forms voids in the Cu/SiCN interface. From these observations, we can conclude that barrier dielectrics with excellent adhesion strength with Cu and a higher compressive stress possess a better EM performance [16–18].

3.8. Stress-induced-void migration (SM)

Stress-induced-void migration is one of the problems related to the reliability of Copper interconnects in semiconductor devices. Repeated cycling from ~400 °C to room temperature causes residual film stress that can lead to stress migration failures. The difference in the coefficient of thermal expansion (CTE) of Cu and barrier dielectric makes stress management in the stack more challenge. Furthermore, in the Cu fabrication process, the CVD process is performed at a high temperature, about 350 ~ 400 °C. As a result, a high temperature ambient causes Cu expansion during Cu-diffusion barrier layer deposition and shrinkage after deposition.

Table 4 shows the relative failure frequency of resistance shift (>100%) versus the tested barrier dielectrics, which was collected from 72 sites after 500 h baking at 175 °C. From the TEM observation on the failure sites, the Cu in the via was pulled up, resulting in Cu voiding at the via-bottoms (Fig. 8). In addition, SiCN films have the highest failure rate. Higher stress is thought to be applied to the Cu film in the via during the high temperature thermal treatment due to the higher CTE of the SiCN related to Cu. The expansion of the Cu wiring at process temperatures around 175 °C gives the stress the ILD around the Cu wiring. The Cu atoms in the vias were strongly squeezed out

Table 4
The failure rate of the stress-induced voiding of various Cu barrier dielectrics

	SiCN	SiCO	SiN
Failure site/total site	7/72	0/72	4/72

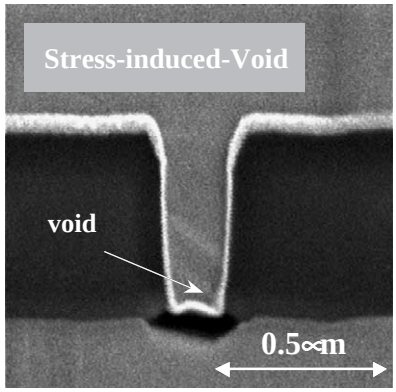

Fig. 8. TEM images of SM failure.

by the thermal stress caused by barrier films with higher residual stress. On the other hand, SiCO films can prevent via degradation because the stress of the SiCO film is lower than that of SiCN and remains constant (shown in Table 2) after the 420 °C thermal cycle. Less stress force was applied to the Cu film in the via during the thermal treatment. Therefore, the failure rate decreases when using SiCO films as the barrier dielectric. Although the intrinsic stress of SiN film is the lowest, the stress change is larger than that of SiCO film and moves from compressive to tensile stress after the 420 °C thermal annealing. This behavior is different from the Cu film stress–temperature cycle, and causes the stress mismatch between the Cu film and SiN films. From stress-induced-void migration results, barrier dielectrics with lower and more stable stress level would appear to suppress the void formation. However, this conclusion partly conflicts with EM requirements, which demand the excellent adhesion strength with Cu and a higher compressive stress for the Cu barrier dielectric. As a result, the optimization of the barrier dielectric properties and pre-treatment conditions seems to be a feasible method for obtaining robust reliability results. A more detailed study will be discussed in future publications.

4. Conclusion

This paper describes the film characterization of Cu barrier layers (SiN, SiCN, and SiCO) in detail, in conjunction with electrical and reliability results. Although SiCN and SiCO achieve a reduced dielectric constant, the biggest challenge is to achieve comparable robust integration as the C and O doping into the dielectrics causes integration problems, such as poor adhesion with Cu and a higher coefficient of thermal expansion. Experimental results show that SiCO films have the best stress-induced voiding resistance as a consequence of a lower and stable temperature–stress curve, but this is offset by poor electromigration due to poor adhesion. Consequently, optimization of the barrier layer stress and enhancement of the Cu barrier layer interface are needed to significantly enhance EM/SM reliability.

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