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Integration issues for siloxane-based hydrogen silsesquioxane (HSQ) applied on TFT-LCDs

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Abstract

In this study, a low-*k* material, siloxane-based hydrogen silsesquioxane (HSQ) has been investigated for a passivation dielectric between the transistor and pixel levels in thin-film transistor (TFT) arrays. The characteristics of low-*k* dielectric film have been studied, especially under visible light illumination and electric operation. Compared with the conventional nitride film ($k \sim 7$), the HSQ passivation layer ($k \sim 2.8$) not only lowers the RC time delay in device, but also enhances the brightness of thin-film transistors liquid crystal displays (TFT-LCDs).
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Keywords: TFT; Low-*k*; Passivation

1. Introduction

Recently, the technology requirements of hydrogenated amorphous Si (a-Si:H) thin-film transistor liquid crystal display (TFT-LCD) in the electronic industries have become more strict with the panel being larger. The dielectric materials that have high transmittance are investigated for high-resolution and aperture ratio TFT-LCD panel. In conventional a-Si:H TFT active matrix arrays, silicon nitride has been used as the passivation layer on back channel etched (BCE) a-Si:H TFT device to protect it from contaminations. In this structure, the region which is covered by the pixel electrodes, gate and signal lines must be minimized as possible. Also, the inactive areas also need to be covered by black matrix (BM). These processes used on TFT devices decrease the transmittance and resolution significantly and make the brightness of TFT-LCD become much lower than the original light source. Thus, the pixel design to achieve the optimum aperture ratio requires the pixel electrode to be extended over the gate and data lines [1]. The passivation layer, which existed between the pixel electrode and the gate electrode, should be with low dielectric constant (*k*) and high transmittance in the visible light range. Conventional silicon nitride passivation layer becomes not suitable for BCE structure due to its relatively high dielectric constant ($k \sim 7$) and slow process rate. To lower the coupling capacitance which causes cross-talk and signal distortion and increase the brightness of TFT-LCD, the low dielectric constant (low-*k*) materials have been considered to replace the conventional silicon nitride passivation layer.

The approach to overcome the transmittance and cross-talk issues is to implement the low-*k* thick passivation layer located between the pixel electrode and data line [1,2]. Because of the low dielectric constant property, the low-*k* film can be thicker than silicon nitride film. By using low-*k* materials as the passivation layer, not only the problems of cross-talk and signal distortion can be solved, but also the

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interconnect RC time delay and mura on large panel for TFT-LCD can be improved. In this study, the low-*k* material ($k \sim 2.8$), siloxane-based hydrogen silsesquioxane (HSQ), which has high transmittance in the range of visible light and good electrical property has been investigated to replace the conventional nitride passivation layer. There is one more process advantage for using HSQ as the passivation layer: higher process efficiency. Compared with the silicon nitride deposited on devices by plasma-enhanced chemical vapor deposition (PECVD), HSQ spun on devices has higher and more effective deposition rate. Therefore, the throughput will be increased dramatically than previous ones. The HSQ film potentially combines the desired features of good adhesion, gap-filling, planarization, high Young's modulus, low coefficient of thermal expansion and non-etchback process [3–5]. As a result, HSQ has become one of the most suitable candidates to replace silicon nitride in the future.

2. Experimental procedure

Fig. 1 shows a schematic diagram of a gate planarized BCE a-Si:H TFT which used HSQ as the passivation layer. The BCE a-Si:H TFT consists of a bottom gate, a silicon nitride (SiN_x) gate insulator, undoped a-Si:H (i), phosphorus doped Si (n^+-Si) and source/drain electrodes. The processes are described as follows: first, aluminum metal was deposited on silicon oxide and a thin chromium layer was in-situ deposited on it by sputtering. The metal was photolithographically patterned for gate electrodes. Subsequently, SiN_x, undoped a-Si:H and n^+-Si layers were deposited continually on the gate in PECVD reactor. The thickness of SiN_x, a-Si:H and n^+-Si was 300, 180 and 40 nm, respectively. After the tri-layer was finished, the active region was defined by second photolithography process. The aluminum was deposited and the source/drain metal contacts were defined by the third photolithography. Finally, the low-*k* film, HSQ, was coated on the BCE a-Si:H TFT device as passivation layer.

The samples were spun coating with low-*k* HSQ at rotational velocity 2000 rpm for 20 s on a spin coater. Afterward, the HSQ film was baked sequentially on hot-plates in air at 150, 200, and 300 °C for 1 min, respectively. The resulting wafers were cured in a quartz furnace at 350 °C for 1 h under N_2 ambient. A metal/insulator/semiconductor (MIS) capacitor structure was used to study the electrical properties of HSQ film. HSQ was coated on a single crystal silicon wafer with 15–25 Ω cm with phosphorus doped. The process conditions are the same as the above processes for TFT device fabrication. At last, the electrode was deposited with aluminum. All the electrical measurements were performed by using a Hewlett–Packard (HP) 4156A semiconductor parameter analyzer.

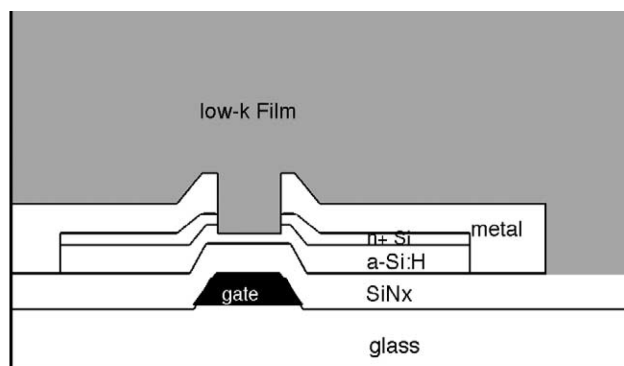

Fig. 1. The schematic diagram of the BCE a-Si:H TFT passivated by HSQ.

3. Results and discussions

HSQ is an inorganic polymeric material. The good performance of HSQ film for interlayer dielectric applications has been observed at the high Si–H bond density [6]. It is found that the thermal processing of HSQ must be executed carefully to guarantee good film properties [7]. In different curing temperatures, the stress in the film does not vary significantly (~65–75 MPa). For the dielectric film integrated on large area TFT arrays, thin film stress is a crucial parameter. The stress values are much lower than those of silicon nitride films which are deposited by PECVD. Therefore, as the influence of the thin film stress is considered, the HSQ passivation film is more suitable than silicon nitride film. The Fourier transform infrared spectra (FTIR) of HSQ films before and after a series of baking and curing steps are shown in Fig. 2. The important peaks that appeared in the FTIR spectrum of HSQ films are indicated as follows. The peak near 2250 cm^{-1} is identified as Si–H stretching bond. The Si–H group makes the surface hydrophobic and prevents the absorption of the moisture. In addition, Si–O stretching cage-like peak is near 1130 cm^{-1}; Si–O stretching network peak near 1070 cm^{-1}; Si–O bending cage-like peak near 860 cm^{-1}, and Si–O bending network peak is near 830 cm^{-1} [8–10]. After the baking processes, the FTIR spectra of HSQ are almost the same. After the curing process with 400 °C, however, the change of spectrum occurs in the chemical structure of HSQ films. The structure of the HSQ film changes from the cage-like structure to a network structure through the breakage of Si–O cage-like bonds and Si–H bonds. The network structure provides more sufficient mechanical integrity to withstand subsequent processes. However, the temperature control in TFT processes is an important factor, and refining the optimum recipe is an essential issue.

Fig. 3 shows the optical transmittance of HSQ films coated on the glass substrate. The optical properties are measured by ultraviolet visible spectrum. One bare glass substrate is employed as the reference sample to be the background for the measurement. As shown in the Fig. 3, it indicates that the HSQ films are almost optically transparent and its transmittance is over 90% in the visible light range. The transmittance does not show drastic variation in

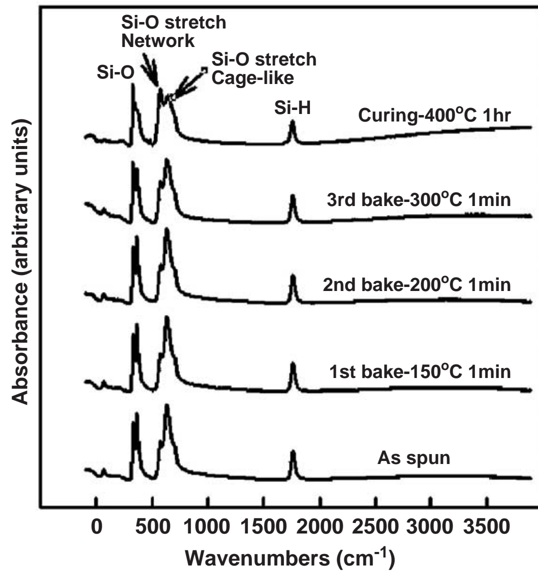

Fig. 2. FTIR spectra of HSQ before and after a series of baking and curing steps.

different temperatures which is an additional advantage of HSQ integrated on TFT devices. For the conventional silicon nitride film passivated on device, it cannot deposit too thick because the nitride film does not have high transmittance. However, when the low-*k* dielectric film is deposited as the passivation layer, it can be deposited over several micron to lower the RC time delay without sacrificing its transmittance. To make sure the leakage current of HSQ passivation film under illumination, a MIS capacitor structure is used to study the photo leakage current density of HSQ film. A 70-nm-thick metal gate Indium Tin Oxide (ITO) was deposited by sputtering and 500-nm-thick aluminum was deposited as the bottom electrode. Fig. 4

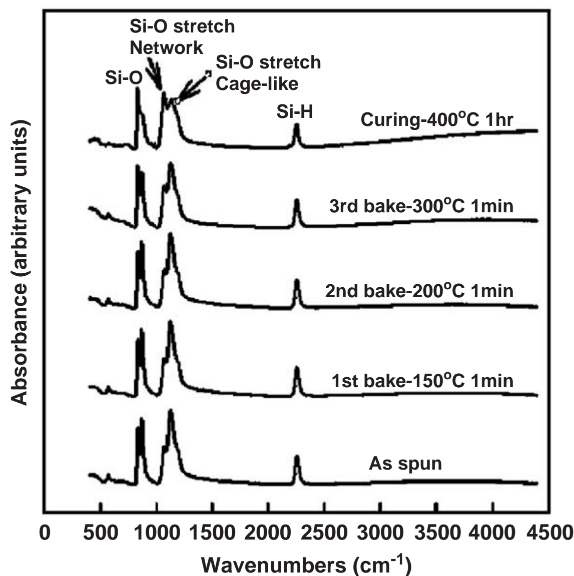

Fig. 3. The optical transmittance of HSQ dielectric film coated on glass substrate.

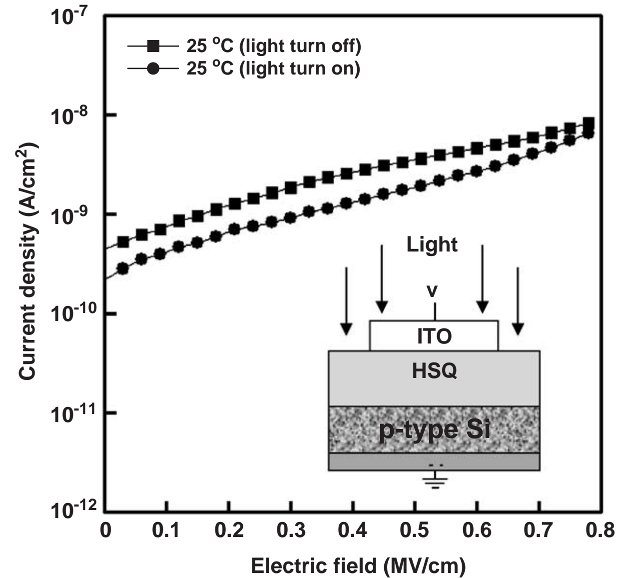

Fig. 4. The current density–electric field (J–E) curves of HSQ measured by under top illuminated by visible light at room temperature.

shows the current density–electric field (J–E) curves of HSQ which was under top illuminated by visible light at room temperature. In Fig. 4, the squares and circles exhibit the electrical properties of HSQ film under top illumination and in the dark, respectively. The photo leakage current is slightly increased after illumination which is induced by that the photons provide energy and the electrons are excited from valence band to conduction band, benefiting the generation of electron-hole pairs. It means that HSQ film is not sensitive under the entire visible light illumination. This is an essential property for low-*k* material applied on a-Si:H TFTs. In the aspect of illumination, HSQ film is very stable. Even if the temperature is increased, the photo leakage current does not significantly change.

Fig. 5 shows the I_d–V_g transfer curves compared with standard a-Si:H TFT and the HSQ passivated a-Si:H TFT

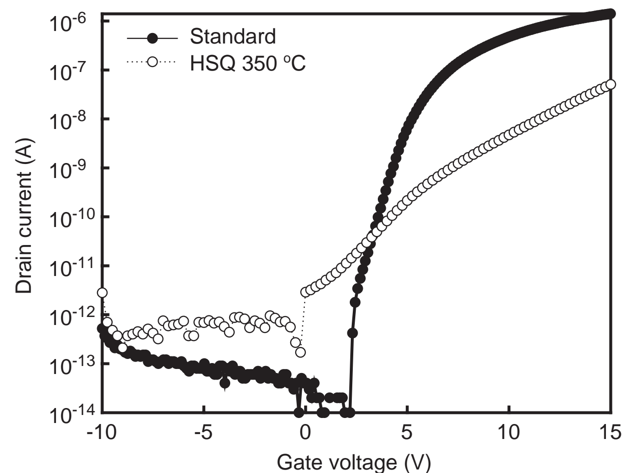

Fig. 5. The I_d–V_g transfer curves of standard a-Si:H TFT and the HSQ passivated a-Si:H TFT with 350 °C curing.

with 350 °C curing. The transfer curve in Fig. 5 shows the standard a-Si:H TFT is with good on/off ratio (>10^6) and the transfer curve of the HSQ passivation layer a-Si:H TFT with 350 °C curing exhibits a lower on-current, higher off-current and a higher threshold voltage. However, the HSQ passivation layer a-Si:H TFT still possesses the switch behavior with on/off ratio at about 10^5. The threshold voltage is higher than that of the standard a-Si:H TFT because the Si–H bonds of a-Si:H layer are broken by the temperature stress during the high-temperature HSQ curing. Thus, the traps are generated in the active channel. Fig. 6 compares the I_d–V_g transfer curves of standard a-Si:H TFT and the HSQ passivated a-Si:H TFT with 330 °C curing. The HSQ passivation layer under the 330 °C curing temperature has similar switch behavior as the standard a-Si:H TFT, and only the on-current is slightly degraded. It is deduced that the trap density at the active channel is decreased. The on/off ratio of 10^6 indicates the electrical performance of the TFT devices. By reducing the HSQ curing temperature, the I_d–V_g curves of HSQ with 330 °C curing exhibits the higher electrical characteristics than HSQ with 350 °C curing as shown in Fig. 5. Fig. 7 shows the I_d–V_g curves of the HSQ passivated a-Si:H TFT with 350 °C curing. It indicates that there is a current crowding effect which is caused by the trap density in the device. Also, the hydrogen bonds in a-Si:H channel are broken due to the high-temperature processes. The generation of dangling bonds near the source captures the electrons, leading to the current crowding effect. Thus, the phenomena exhibit that the a-Si:H TFT might be damaged by the temperature. Therefore, the most important issue is to lower the process temperature. The temperature stress reduces the on-current and deteriorates the characteristics of the device on its electrical performance and stability. Although the TFT with 330 °C cured HSQ has already performed good electrical characteristics, the optimum conditions for a-Si:H TFT device should be taken into account. However, if the curing process temperature is lowered drastically, the low-k films will have no sufficient mechanical integrity to protect the devices. Therefore, how to refine the optimum condition of the process temperature is one of the most important issues for a-Si:H TFT in the future.

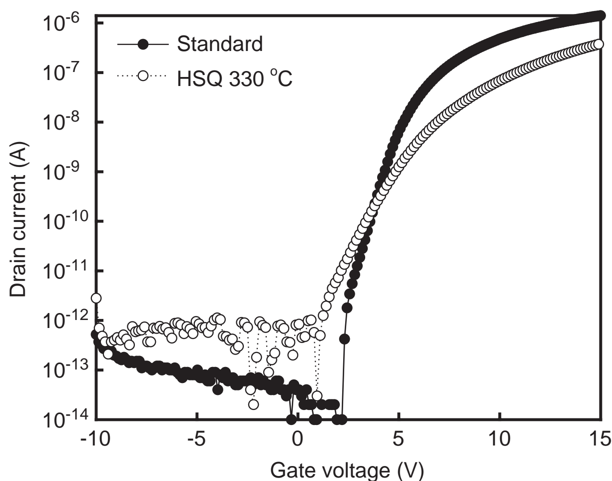

Fig. 6. The I_d–V_g transfer curves of standard a-Si:H TFT and the HSQ passivated a-Si:H TFT with 330 °C curing.

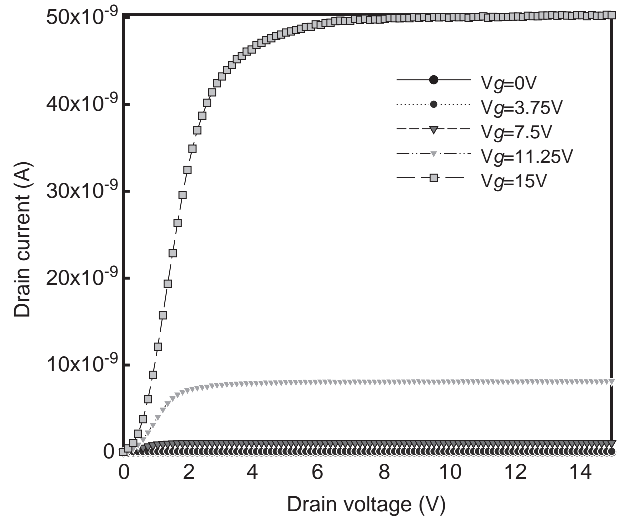

Fig. 7. The I_d–V_g curves of the HSQ passivated a-Si:H TFT with 350 °C curing.

4. Conclusion

Inorganic polymeric low-k material, HSQ, has been studied for integration as the passivation layer on a-Si:H TFT arrays in this study. HSQ is a potential candidate to replace conventional silicon nitride for its properties of low dielectric constant and high transmittance. Moreover, the other properties of HSQ, such as planarization, low film stress, good adhesion, gap-filling, high Young's modulus, low coefficient of thermal expansion, and non-etchback process are all suitable to be the passivation layer for high-performance BCE a-Si:H TFTs. Therefore, the problems such as cross-talk, signal distortion, interconnect RC delay and mura in TFT-LCDs can be improved by using HSQ passivation layer. The resolution and aperture ratio can also be promoted at the same time. Also, the process efficiency of HSQ spin-coating is much higher than conventional PECVD silicon nitride deposition. The approach, substituted the low-k film for PECVD nitride, improves the performance of a-Si:H TFT arrays and increases the throughput of the TFT-LCDs. Since the temperature in a-Si:H TFT-LCD fabrication is generally less than 300 °C, the fabrication conditions of HSQ should be fine-tuned to match the TFT devices in the future.

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