An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs With 1.6-nm Gate Oxide Near Room Temperature

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***Abstract*—This letter provides an assessment of single-electron effects in ultrashort multiple-gate silicon-on-insulator (SOI) MOSFETs with 1.6-nm gate oxide. Coulomb blockade oscillations have been observed at room temperature for gate bias as low as 0.2 V. The charging energy, which is about 17 meV for devices with 30-nm gate length, may be modulated by the gate geometry. The multiple-gate SOI MOSFET, with its main advantage in the suppression of short-channel effects for CMOS scaling, presents a very promising scheme to build room-temperature single-electron transistors with standard silicon nanoelectronics process.**

***Index Terms*—CMOS, coulomb blockade oscillation, multiple gate, silicon-on-insulator (SOI), single-electron effect, single-electron transistor.**

I. Introduction

TO ENABLE low-power electronics in the next generation, building single electron transistors (SETs) with standard silicon nanoelectronics process is a very attractive approach [1], [2], [6]. Especially, the SETs compatible with existing CMOS device architectures are potentially important for high-density memory cells. Table I lists several studies of silicon-based SETs with MOS structures, and reveals that downsizing the SET is essential to achieving the Coulomb blockade oscillation (CBO). The main challenges are the control of tunnel barriers [3], [4] and the suppression of short-channel effects [1]. Boeuf *et al.* [6] has demonstrated controlled single-electron effects using nonoverlapped extensions acting as tunnel barriers. M. Peters *et al.* [1] showed significant CBO using multiple-gate silicon-on-insulator (SOI) MOSFETs to overcome the short-channel effect. Although both studies represent attractive schemes to build SETs on large-scale wafers, the operating temperature is low (less than about 5 K).

To allow high-temperature operation, the size of the SET needs to be further reduced [1]–[7], [12]. The suppression of short-channel effects, therefore, is especially critical to enabling single-electron tunneling at elevated temperature in the scaled MOSFET. In this letter, we control the short-channel effect for devices with gate length down to 30 nm using thin oxide and multiple-gate SOI structures [9], [10]. Our device structure features nonoverlapped gate to source and drain. We conduct an assessment of single-electron effects in our multiple-gate SOI MOSFETs with 1.6-nm gate oxide near room temperature.

TABLE I
SEVERAL STUDIES ON SINGLE-ELECTRON EFFECTS IN MOS STRUCTURES

	this work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
type	N-Fin	N-Fin	N-SET	SET	N-SEQDT	Acc-SET	NP-Bulk	N-bulk
T_{ox} (nm)	**1.6**	25	**6**	30	25	10	**2~3**	**2.4~3.8**
L (nm)	**30**	200	**40**	**50~200**	**dot**	~100	**16~27**	**50~100**
W (nm)	**25**	100~500	**15**	**20**	**16**	>50	280	1000~400
H (nm)	**40**	100	**25**	**30**	**32**	**10**		
C_g (aF)	20~30	5.2	2	3~5	1.7	27	66	46~80
ΔV_g (mV)	17	~31	400	50~30	1400	6	9~6	3.5~2
Temp. (K)	**<300**	1.8	**<250**	**300**	**300**	<10	<5	<5
lithography	**optical**	E-beam	E-beam	E-beam	E-beam	E-beam	**optical**	

II. Devices

Our transistors, as shown in Fig. 1, were fabricated on p-type SIMOX SOI wafers using optical lithography as described in [10]. The Si-body thickness, $H_{\rm fin}$, was thinned down to about 40 nm by thermal oxidation. The fin-width, $W_{\rm fin}$, was defined by wet-etching and is about 25 nm. After $W_{\rm fin}$ was developed, the 1.6-nm gate oxide was thermally grown. The ultra-thin gate oxide contributes to not only the suppression of short-channel effects, but also the gate-dot coupling strength of the SET [2].

The gate length L_g was defined by *in situ* heavily doped n^+ poly-silicon gate and ranges from 30 to 40 nm. Without the light doping drain (LDD) implantation, the composite spacer of silicon oxide and nitride was deposited and anisotropically etched. The undoped regions under the spacers separate the inversed carriers from source/drain and act as electrostatic tunnel barriers as depicted in Fig. 1. Finally, heavily-doped n^+ source/drain was made. It is worth noting that the parasitic source/drain resistance, which may determine the tunnel barrier [5], depends on $H_{\rm fin}$ and $W_{\rm fin}$ in this multiple-gate SOI structure.

III. Results and Discussions

Fig. 2 shows the G_m–V_G characteristics measured by HP4156B in a low-noise probe station at room temperature ($T = 20^{\circ}$C) for the device with $L_g = 30$ nm and $W_{\rm fin} = 25$ nm. Periodic oscillations in G_m, an indication of the CBO [2], [4], [8], [13], can be seen starting from $V_G \sim 0.2$ V.

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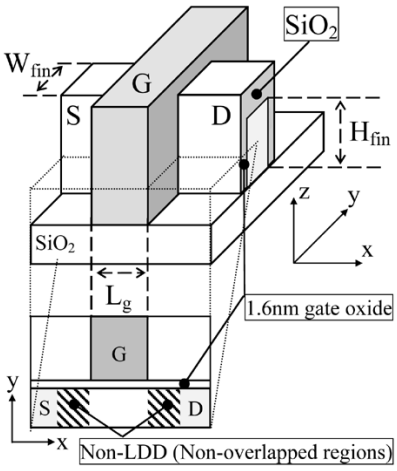

Fig. 1. Multiple-gate FinFET SOI structure investigated in this work and its cross-sectional view along the channel direction showing the nonoverlapped gate to source/drain regions.

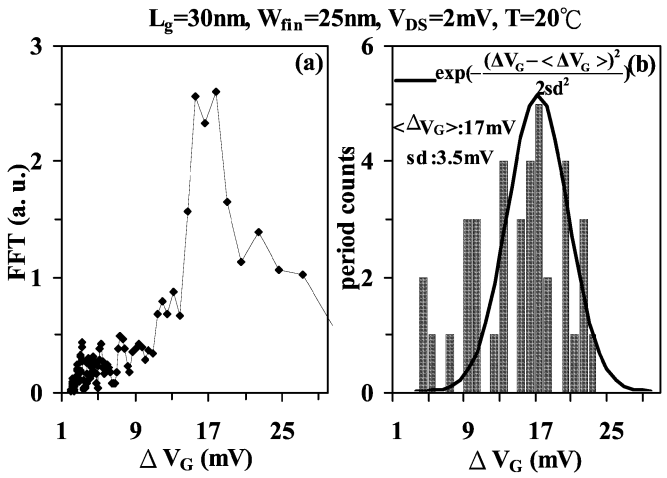

Fig. 3. Both (a) the fast Fourier transform (FFT) and (b) the histogram of the directly counted peak-to-peak spacing (ΔV_G) confirm that the period in Fig. 2 is 17 mV.

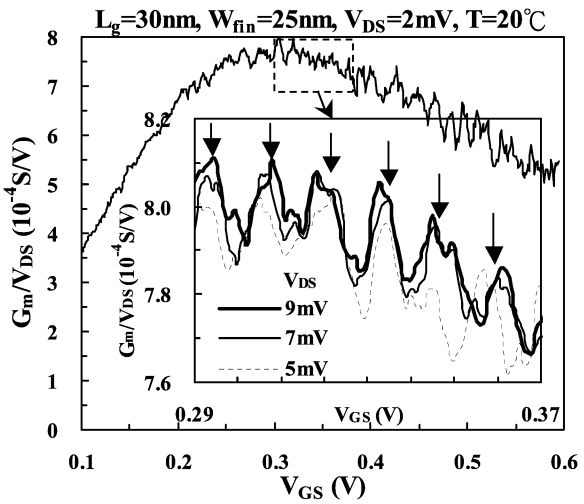

Fig. 2. Periodic oscillations occur in G_m/V_{DS} vs. V_{GS} for the device with $L_g = 30$ nm and $W_{\text{fin}} = 25$ nm at $T = 20\,^{\circ}$C. G_m is extracted by dI_D/dV_G and shows a period of 17 mV.

For an SET, the ability to produce CBO at low gate bias is important to low-power applications [2]. We have also noted that the periodic oscillations can be reproduced from sample to sample, and the peaks of each period for the same device may be repeated at the same gate bias. It can be seen from the inset of Fig. 2 that the oscillating period is about 17 mV. For devices with large dimensions under the same measurement system, nevertheless, only the thermal noise can be seen. In addition, we have confirmed that the effect of source accuracy [16] is not responsible for the observed periodic oscillation.

To further analyze the periodic oscillation in G_m, both the discrete fast Fourier transform (FFT) [11] and the histogram of the directly counted peak-to-peak spacing (ΔV_G) [5], [6] in the G_m–V_G characteristics can be applied. The power spectrum density of FFT, shown in Fig. 3(a), may represent the intensity of the corresponding periodic signal plus the period counts of ΔV_G [Fig. 3(b)]. It can be confirmed from Fig. 3 that the observed conductance oscillation in Fig. 2 indeed has a period of 17 mV.

The period of conductance oscillation, ΔV_G, represents the charging energy and is related to the gate capacitance by e/C_g [12], [20]. From $e/C_g = 17$ mV and the gate capacitance per unit area $\left(C_g/A_{\text{eff}} \sim 1.3 \times 10^{-6}\ \text{F/cm}^2\right)$, we may deduce an effective area of the dot, $A_{\text{eff}} \sim 7.1 \times 10^{-12}\ \text{cm}^2$, which is about a factor of three smaller than the total gate area of our FinFET device $\left(2H_{\text{fin}}L_g = 24 \times 10^{-12}\ \text{cm}^2\right)$. Note that similar discrepancy has also been observed in [6]. Besides uncertainties of process control in very small geometries, the discrepancy between the deduced effective area (A_{eff}) and the total gate area of our device ($2H_{\text{fin}}L_g$) may stem mainly from the junction capacitance [14], [15]. In other words, the quantum dot in our device may no longer be considered as a disk-like island but rather a three-dimensional box. In addition, the shape of this three-dimensional box may be deformed by V_G because the tunnel barriers may be electrostatically modulated by V_G. Therefore, the oscillating period, ΔV_G, is a distribution instead of a fixed value. As shown in Fig. 3(b), our measured ΔV_G can be described by Gaussian distribution [6], [17]–[19] with $\langle \Delta V_G \rangle \sim 17$ mV and sd~ 3.5 mV ($\langle \Delta V_G \rangle$: mean, sd: standard deviation). Moreover, the normalized width of the distribution, sd$/\langle \Delta V_G \rangle$, is about 0.2. Similar results have also been obtained in [6] and [19].

Fig. 4 shows the G_m–V_G characteristics for the device with $L_g = 40$ nm and $W_{\text{fin}} = 25$ nm at $T = 20\,^{\circ}$C. The phenomenon of G_m oscillation can still be seen. Moreover, we have noted that the oscillating period, ΔV_G, is about 15 mV, as shown in the inset of Fig. 4, for all the devices with this size. Compared with the 17-mV period for $L_g = 30$ nm (Fig. 3), the decreased ΔV_G for $L_g = 40$ nm may be attributed to the increased C_g. This geometrical dependence of charging energy indicates that the observed single-electron effect is controlled by the gate geometry rather than the disordered potential landscape demonstrated in the multiple-gate SOI structures of [1].

IV. Conclusion

We have conducted an assessment of single-electron effects in ultrashort multiple-gate SOI MOSFETs with 1.6-nm gate

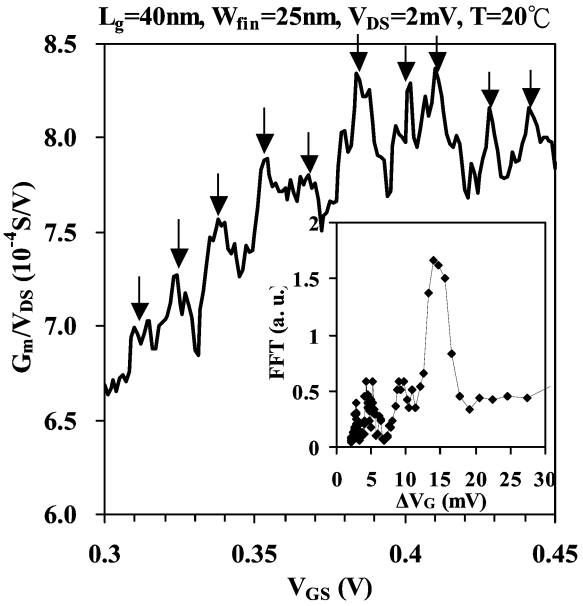

Fig. 4. Periodic oscillations occur in G_m/V_{DS} versus $V_{\rm GS}$ for the device with $L_g = 40$ nm and $W_{\rm fin} = 25$ nm at $T = 20$ °C. Smaller peak-to-peak spacing ($\Delta V_G = 15$ mV) from the FFT can be seen.

oxide. Coulomb blockade oscillations have been observed at room temperature for gate bias as low as 0.2 V. The charging energy may be modulated by the gate length of the MOSFET. The multiple-gate SOI structure, with its main advantage in the suppression of short-channel effects for CMOS scaling, presents a very promising scheme to build room-temperature single-electron transistors with standard silicon nanoelectronics process.

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