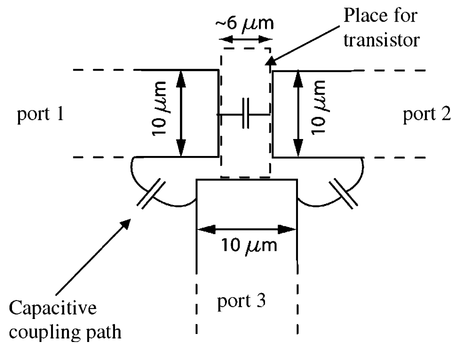

Fig. 3. Detailed view of test fixture DUT gap area in the proposed test fixture [1]. The above illustration is drawn based on the physical dimensions given in [1].

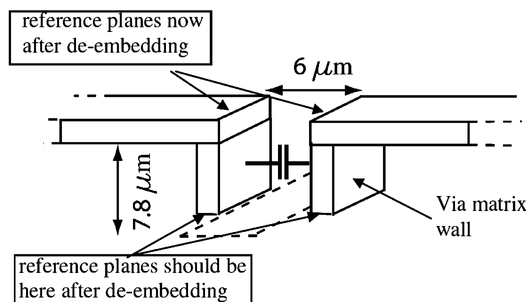

Fig. 4. Detailed view of the vertical via walls. The third port is not included in the illustration.

There are three capacitive coupling paths drawn in Fig. 3. When each port is treated individually, as is the case in the proposed de-embedding method [1], all of these three coupling paths caused by the test fixture itself are neglected. Furthermore, the authors have not described the connections between signal trace ends and the transistor. As mentioned in [1], the signal traces are 7.8 μm above the silicon substrate. Therefore, several via layers are required (from metal 6 to metal 1) in order to connect the tips of the signal traces to the transistor terminals (gate, drain, and source). We have sketched part of these via connections in a detailed view shown in Fig. 4. The via matrix causes vertical walls at the end of the signal traces, as shown in Fig. 4. Typically the width of the vertical via matrix wall is equal to the signal trace width. In this case, it is assumed that 10-μm-wide and 7.8-μm-high via matrix walls are implemented in each port. The reason why a signal-trace-wide via matrix should be employed is to minimize the series resistance caused by the vias. However, these vertical walls again increase the coupling between ports. Thus, it is emphasized that the measurement reference plane after de-embedding should be at the transistor terminals and not 7.8 μm above, at the tips of the signal traces, as indicated in Fig. 4.

Consequently, we cannot say how great an error is possibly caused by neglecting the coupling between signal trace tips and the additional coupling due to the vertical via matrix walls. We do not have experimental data concerning the increased (if any) forward coupling due to coupling between tips of the signal traces. Thus, we suggest making additional measurements employing an open device with signal traces in order to check the validity of the assumption regarding the negligible port coupling. The additional coupling could be, for example, extracted by applying the proposed de-embedding method to a ground-shielded test fixture without a transistor.

III. Method Comparison

It would have been interesting to make a comparison between the conventional two-port cascade-based de-embedding method and the proposed three-port cascade-based de-embedding method employing shield-based test fixtures in a "conventional way." This would have required an additional ground-shielded *two*-port test fixture with an embedded DUT transistor for the conventional de-embedding method. The authors of [1] have shown that we cannot ignore the third port parasitic components (the dangling leg connected to transistor source) of the three-port test fixture. This is obvious since the third port is similar to the other two in the proposed three-port test fixture. That is why it has the same parasitic components as well, which have to be taken into account. However, when we employ the conventional two-port cascade-based de-embedding method with ground-shielded two-port test fixtures, the source of the transistor is connected directly to the test fixture ground plane. Shield-based test fixtures reduce dangling leg impedance significantly [2]. Thus, the dangling leg problem described in the first paragraph of [1, Sec. II] could perhaps have been solved by just changing the test fixture type from unshielded to ground shielded. At least this kind of comparison would have given a new perspective and information about the dangling leg parasitic components of the ground-shielded test fixture. Perhaps the three-port de-embedding method would have given a still better result. The source of the transistor under study in [1] was biased to 0 V, which would have made it possible to carry out this suggested comparison.

References

[1] M.-H. Cho, G.-W. Huang, L.-K. Wu, C.-S. Chiu, Y.-H. Wang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu, "A shield-based three-port de-embedding method for microwave on-wafer characterization of deep-submicrometer silicon MOSFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2926–2934, Sep. 2005.
[2] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1039–1044, Jun. 2001.

Author's Reply

Ming-Hsiang Cho

I would like to thank Kaija and Heino for their comments on the above paper [1]. Below are some replies to their comments.

A. Proposed Method

Kaija and Heino propose a new test and dummy fixture set for use with a cascade-based three-port de-embedding method [1]. The test fixture is based on the three-port fixture presented in [2]. Both test fixture and dummies do not have ground bars and all signal traces have the same length. In my opinion, these proposed test fixture and dummies without ground bars can indeed simplify the layout process

Manuscript received December 23, 2005.
The author is with National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. and also with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mhcho@mail.ndl.org.tw).
Digital Object Identifier 10.1109/TMTT.2006.869699

0018-9480/$20.00 © 2006 IEEE

of the on-wafer test structures, even if they may have the same results with those previously reported. In addition, they also suggest that the three-port test fixture can be designed with the same interconnect length. Therefore, only one open and thru dummy fixtures are needed and the die area is significantly reduced. This concept basically agrees with our new idea presented in [3]. This new de-embedding method is scalable, i.e., can be used to subtract the redundant parasitics of the test fixture with arbitrary interconnect length and, thus, also results in a large chip-area saving.

B. Method Comparison

Although the shield-based technique can significantly reduce dangling impedance [2], the parasitic effects of shielded dangling leg, especially the capacitive parasitics, would become considerable at microwave frequencies and should be also taken into account in the de-embedding procedure. Hence, the shield-based three-port de-embedding method [1] has been developed to eliminate the dangling parasitics. If the multiport S-parameters measurement system is unavailable, one can use another de-embedding method [4] to subtract the dangling parasitics through the two-port to three-port transformation for S-parameters.

References

[1] M.-H. Cho, G.-W. Huang, L.-K. Wu, C.-S. Chiu, Y.-H. Wang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu, "A shield-based three-port de-embedding method for microwave on-wafer characterization of deep-submicrometer silicon MOSFET's," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2926–2934, Sep. 2005.

[2] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1039–1044, Jun. 2001.

[3] M.-H. Cho, G.-W. Huang, C.-S. Chiu, and K.-M. Chen, "Unified parasitic de-embedding methodology of on-wafer multi-port device characterization," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 1307–1310.

[4] M.-H. Cho, C.-S. Chiu, G.-W. Huang, Y.-M. Teng, L.-H. Chang, K.-M. Chen, and W.-L. Chen, "A fully-scalable de-embedding method for on-wafer S-parameter characterization of CMOS RF/microwave devices," in *IEEE RFIC Symp. Dig.*, Jun. 2005, pp. 303–306.

Comments on "A Comprehensive Study of Discontinuities in Chirowaveguides"

Miguel A. Solano, Angel Vegas, and Álvaro Gómez

The above paper [1] presents a study of two- and three- dimensional discontinuities in chirowaveguides. Their study is an extension of the formulation developed by Chaloupka [2] for rectangular waveguides containing vertical ferrite slabs. The formulation in [2] is a multimode coupled mode method (CMM) extended from the analysis of straight waveguides to the analysis of discontinuities in the propagation direction. The CMM is, basically, a method of moments (MoM), which uses the modes of an empty waveguide (in this case, a rectangular waveguide with perfect electric conductor (PEC) walls) as base functions. The goal of the CMM is to obtain the electromagnetic field of the modes in a waveguide with a PEC contour containing any kind of nonconducting medium, irrespective of whether it is isotropic, anisotropic, or bi-anisotropic. We use the term *proper* modes to designate such modes. This leads to an inevitable fact: the boundary conditions on the PEC walls for the electromagnetic field of the base modes are the same as those for the proper modes of the waveguide containing the dielectric media. As is known, in the CMM, only two of the electromagnetic fields of the proper modes have to be expanded in terms of the electromagnetic field of the base modes. In [1], as in [2], the fields to be expanded are the electric field $\vec{E}$ and magnetic field $\vec{H}$. For both fields, when an isotropic medium is in contact with a PEC wall, the boundary conditions are the same for both base and proper modes. In particular, in this case, the normal component of $\vec{H}$ on the PEC is zero for all base and proper modes. The same is true for the tangential components of $\vec{E}$ on a PEC wall. However, if the material in contact with a PEC wall is, for instance, a chiral medium, the normal component of the magnetic field $\vec{H}$ of a base mode is zero on the PEC, but it is different from zero for any proper mode. Therefore, strictly speaking, the magnetic field $\vec{H}$ of any proper mode obtained with the approach in [1] is erroneous because its normal component is zero on the PEC, whereas it should be different from zero. Besides considering the accuracy of the results for the propagation constants and the scattering parameters provided by the type of formulation used in [1], we think that this very important fact of this formulation should have been pointed out in [1].

The situation described above can be overcome in several different ways. Perhaps the most intuitive would be to expand those fields that fulfill the same boundary conditions on a PEC wall for both base and proper modes, irrespective of the kind of medium in contact with the PEC. These fields are $\vec{E}$ and $\vec{B}$. Such a formulation (which we call an EB formulation in contrast to the classical one, which is called an EH formulation) for a parallel-plate waveguide partially filled by slabs of chiral media can be seen in [3]. Reference [3] also shows a comparison between results for the propagation constant as a function of the number of base modes for EB and EH formulations. In [4], there is a good discussion of EH and EB formulations (which these authors call

Manuscript received November 14, 2005. This work was supported by the Dirección General de Investigación of the Spanish Ministerio de Educación y Ciencia under Project TIC2003-09677-C03-01.

M. A. Solano and A. Vegas are with the Departamento de Ingeniería de Comunicaciones, Escuela Técnica Superior de Ingenieros Industriales y de Telecomunicación, Universidad de Cantabria, 39005 Santander, Cantabria, Spain (e-mail: solanom@unican.es).

Á. Gómez is with the Departamento de Electricidad y Electrónica, Facultad de Ciencias, Universidad de Valladolid, 47011 Valladolid, Spain.

Digital Object Identifier 10.1109/TMTT.2006.869696

0018-9480/$20.00 © 2006 IEEE