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Oxide-mediated formation of epitaxy silicide on heavily doped Si surfaces and narrow width active region

Yen-Ming Chen [a], George C. Tu [a], Ying-Lang Wang [b,*]

[a]Department of Materials Science and Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, ROC
[b]College of Science and Engineering, National University of Tainan, Taiwan

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Abstract

Oxide-mediated epitaxy (OME) is a highly promising means of forming epitaxial $CoSi_2$. In this work, various chemical treatments were applied to grow chemical oxides on heavily doped Si substrates and narrow width active region. The effects of the treatment on the OME performance were investigated. Both the thickness and the quality of the oxide varied with the chemicals and dopants, resulting in various levels of junction leakage current. The junction leakage current was minimized by choosing the most favorable chemical treatment and optimizing the annealing temperature.
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Keywords: Oxide-mediated epitaxy; Silicide; Junction leakage

1. Introduction

The formation of a reliable, low-resistance and shallow silicide contact on complementary metal–oxide–semiconductor (CMOS) devices is a challenge in the manufacture of deep sub-micron ultra large-scale integrated (ULSI) circuits. As the depth of the junction is reduced to less than 0.1 μm, the thickness of the silicide layer must be kept under 30 nm. Good silicide uniformity and a smooth silicide/Si interface are required to ensure that the junction leakage current is low. Cobalt silicide ($CoSi_2$) has attracted much attention in the field of sub-micron CMOS technology because it has better characteristics than other silicides such as $TiSi_2$ [1]. Beyond having a low resistivity of 10–18 μΩ cm and the excellent chemical stability [2] ,$CoSi_2$ grows epitaxially on Si because its has a similar lattice structure to Si (CaF_2) and a small lattice mismatch (~ 1.2%) with Si at room temperature. However, single-crystal epitaxial $CoSi_2$ cannot be formed with simple deposition and annealing on most of Si surfaces, except on a (111) Si surface [3]. Therefore, many methods of improving the epitaxy of $CoSi_2$ on Si surfaces have been developed. Titanium-interlayer-mediated epitaxy (TIME) [3] oxide-mediated epitaxy (OME) [4] and high-temperature sputtering (HTS) [5] can improve epitaxy. Among these techniques, OME is compatible with general semiconductor processes because of the simple process requirement.

Epitaxial cobalt silicide has a smoother interface than silicon and a much higher thermal stability [6,7]. However, the dopants implanted in the Si layer seem to influence strongly the properties of silicide [8,9]. In this work, the effects of the dopant species and the various chemical oxides on the electrical characteristics of cobalt silicides are investigated.

2. Experiments details

A boron-doped, p-type Si blanket wafer with a resistivity of 10 Ω cm with an (001) orientation was used as the substrate in this work. Heavy N-type and P-type dopants were implanted into the Si substrate and then high-temperature spike rapid thermal annealing was performed (RTA). Three different chemical species – ozone(50 °C), APM ($NH_4OH/H_2O_2/H_2O = 1:5:25$, 70 °C) and HPM ($HCl/H_2O_2/$

* Corresponding author. Tel.: +886 6 505 9688; fax: +886 6 5051262.
E-mail address: ylwang@tsmc.com (Y.-L. Wang).

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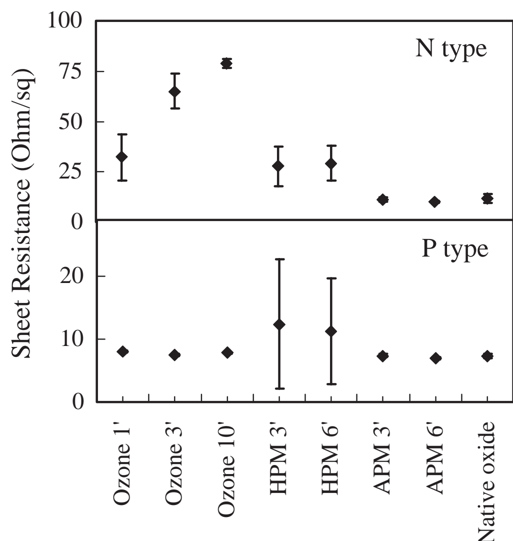

Fig. 1. The sheet resistance with different chemical treatments and process time on heavy doped N^+ and P^+ wafers.

H_2O = 1 : 1.5 : 4, 60 °C) – were used to form chemical oxide layers before cobalt sputtering to study the effect of quality of the chemical oxide on the OME. The different process time for each chemical species were also applied for sample preparation. A 160 Å titanium (Ti) cap was sputtered after 110 Å of cobalt (Co) was deposited without breaking a vacuum. Various annealing temperatures were applied after Co and Ti were deposited; then, selective etching was applied to remove any un-reacted Co or Ti. The sheet resistance of the silicide was measured using a 4-point probe.

Another experiment was done on ultra-high density integrated circuit wafers according to the observation from above blanket wafers experiment. Ozone 1 minute and APM 3 minutes chemical treatments were selected to applied on 85 nm CMOS devices. Shallow trench isolation (STI) was used with an active region width from 2 μm to 0.1 μm, to evaluate the line width effect. N^+ source/drain and P^+ source/drain were fabricated by implanting arsenic/phosphorus and boron, respectively. Spike rapid thermal annealing (RTA) was then performed to activate the implanted species. After treatment with various chemicals, Ti/Co were sputtered, and RTA was conducted at a temperature of 500, 520 or 540 °C. Subsequently, selective etching was used to remove un-reacted Ti; the samples were then annealed by 2nd RTA at 860 °C for 35 s. Lithography and etching were applied to define the contact layer after the inter-layer dielectric layer had been formed by chemical vapor deposition. Finally, copper metallization was performed.

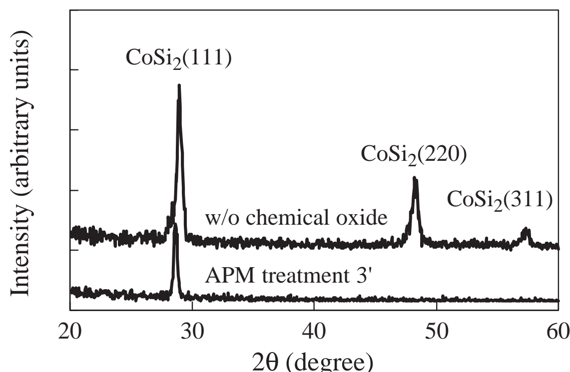

Fig. 2. X-ray diffraction patterns for without chemical oxide (native oxide) and with APM treatment for 3 min.

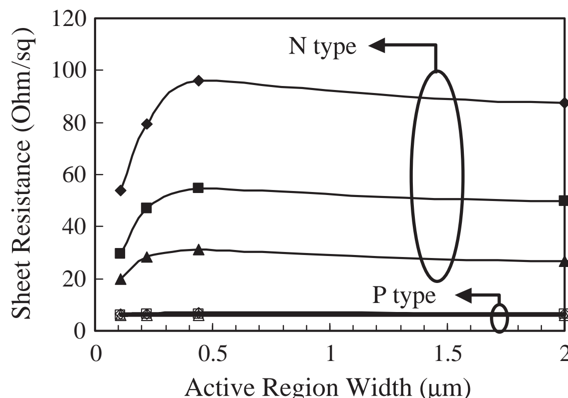

Fig. 3. Sheet resistance of active region treated by 1 min of ozone (N-type: (♦) 500 °C, (■) 520 °C, (▲) 540 °C; P-type: (◇) 500 °C, (□) 520 °C, (△) 540 °C).

3. Results and discussions

The sheet resistance of silicided N^+ and P^+ blanket wafers was measured after the second RTA. Fig. 1 plots the changes of the sheet resistance when different chemicals and the process time the process time for both heavily doped N^+ wafers and P^+ wafers. On the heavily doped N^+ wafers, the sheet resistance changed significantly with the process time in ozone, but not in APM or HPM. When the process time was short (1 min) in ozone, the sheet resistance even exceeded that associated with a longer treatment time in APM/HPM. Ozone treatment is believed to generate a

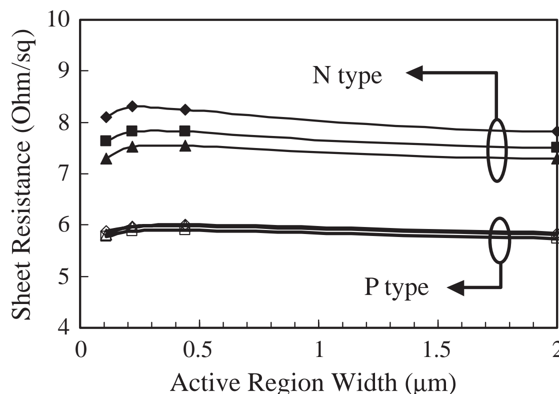

Fig. 4. Sheet resistance of active region treated by 3 min of APM (N-type: (♦) 500 °C, (■) 520 °C, (▲) 540 °C; P-type: (◇) 500 °C, (□) 520 °C, (△) 540 °C).

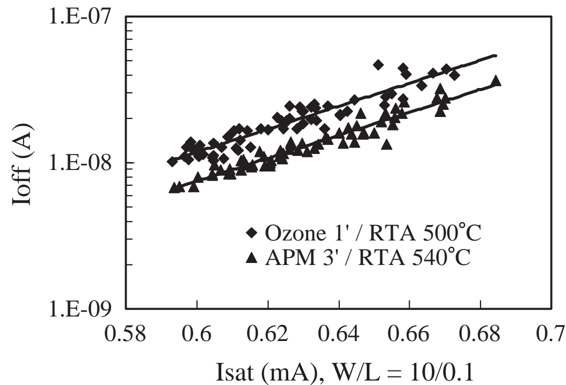

Fig. 5. The I_{sat}–I_{off} measurement on NMOS processed by different chemical oxide.

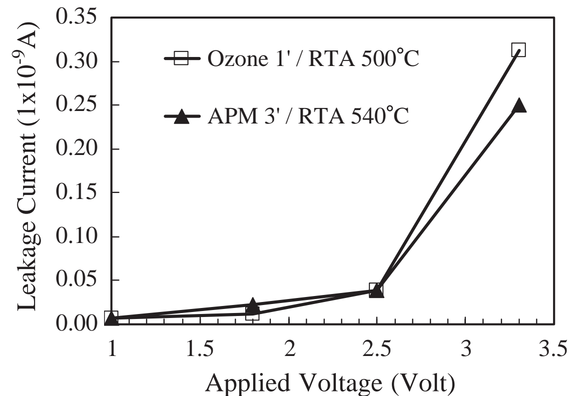

Fig. 7. Junction leakage on N-type finger-type active region.

thicker oxide film on N^+ heavily doped wafers than on wafers treated with HPM/APM. Notably, the sheet resistance was not uniform after HPM treatment. Bardwell et al. also found that the uniformity of the oxide on the Si wafer was poor when the process time in HPM was short [10]. The poor oxide uniformity on the HPM-treated wafer resulted in the large variation for the sheet resistance. APM offered the lowest sheet resistance and best uniformity. After chemical treatment, the sheet resistances differed less on the P^+ wafer than on the heavily doped N^+ one, that indicated the thickness of oxide produced on P^+ are similar among different chemicals. This phenomena is consistent with the observation in previous study [10]. The X-ray diffraction patterns in Fig. 2 reveal the difference between the orientations of the samples that had and had not been treated with chemical oxide. Unlike the untreated sample, the wafer treated for 3 min with APM exhibited only the $CoSi_2$ (111) orientation. This finding is consistent with that of a previous investigation [11]. The single orientation demonstrates the success of epitaxial $CoSi_2$ formation and the smoothness of the $CoSi_2$/Si interface.

APM and ozone treatment were applied to the CMOS process to check their effects on the sheet resistance in the narrow active region, the specific contact resistance and the junction leakage. The first RTA temperature for forming silicide was also studied to optimize OME process and to obtain uniform sheet resistance and low junction leakage. Fig. 3 shows the effect of 1 min of ozone treatment on the sheet resistance of heavily doped N^+ and P^+ active regions. The sheet resistance is much higher on the N^+ active region than on the P^+ active region. This result is consistent with the observation of the blanket wafers. The thick chemical oxide on the N^+ active region suppresses the formation of silicide, even at the first RTA temperature of 540 °C. The lower sheet resistance on the narrower active region reveals that the oxide thickness is thinner at narrow active region. The retarded oxidation by compressive stress was reported by Kao et al. [12]. The oxide thickness on active region around STI corner is thinner than planar area because of the compressive stress produced by STI. The oxide thinning at active region corner makes the oxide thickness thinner for small active region than large active region.

After APM treatment, the sheet resistance on the N^+ active region is comparable with that of the P^+ active region, as presented in Fig. 4. The saturation (I_{sat}) and off (I_{off}) current of the NMOS devices with a gate length of 0.1 μm were measured to understand the impact of the formation of silicide on the electrical properties. Fig. 5 shows that the I_{sat}–I_{off} curve was degraded by 4% when ozone-treated chemical oxide was applied. As the MOS shrinks to the sub-micron scale, the intrinsic parasitic series resistance substantially affects the speed of the device [13]. An important part of the parasitic series resistance is the specific contact resistance. The specific contact resistance was measured on

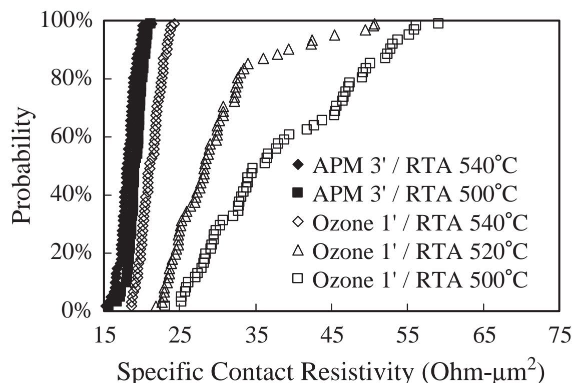

Fig. 6. Specific contact resistance for different chemical treatment substrate.

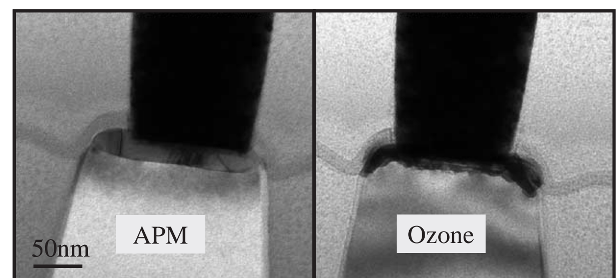

Fig. 8. TEM cross-section for APM and ozone treatment process on N^+ active region.

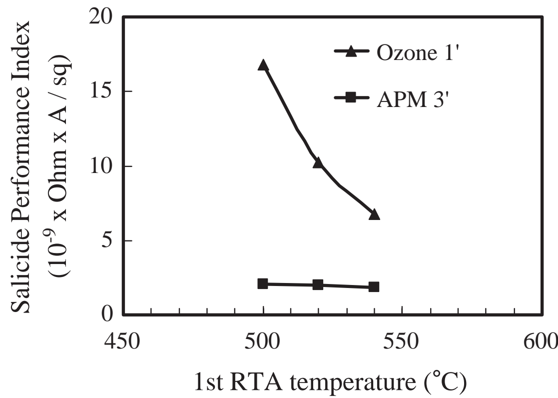

Fig. 9. The silicide selection index.

the modified Kelvin structure, as reported by Lynch and Ng, to confirm that the poor formation of silicide on the ozone-treated surface contributed to the degradation of the device [14]. Fig. 6 clearly indicates that the poor specific contact resistance induced by the poor formation of silicide degrades the device.

Junction leakage control is also crucial for deep sub-micron CMOS devices, especially those used in low power applications. Fig. 7 plots the junction leakage measured on the N-type STI edge intensive test pattern (periphery is about 6 mm) with different applied voltage. Under 3.3 V stress, the leakage current for APM 3 min/540 °C RTA wafer is lower than that of ozone 1 min/500 °C RTA wafer. The higher sheet resistance and the higher junction leakage of the 1 min ozone-treated wafer indicate that the silicide/Si interface obtained by ozone treatment is rougher than that obtained by APM treatment. Fig. 8 displays the TEM cross-sections of the N^+ active regions on both APM- and ozone-treated wafers. The Si/silicide interface associated with the APM treatment process is clearly smoother than that of the ozone treatment process. The smooth interface provides better junction leakage performance and is very important to the manufacture of nano-scaled devices. Fig. 9 shows the index for silicide selection. The multiple of sheet resistance and junction leakage current by 3.3 V test was used as the index. Low sheet resistance and junction leakage current are both important factors for nano-scaled devices fabrication. According to this index, the APM treatment process showed superior performance to the ozone treatment process for future deep sub-micron device need.

4. Conclusion

The effect of chemically treating the wafers on OME cobalt silicide was investigated. Different heavily doped Si surfaces were also considered. APM treatment provides the best control of the sheet resistance and junction leakage than other chemical treatments. Low sheet resistance and junction leakage current can be obtained by optimal chemical treatment and the use of an optimal RTA temperature.

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