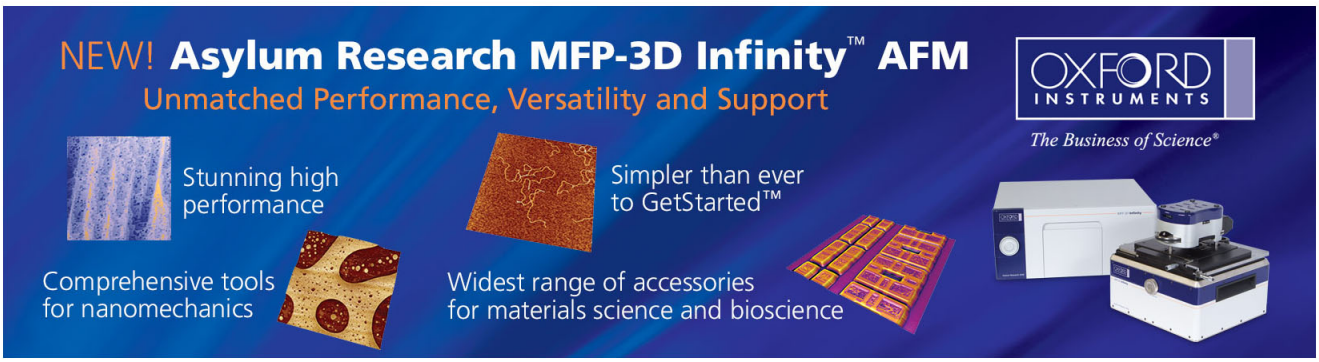
Complementary carbon nanotube-gated carbon nanotube thin-film transistor

Bae-Horng Chen, Horng-Chih Lin, Tiao-Yuan Huang, Jeng-Hua Wei, Hung-Hsiang Wang, Ming-Jinn Tsai, and Tien Sheng Chao

Citation: Applied Physics Letters **88**, 093502 (2006); doi: 10.1063/1.2179612
View online: http://dx.doi.org/10.1063/1.2179612
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/88/9?ver=pdfcov
Published by the AIP Publishing



Complementary carbon nanotube-gated carbon nanotube thin-film transistor

Bae-Horng Chen, Horng-Chih Lin, and Tiao-Yuan Huang
Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

Jeng-Hua Wei
Department of Electronic Engineering of Ching Yun University, Jung-Li 229, Taiwan

Hung-Hsiang Wang and Ming-Jinn Tsai
Electronics Research and Service Organization (ERSO), ITRI, Hsinchu 310, Taiwan

Tien Sheng Chao[a)]
Department of Electrophysics, National Chiao Tung University, Hsinchu 300, Taiwan

(Received 11 July 2005; accepted 18 January 2006; published online 27 February 2006)

We introduce, a complementary carbon nanotube (CNT)-gated CNT thin-film field effect transistor (FET). By using two perpendicularly crossed single-wall CNT (SWNT) bundles as the gate and the channel interchangeably, a sub-50 nm complementary CNT-FET is demonstrated. It is found that the new CNT-FET shows acceptable FET characteristics by interchanging the roles of the gate and the channel. The unique dual functionality of the device will open up a new possibility and flexibility in the design of future complementary CNT electronic circuits. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2179612]

Single-wall carbon nanotube (SWNT) is an ideal candidate for future nanoelectronics because of its small diameter, high current-carrying capability, and high conductance in a one-dimensional nanoscale channel. The carbon nanotube (CNT) field effect transistor (FET) and several related logic gates have been fabricated by using semiconducting-type CNTs (Refs. 1–3) as the building block, and the CNT-FET shows superior electrical properties over the conventional silicon metal-oxide-semiconductor field effect transistor (MOSFET). Although these CNT-FETs feature a small channel width, the gate length is usually larger than 100 nm which is limited by the lithography process.[3]

Previously, our group manufactured *n*-type (Refs. 4–6) and *p*-type CNT-FETs without resorting to any additional and complex annealing process (Table I). In this study, a complementary CNT-gated CNT-FET (CG-CNT-FET) structure is proposed and demonstrated. Without relying on electron-beam lithography, the gate length and the gate width of CNT-FET are easily shrunk to 20–50 nm or less. This is achieved by using two perpendicularly crossed SWNT bundles as the interchangeable channel and gate. The new CG-CNT-FET shows either *n*- or *p*-type FET characteristics, depending on whether the bottom CNT bundle (CNT1) or the top CNT bundle (CNT2) is used as the channel, with the other CNT bundle acting as the gate. After interchanging the roles of the gate and the channel, the upsidedown device still shows good FET characteristics. Detailed operation principles will be explained next.

The key fabrication process of the dual-functionality CG-CNT-FET is as follows: Briefly, a 600 nm SiO_2 field oxide layer was first grown by wet oxidation at 985 °C on 4 in. *p*-type silicon wafer. Then, a 100 nm Ti layer was deposited by radio-frequency (rf) sputtering, and subsequently patterned and etched to serve as the source/drain metal pads in the upright mode (and as the gate metal pads in the upsidedown mode). The width of the source/drain metal pads is 1 μm, and the spacing between source and drain pads is 2 μm, as shown in Fig. 1(a). Afterward, the bottom SWNT bundle (CNT1) was coated to serve as the channel in the upright mode (and as the gate in the upsidedown mode). Then, a 100 nm Si_3N_4 was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 390 °C to serve as the gate insulator. Next, a second 100 nm Ti layer was deposited by rf sputtering, and subsequently patterned by lithography and dry etching to serve as the gate metal pads in the upright mode (and as the source/drain metal pads in the upsidedown mode). Afterwards, the top SWNT bundle (CNT2) was coated. It is worth noting that CNT2 was laid perpendicularly crossing the first CNT1 bundle to serve as the gate in the upright mode (and as the channel in the upsidedown mode). This is followed by a 100 nm SiO_2 deposition by PECVD at 400 °C to serve as the passivation layer. Contact holes to the gate and source/drain metal pads were subsequently etched in a MERIE dry etcher. Wafers could then follow a standard back-end processing to completion. A commercial HP-4155A was applied to measure I_{ds}-V_{ds} and I_{ds}-V_g transfer curves of the CNT-FETs. The top view and cross section of the completed device are shown in Figs. 1(a) and 1(b), respectively. By controlling the process, the bottom CNT1 bundle behaves as an *n*-type semiconductor, while the top CNT2 bundle behaves as *p*-type semiconductor.[4–6]

Scanning electron microscopy (SEM) image of the CNT-gated CNT-FET is shown in Fig. 2. It can be seen that the two CNT bundles, which serve as the gate and the channel interchangeably, are placed on each side of the gate insulator. Note that the two CNT bundles are perpendicularly crossed so as to form a FET structure at the intersection. The diameter of each CNT bundle is around 20 to 50 nm. A bias voltage, which is applied to the top CNT2 bundle, modulates the bottom CNT1 bundle at the intersection. The effective gate length is only 20–50 nm. I_{ds}-V_{ds} characteristics of the

[a)]Author to whom correspondence should be addressed; electronic mail: tschao@mail.nctu.edu.tw

TABLE I. The influence of electrical characteristics by depositing different dielectric layers.

	The dielectric layer deposited on bottom CNT (i.e., CNT 1)/deposition temperature/film thickness	The dielectric layer deposited on top CNT (i.e., CNT 2)/deposition temperature/film thickness	Majority type of the devices on a wafer (using CNT 2 as gate electrode and CNT 1 as channel)	Majority type of the devices on a wafer (using CNT 1 as gate electrode and CNT 2 as channel)
[a]	PE-oxide/400 °C/200 nm	PE-oxide/400 °C/200 nm	*p* type[b]	*p* type[b]
[a]	PE-oxide/400 °C/200 nm	PE-nitride/390 °C/200 nm	*p* type[b]	*n* type[b]
This study	PE-nitride/390 °C/200 nm	PE-oxide/400 °C/200 nm	*n* type[b]	*p* type[b,c]
[a]	PE-nitride/390 °C/200 nm	PE-nitride/390 °C/200 nm	*n* type[b]	*n* type[b]

[a]Data not shown here.
[b]Some of these devices contains ambipolar characteristics.
[c]We got a *p*-type depletion mode characteristic device in this work.

CNT-gated CNT-FET is shown in Fig. 3, respectively. The drain current of the CNT-FET with silicon nitride as the gate insulator increases with the gate voltage, and shows typical *n*-channel FET characteristics. The on/off current ratio is ~1000. By interchanging the roles of the channel and the gate, i.e., the conducting channel now becomes the gate (i.e., the bottom CNT1 bundle becomes the gate), while the gate becomes the new channel (i.e., the top CNT2 now becomes the channel), the upsidedown device also shows FET characteristics, as shown in Fig. 4, albeit with the complementary conduction type (i.e., *p* type). This is because of the close proximity between CNT2 bundle and the oxide passivation layer (Table I).

From the above results, we found that both the bottom and top CNT bundles in the structure can act as the channel and the gate interchangeably. This behavior is unique and differs from traditional Si-based devices. It opens up a new possibility and flexibility in circuit design. For example, the signal is usually routed from one MOSFETs' drain electrode (i.e., output) to the next stages' gate electrode (i.e., input) in Si-based MOSFET circuits. It would require a via and a metal line to connect the two MOSFETs. In contrast, in the new dual-functionality CG CNT-FET structure, one CNT can act as the conduction channel of the first FET and the gate electrode of the next one simultaneously. No interconnection metal is thus needed. In addition to the small gate length and the dual-functionality CNT, the new CNT-FET also offers both *n*- and *p*-type characteristics, lending itself readily to complementary-type circuit implementation, i.e., the CNT conducting channel is changed from *n* type (i.e., CNT1, as described previously) to the *p* type (i.e., CNT2). It is worth noting that the conduction-type of CNT can be tailored by the passivation layer in close contact with the CNT (Table I), as the passivation layer greatly affects the oxygen desorption/reabsorption of the nearby SWNTs, which in turn set the conduction type.

By using plasma-enhanced (PE) nitride as the gate dielectric layer on top of CNT1, the process temperature of the deposition would be high enough (390 °C) to simultaneously remove the oxygen atoms from the CNT1 and CNT1/metal interface in the PECVD deposition chamber. So, we can achieve *n*-type CNT1 channel without extra processing steps.[4–6] For CNT2 as the channel, we adopted PECVD oxide as the passivation layer in this work. The process temperature was around 400 °C. Even though this temperature was high enough to desorb oxygen from CNT2, a few oxygen atoms could be driven back to CNT2 during PECVD TEOS oxide process.[7,8] So CNT2 depicts *p*-type semiconducting characteristics. This is because when the oxygen atoms are reabsorbed during the PECVD oxide process, the Fermi level in CNT2 moves away from the conduction band, and becomes closer to the valence band. So, by applying a negative bias to CNT1 as the gate electrode, the hole can tunnel through the energy barrier efficiently in CNT2 channel. Similarly, we could selectively create *p*-type

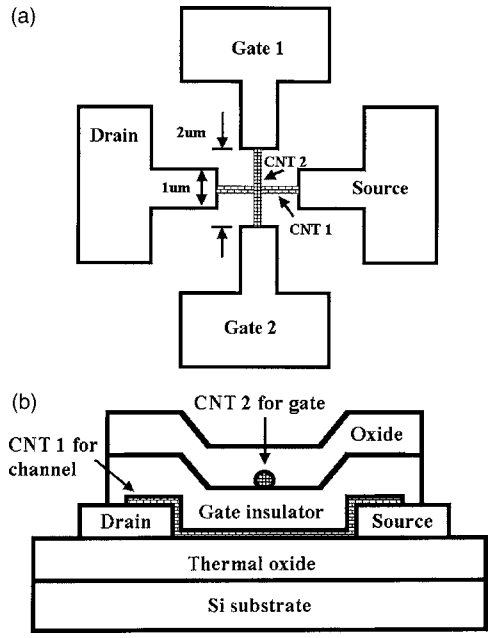


FIG. 1. Top-view (a), and cross-sectional (b) images of the dual-functionality CG CNT-FET.

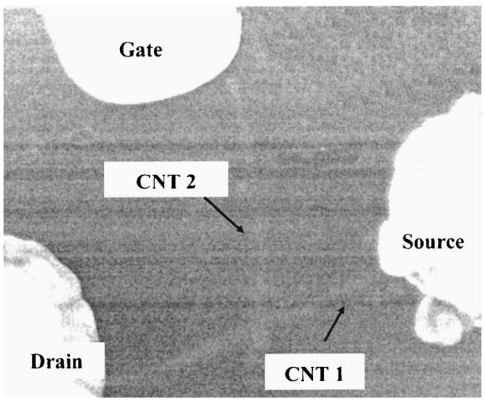


FIG. 2. SEM image of the perpendicularly crossed CNT-FET. Two CNT bundles connected to metal pads are shown forming a cross in this image.

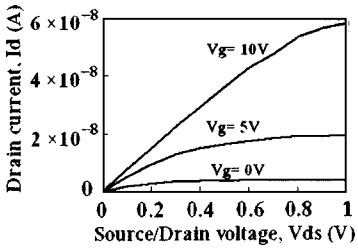


FIG. 3. I_{ds}-V_{ds} curves of CG CNT-FET in the upright mode, showing typical *n*-type FET characteristics (i.e., the bottom CNT1 as the channel, and the top CNT2 as the gate).

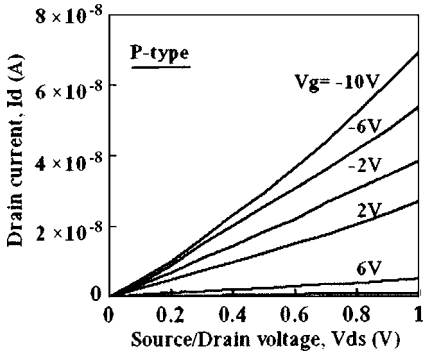


FIG. 4. I_{ds}-V_{ds} curves of CG CNT-FET after interchanging the roles of the channel and the gate (i.e., the bottom CNT1 as the gate, and the top CNT2 as the channel). The upsidedown FET shows typical *p*-type FET characteristic.

CNT-FETs (actually, depletion-mode *p*-type CNT-FET, as shown in Fig. 4), by using CNT2 as the channel and CNT1 as the gate. Both *n*- and *p*-type devices are crucial for complementary metal-oxide-semiconductor (CMOS) circuits as well as certain circuit applications, such as detectors, i.e., a *p*-channel CNT-FET sensor is required for negative charge enzyme system.[9] In the proposed CG-CNT-FET structure, the current-voltage (*I*-*V*) characteristics of each device can be turned by the nearby passivation layer. With the small gate length of CG-CNT-FET, it appears to be promising for future ultrahigh sensitive sensors.

In conventional ultralarge-scale integrated technology, all devices in a chip, or more precisely the whole wafer, are all predetermined early in the process flow. In contrast, for the proposed CG CNT-FET, the type of conduction of each individual CNT-FET in a wafer can be individually controlled much later in the process flow by metal routing. This is because CNT1 and CNT2 can be tuned to different conduction-type by the different passivation layers (Table I). It thus opens up the possibility and flexibility in future CMOS circuit design and fabrication.

In conclusion, a dual-functionality complementary CG CNT-FET is proposed in this study. This CNT-FET has sub-50 nm or smaller feature size without using electron-beam lithography and sub-100 nm etching technology. Two separate CNT bundles are deposited to serve the dual roles of gate and channel of the FET simultaneously. The conduction type of each device is individually determined by selecting CNT1 or CNT2 as the channel, with the other CNT serving as the gate. While the conduction type of CNT1 and CNT2 can be set to be of the complementary type by choosing different passivation layers in close proximity with each CNT bundle. The diameter of CNT bundle could shrink further by improving the CNT purification process, a FET of the SWNT with 1–2 nm gate length can be expected. This unique dual functionality offers the flexibility in the design of future complementary CNT logic circuits.

This work was supported by the Ministry of Economic Affairs, R.O.C. under Contract No. A331XS3410 of the Industrial Technology Research Institute, Hsinchu, Taiwan, R.O.C., and was partially supported by the National Science Council of Taiwan, R.O.C., under Contract Nos. NSC-93-2215-E-009-037 and NSC-93-2120-M-007-002. The authors would like to thank their colleagues in ERSO/ITRI for their valuable discussions as well as their expertise technical assistance.

[1]R. Martel, T. Schnidt, H. R. Shea, T. Hertel, and P. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[2]V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, Nano Lett. **1**, 453 (2001).
[3]S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris, Appl. Phys. Lett. **80**, 3817 (2002).
[4]J.-H. Wei, H.-H. Wang, and M.-J. Kao, U.S. Patent No. 6,723,624April 20, 2004.
[5]J.-H. Wei *et al.*, in *Proceedings of the IEEE-TSA* (2003), p. 42.
[6]D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, Appl. Phys. Lett. **86**, 113115 (2005).
[7]V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, Appl. Phys. Lett. **80**, 2773 (2002).
[8]S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, Phys. Rev. Lett. **89**, 106801 (2002).
[9]K. Besteman, J.-O. Lee, F. G. M. Wiertz, H. A. Heering, and C. Dekker, Nano Lett. **3**, 727 (2003).