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Investigation of overpotential and seed thickness on damascene copper electroplating

K.W. Chen [a], Y.L. Wang [b,*], L. Chang [a], F.Y. Li [c], S.C. Chang [b]

[a] Department of Material Science and Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, ROC
[b] College of Science and Engineering, National University of Tainan , Taiwan, ROC
[c] Department of Chemistry, National Chung-Hsin University, Taichung, Taiwan, ROC

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Abstract

This study found that higher overpotential from higher plating current density and a thinner seed layer resulted in more incorporation of sulfur impurities into a deposited copper film. Our results suggested that the higher plating overpotential resulted in smaller copper grains with more grain boundaries where more impurities were trapped. To achieve a defect-free filling in vias, the optimization of the plating current density and the seed layer thickness was necessary. A copper seed with thickness less than 30 generated a sulfur-rich copper film, while, thickness larger than 200 nm for 0.13-nm technologies, the copper seed led to a poor gapfilling with a void after electroplating.

Keywords: Copper electroplating; Plating current density; Overpotential; Copper seed layer

1. Introduction

Since a damascene structure was successfully implemented in copper interconnection technologies, the gapfilling capability of copper electroplating was progressively researched and developed. It was thought that the quality of copper seed layer was critical for copper nucleation and gapfilling. To achieve a void-free filling as a feature size shrank, a thin and continuous seed layer was necessary for high-aspect-ratio patterns [1,2]. For sub-130-nm technologies, an optimized process condition should be applied to obtain a defect-free filling [3,4]. Previous studies have indicated that the overpotential of copper electroplating was a function of applied current densities and additive compositions, and further responded to the change of film resistivity, electrocrystallization and impurity distribution [5–7]. While high plating voltage or current was applied, the breakdown of organic additives and the incorporation of impurities into a deposited film easily occurred during electrodeposition [6,8]. As the feature size shrank to sub-90 nm, the applied current density and the thickness of the copper seed layers became more critical to optimize the film quality and gapfilling capability [9]. From this point of the view, this study focused on the effect of the plating overpotential on the film properties as well as the correlation between the impurity incorporation, gapfilling capability and the seed layer thickness.

2. Experimental

Blanket and patterned (0.17–0.2 μm) 200-mm Si wafers with silicon dioxide as a dielectric layer, tantalum as a barrier layer and copper as a seed layer were used in this work. The barrier and seed layers were deposited with a commercial physical vapor deposition (PVD) tool. The thickness of barrier and seed layers ranged from 30 to 200 nm. The electroplating experiments were carried out in a commercial plating tool with an electrolyte composed of copper sulfate (50–100 g/l), sulfuric acid (10–30 g/l), chloride ion (50–100 ppm), suppressor (0–20 ppm) and

* Corresponding author. Tel.: +886 6 5051400x5069; fax: +886 36 5051273.
E-mail address: ylwang@tsmc.com (Y.L. Wang).

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accelerator (0–20 ppm). The sheet resistance and the thickness of electroplated copper films were measured by 4-point probe and scanning electron microscopy (SEM), respectively. The surface roughness and grain size image were obtained by atomic force microscopy (AFM). In addition, secondary ion mass spectrometry (SIMS) was used to detect the impurity profiles of the deposited films. Finally, the reliability tests were examined in vias with various seed layer thicknesses; then the failure samples were executed with transmission electron microscopy (TEM) and the impurity components were detected by energy dispersive spectroscopy (EDS).

3. Results and discussion

Table 1 and Fig. 1 summarizes the relationship between different plating current densities and copper film properties, such as resistivity, stress, roughness, reflectivity, and grain size. As the plating current density increased, the surface roughness and grain size of copper films decreased due to an increase of plating overpotential [2]. On the contrary, the resistivity of copper films increased as the plating current increased. This may result from an increase of impurity incorporation, especially for sulfur species. Fig. 2 shows a SIMS profile of the sulfur concentration distribution in a copper film deposited with various current densities. During the above process, the sulfur concentration at the copper surface was higher than that within the intermediate copper film supposedly due to the surface adsorption of impurities from environment or the impurity diffusion from inside film to the surface after post-electroplating annealing [7,10]. It was found that the concentration of sulfur impurities increased also as the plating current density increased, but decreased with the plating transition time. The higher sulfur incorporation rate at the higher plating current density especially in the initial stage of electrodeposition may result from higher copper nucleation rate [11]. Several previous researches have demonstrated that the polarization (overpotential) increased with increasing the plating current density leading to the high copper nucleation rate [2,4,5,9,10,12]. Hence, more impurities, such as sulfur species from the breakdown of accelerators, were trapped in the grain boundaries between smaller grains. The same explanation could also be applied to the phenomena of higher impurities existing in the initial period than that in the subsequence period of the plating. In the initial stage of the deposition, threshold energy was necessary to overcome the high-resistance of the thin seed layer and the barrier of the copper nucleation [9,12–15]. Therefore, higher incorporation rates of the impurities

Table 1
Effect of different plating current densities on the properties of deposited copper films

Items	Plating current			Trend as plating current increasing
	10 mA/cm^2 (small)	40 mA/cm^2 (medium)	60 mA/cm^2 (Large)	
Resistivity (μΩ)	1.75	1.96	2.02	↑
Stress (dyne/cm^2)	$+3.72\times10^9$	$+3.48\times10^9$	$+3.18\times10^9$	(Tensile)↓
Roughness (nm)	11.30	7.38	5.95	↓
Reflectivity	1.25	1.36	1.38	↑
Average grain size (AFM)	0.5 μm	0.3 μm	0.2 μm	↓

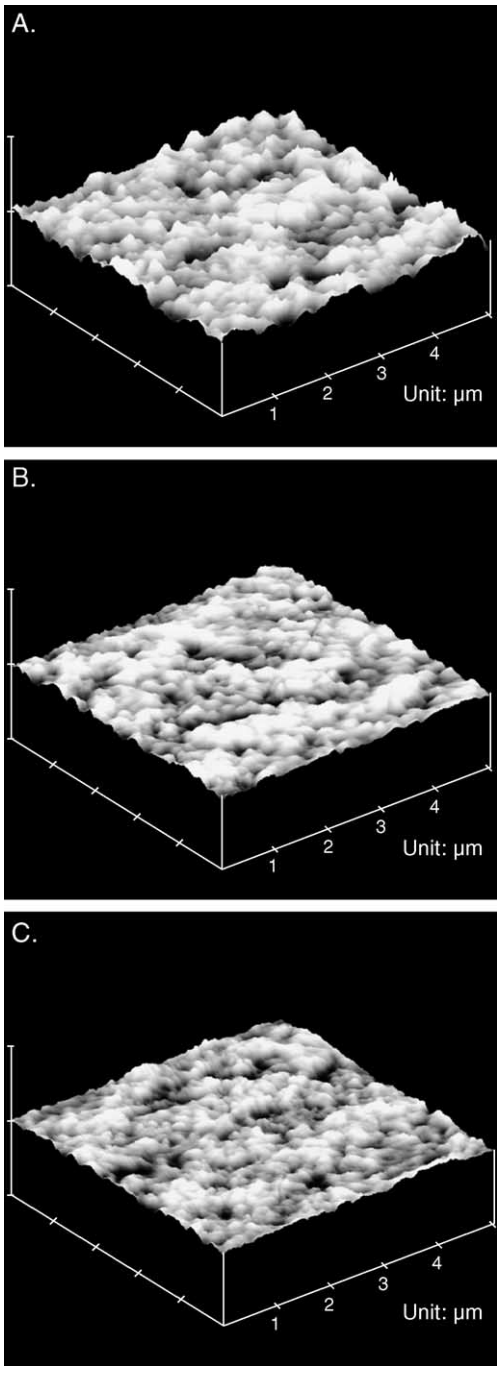


Fig. 1. AFM profile of copper grain size for various plating current densities, where conditions (A), (B) and (C) indicated 10, 40 and 60 mA/cm^2, respectively.

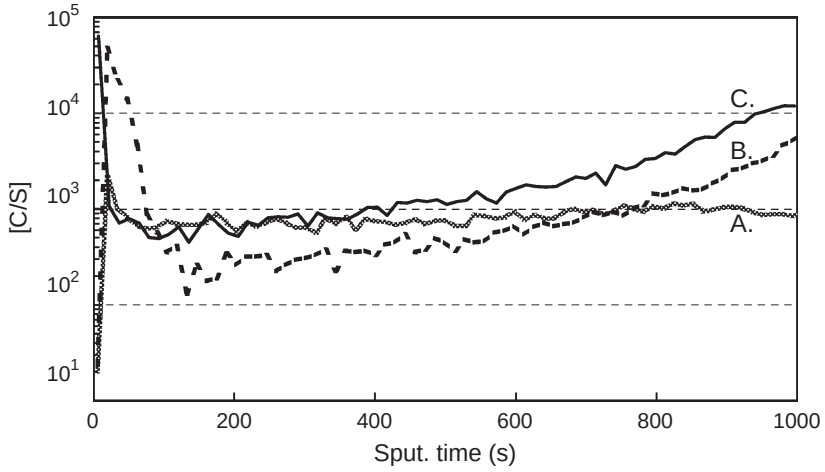


Fig. 2. Sulfur concentration profile of SIMS analysis for various plating current densities, where lines A, B, C indicated 10, 40 and 60 mA/cm^2, respectively.

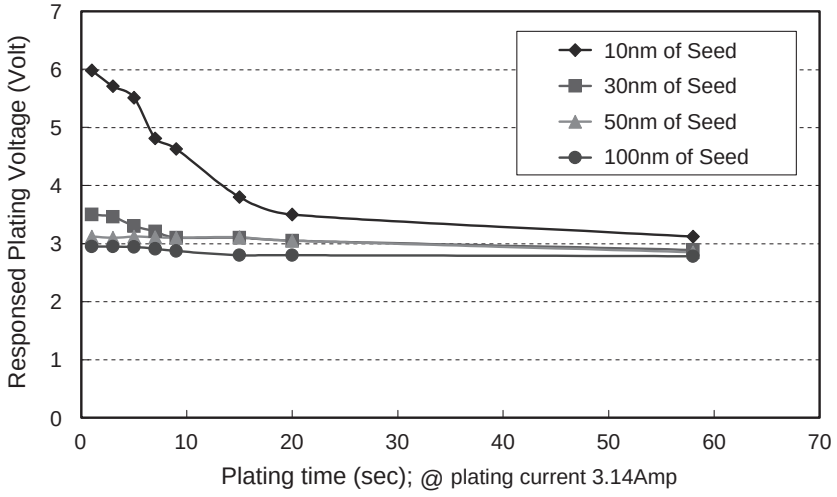


Fig. 3. Plots of plating voltage with plating time for various thicknesses of the copper seed layers. In this case, the current density was fixed at 10 mA/cm^2.

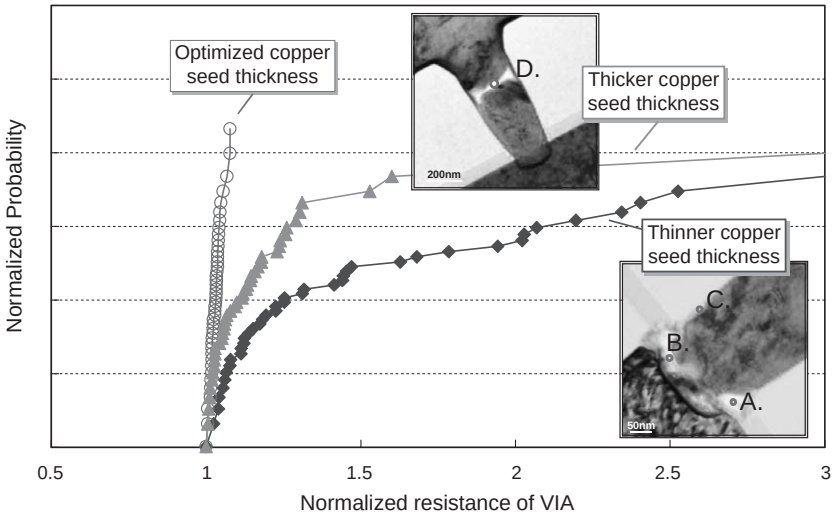


Fig. 4. Normalized resistance probability distribution of the vias under different thicknesses of the copper seed layers.

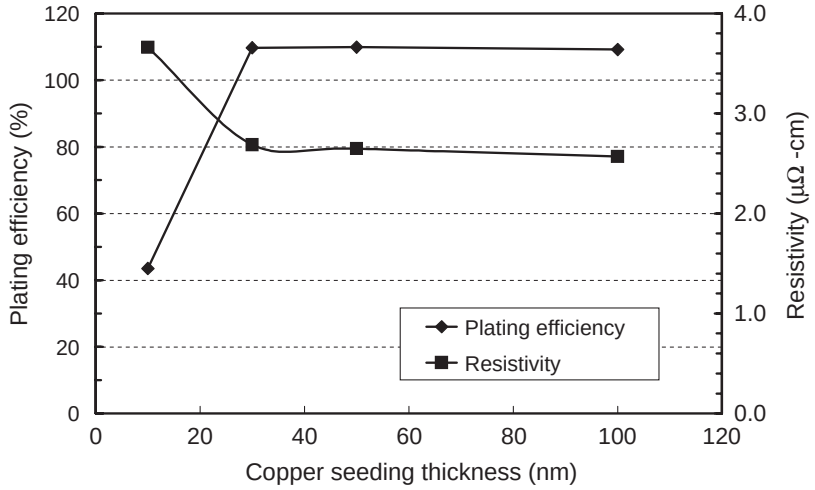
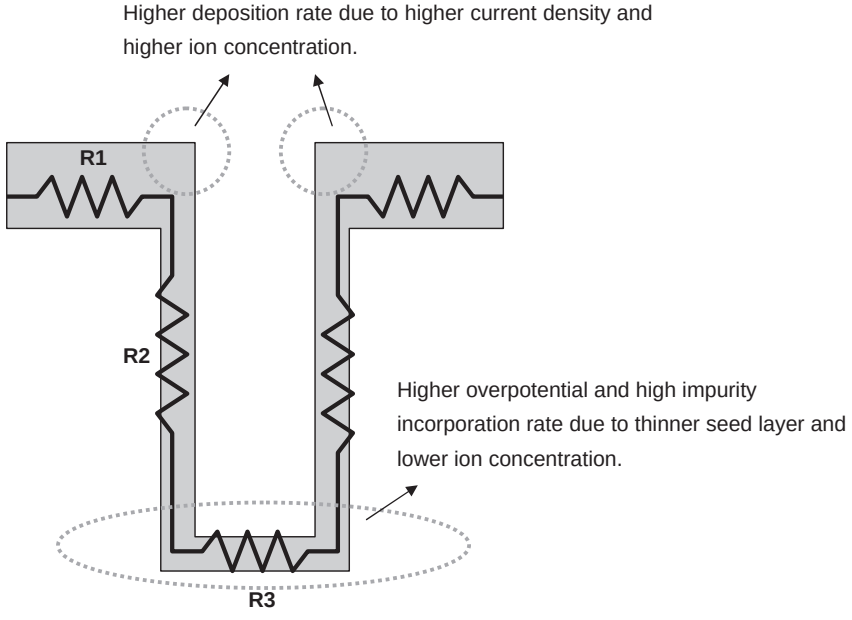


Fig. 5. Resistivity of deposited copper films using different thicknesses of the copper seed layers.

occurred in the initial plating due to the higher initial overpotential or higher initial surface concentration of additives. As shown in Fig. 3, the plating voltage was high in the initial period of the plating and decreased with increasing the deposition time due to an increase in deposited copper thickness. In addition, increasing the thickness of copper seed layers decreased the plating voltage especially in the initial stage (0–10 s) of the plating. The plausible reason was that the charge transfer resistance decreased as the seed layer thickness increased.

Fig. 4 displays the reliability tests of 0.17–0.22 μm vias deposited with various seed thicknesses of 100, 150 and 200 nm. The experiments were carried out in 500 h and 180 °C baking torture after the plating process. To avoid the discontinuous seed layer in the vias, the cross-sectional profiles of the vias with different seed layer thicknesses were checked by TEM before copper electroplating. On the via sidewalls and bottoms, the copper thickness was about 5–20 times thinner than that on the field area outside of the vias. For example, as the 100-nm-thick seed was deposited on the field area by PVD process, there was around 10–20-nm-thick copper seed existing on the sidewall and bottom. However, this level of the copper thickness induced a thin seed effect [9]. In Fig. 4, the



R1: copper seed resistance on the field area
R2: copper seed resistance on the sidewall
R3: copper seed resistance on the bottom
R2 ≈ R3 > R1

Fig. 6. Proposed model of seed thickness effect on copper electroplating.

resistance of the thinner (~100 nm on the field area) seed layer, i.e. the solid diamond line, had a tailing distribution. From the TEM analysis, it was found that the explosion-like copper structure was obtained at the bottom where the seed thickness was relatively thinner (~10–20 nm) and mass transfer was limited. The EDS measurement also detected these defect areas with rich sulfur elements (A, B, and C points). It was suspected that high overpotential at the bottom caused high impurity incorporation and the formation of CuS_x components expanded the molecular volume. Previous studies have reported that the major source of the sulfur impurities resulted from the decomposition of accelerators at higher plating overpotentials [5,16,17]. Fig. 5 shows that a high resistivity copper film was obtained using too thin copper seed layer (<30 nm) supposedly due to more sulfur incorporation. On the other hand, the via resistance of the thicker seed layer (~200 nm on the field area), i.e. the solid-triangle line, also had a tailing distribution owing to the void formation after copper electroplating, as shown in the TEM image (D point) of Fig. 4. A proposed model in Fig. 6 displays that at the via bottom with a thinner seed layer, higher overpotential induced higher impurity incorporation rate due to higher seed resistance and lower ion concentration, while on the filed area with a thicker seed layer, higher deposition rate easily caused overhang phenomenon due to higher current density and higher ion concentration. The optimized thickness of the copper seed layer (hollow-circle line) shows a low and sharp distribution of the via resistance through the reliability tests.

4. Conclusions

The incorporation concentration of sulfur impurities from the breakdown of accelerators during copper electroplating depended on the plating current densities as well as the seed layer thickness. The high plating overpotential from the high plating current density and the thin copper seed layer led to a high resistivity copper film. The thickness of copper seed layers was also critical for the via resistance of electroplated copper films. Using a copper seed layer too thin resulted in a sulfur-rich copper film, while depositing a copper seed layer too thick easily caused the void formation in the feature. The optimized seed thickness was necessary to reduce impurity incorporation at the feature bottom as well as to inhibit the overhang phenomenon at the feature opening.

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