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A novel method for growing polycrystalline Ge layer by using UHVCVD

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Abstract

Poly-Ge grown on SiO_2 substrates by using one-step ultra-high vacuum chemical vapor deposition (UHVCVD) process with thin Si nucleation layers at very low deposition temperature (350 °C) was demonstrated. The results demonstrated that the polycrystalline silicon (poly-Si) nucleation layer is needed for the growth of polycrystalline germanium (poly-Ge) on SiO_2 substrates at low growth temperature. SEM image presents the films with uniform grain size and uniform thickness occurring in the samples. The grain size of poly-Ge is about 100 nm. The Raman shift spectrum and XRD spectrum also identified that films are high quality poly-Ge by using this method.

Keywords: UHVCVD; Polycrystalline; Germanium

1. Introduction

Poly-Si thin film transistors (poly-Si TFTs) are currently investigated for applications in active matrix liquid crystal displays (AMLCDs) [1]. In recent years, many research in poly-Si and poly-SiGe on TFT application have been conducted [2–9], but there is no advanced study on poly-Ge TFT. Inspired by the recent progress of high-k dielectric gate in Si MOSFET applications, the poly-Ge have attracted more and more attention; they will be extensively investigated in the future. Poly-Ge is a candidate for TFT application due to the advantage of its high field effect mobility and the smaller band gap for supply voltage scaling. Recently, it has been found that UHVCVD system can grow poly-Si film with high purity on SiO_2 substrate [10,11] but that it is difficult for depositing Ge atoms on SiO_2 substrate [12]. Hence, it is necessary for depositing nucleation layers on SiO_2 substrate such as Si layers using plasma-enhanced chemical vapor deposition [13].

In this study, we report a new method for growing high quality and high purity poly-Ge at low growth temperature. The method includes: (1) thin silicon nucleation layers grown at 450 °C/85 mTorr and (2) poly-Ge grown at 350 °C/5 mTorr. The results show some advantages of the poly-Ge layer such as one growth process of polycrystalline Ge layers deposition, high thick uniformity of the film, low deposition temperature, uniform grain size, large grain size, large wafer size, and high throughput. By this method, the poly-Ge grown at low temperature environment on oxide-coated silicon by using one growth process procedure has been demonstrated. There are no technical literatures presented which about the one growth process depositing of poly-Ge at low temperature. Moreover, the deposition temperature and deposition thickness can be controlled accurately. In addition, as results of the method, the application of low temperature thin film transistors by using high dielectric constant material, novel structure and re-crystal technology on LTPS become possible. Very low temperature poly-Ge thin film transistors will be achieved and the next display generation will be realized.

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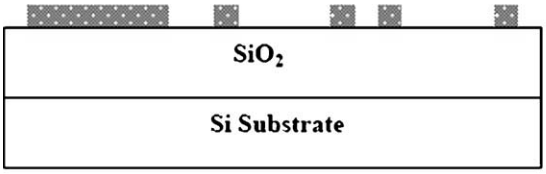
2. Experimental details

2.1. Experimental methods

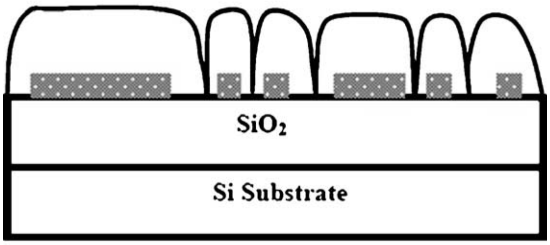
The poly-Ge layers were deposited on the silicon dioxide wafers by using ultra-high vacuum chemical vapor deposition (UHVCVD) at 350 °C. The UHVCVD system features an ultra clean growth environment (background pressure $\sim 2 \times 10^{-8}$ Torr) that provided low carbon and oxygen contamination in the chamber. The hot-wall UHVCVD method can distribute uniform heat on the poly-Si nucleation layers that is an important issue for growing uniform Ge film. It is easier for Ge atoms to be uniformly deposited on the first nucleation layers, if the temperature is kept uniform. The result shows that the surface of the poly-Ge was bright and uniform. The low temperature, high quality and high purity Ge were realized by using this method. The mechanism of the one growth process procedure employed in this work is shown schematically in Fig. 1. By the method, the Ge ions can be successfully deposited on SiO_2 to overcome the difficulty by using conventional thermal chemical vapor deposition method.

2.2. Sample preparation

The 6-in. wafers were first cleaned by using RCA method to remove the particles, metal ions, and native oxide. After RCA cleaning, the wafers were subjected to thermal furnace to grow the thermal oxide. In order to simulate the environment of thin film transistor fabrication, the depth of thermal oxide was 550 nm. The poly-Si (poly-Si) layer was deposited by using UHVCVD system on the double side oxide-coated Si wafers. The deposition duration of poly-Si was about 60 min at 450 °C. The poly-Si layer was severed as the nucleation layer to make Ge ions deposited. The poly-Si buffer layer provides a suitable nucleation layer for depositing poly-Ge layer. After the poly-Si buffer layer deposited, we turned off the SiH_4 gas source and then dropped the temperature from 450 °C to 350 °C which is the poly-Ge deposition temperature. When the temperature arrived at 350 °C, we inserted GeH_4 gas into the chamber (350 °C/5 mTorr for 1 h) to form poly-Ge layer. In addition, the directly deposited poly-Ge condition was performed at 350 °C for 2 h in the study. Furthermore, the directly deposited poly-Si layer was also performed at 600 °C for 2 h to compare with the poly-Ge layer by the new method. The sample preparations were illustrated in Fig. 2, respectively.



(a) Si seeds and nucleation layer



(b) poly Ge layer

Fig. 1. (a) Si seeds and nucleation layer and (b) poly-Ge layer.

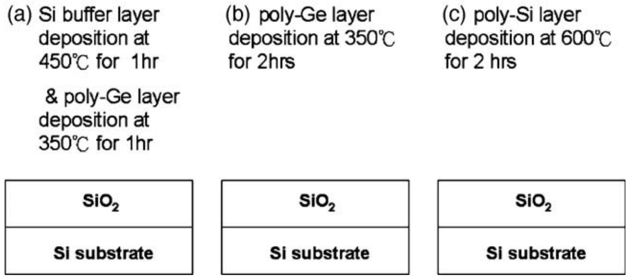


Fig. 2. The sample preparation for (a) poly-Ge deposition using new method, (b) poly-Ge deposition using conventional method, and (c) poly-Si deposition by conventional method.

3. Results and discussion

We have grown poly-Ge on the SiO_2 wafer successfully and overcome the difficulty of growing Ge on the SiO_2 without plasma-enhanced chemical vapor deposition (PECVD). The silicon nucleation layers were used as nucleation seeds for growing poly-Ge in this method. Fig. 1(a) shows the Si nucleation layers on the SiO_2 substrate. For the low-temperature surface reaction-limited regime shown, surface hydrogen coverage is a key factor in growing the poly-Si on oxide. Therefore, the higher growth temperature and higher growth pressure is needed in the first growth step. The conventional method was presented where Ge atoms can react with SiO_2 in the heat environment [12], but where uniform Ge layers on SiO_2 layer were hard to form. Fig. 1(b) presents the poly-Ge growth mechanism. Incubation time of poly-Ge growth is shorter than direct growth poly-Ge on SiO_2, which may be due to the addition of Ge to increased hydrogen desorption, increasing the number of polycrystalline Si surface sites for precursor adsorption in this procedure. Hence, the growth temperature and the growth pressure can be reduced.

The electrical characteristics of lager grain-size poly-Si thin film transistors will be improved such as turn on current because the carrier will suffer from lower grain boundaries. On the other hand, the uniformity of poly-Si plays an important role of the large-scale thin film transistors. The grain size and uniformity become the index of lager scale poly-Si thin film transistors that also for the application of

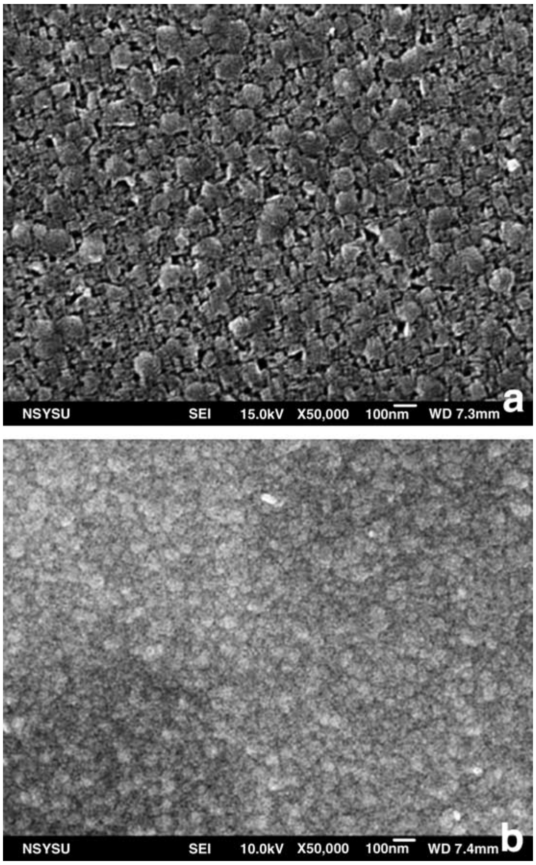


Fig. 3. (a) The SEM top view of poly-Si and (b) the SEM top view of poly-Ge.

the poly-Ge TFT. Fig. 3(a) shows the SEM top view image of poly-Si layer grown on SiO_2 substrate at 600 °C which is around the transition temperature for poly-Si growth. The grain sizes of poly-Si are about 100 nm, but the films are non-uniform. Fig. 3(b) shows the SEM image top view of polycrystalline Ge layers deposited on SiO_2 substrate. The grains of the polycrystalline Ge layers on the SiO_2 with the polycrystalline Si nucleation layers can be clearly observed and the grain size is about 100 nm. Furthermore, the grains of polycrystalline Ge layers are very uniform.

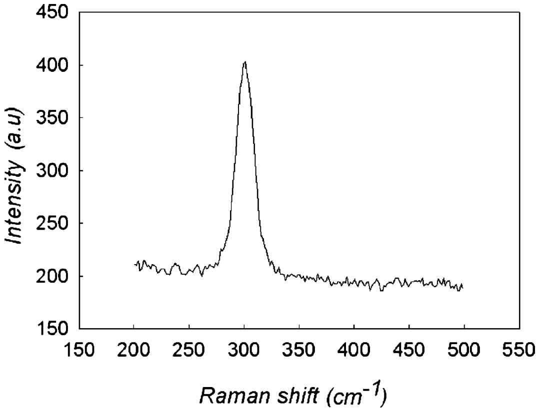


Fig. 4. The Raman shift spectra of the poly-Ge depositing using new method.

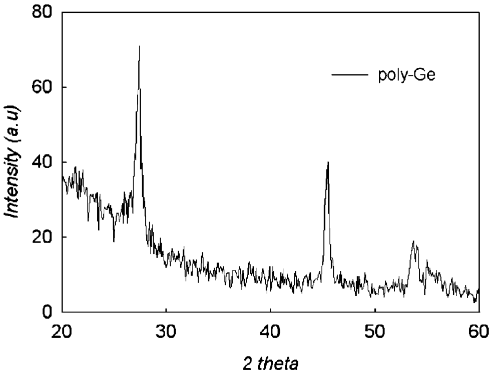


Fig. 5. The XRD of the poly-Ge depositing using new method.

The poly-Si TFT technology is really the most promising approach. However, the process temperature of 600 °C limits the poly-Si TFTs to be fabricated on cheap glasses. Fig. 4 shows the Raman shifted spectrum of poly-Ge film grown at 350 °C. At peak of 300 cm^{-1}, the Ge–Ge peak was obviously observed and the intensity of the peak was very strong. Fig. 4 shows the XRD spectrum with glancing angle of poly-Ge film grown at 350 °C. The Ge peaks are also clearly observed in the spectrum. According to the Figs. 4 and 5, we can confirm that the crystalline of deposited germanium films by this method is polycrystalline type. In a previous work, the deposition temperature of the poly-Si is larger than 550 °C, which is higher than this work. This may be attributed to the high hydrogen desorption in the oxide surface at high growth pressure that provides more sites for Si atoms to nucleate; this conjecture needs future investigation. Therefore, the poly-Ge films can grow at low temperature with uniform thickness.

Fig. 6 presents the SEM top view image of the sample. The sample was directly grown on SiO_2 substrates by using the conventional method without Si nucleation layers. Comparing Fig. 6 with Fig. 3, the result shows lack of Ge agglomerates formed on SiO_2. Indeed, it is difficult for the formation of Ge layers on SiO_2. The poly-Ge peaks were

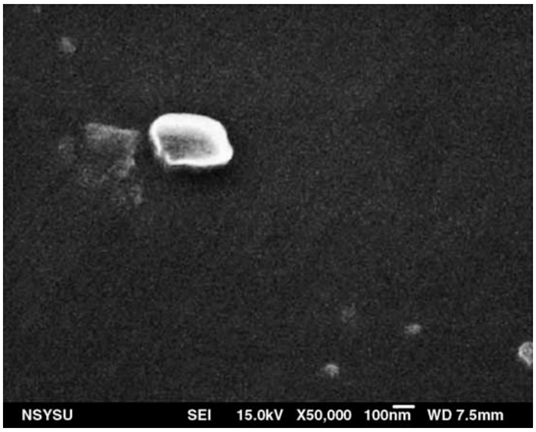


Fig. 6. The SEM top view of poly-Ge deposited on SiO_2 at 350 °C using conventional method.

not to be observed in the Raman-shifted spectrum and the XRD spectrum (data not shown).

4. Conclusion

The growth of polycrystalline Ge on SiO_2 layer at low temperature (350 °C) has been demonstrated by using ultra high vacuum chemical deposition (UHVCVD) method. The growth method includes: (1) thin silicon nucleation layers grown at 450 °C/85 mTorr and (2) high quality poly-Ge grown at 350 °C/5 mTorr. The results show that the films formed by using this method has high uniformity and high polycrystalline of Ge layer. The grain size of polycrystalline Ge is about 100-nm-thick that is close to the high temperature grown poly-Si in this work. Due to the low temperature poly-Ge preparation, the thermal budget and cost will be reduced. In addition, the Ge layer deposition technology on SiO_2 can be applied on TFT fabrication process for its higher field effect mobility than Si material.

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