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Process-variation- and random-dopants-induced threshold voltage fluctuations in nanoscale planar MOSFET and bulk FinFET devices

Yiming Li *, Chih-Hong Hwang, Hui-Wen Cheng

Department of Communication Engineering, National Chiao Tung University, P.O. Box 25-178, Hsinchu 300, Taiwan

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ABSTRACT

Impact of the intrinsic fluctuations on device characteristics, such as the threshold voltage (V_{th}) fluctuation is crucial in determining the behavior of nanoscale semiconductor devices. In this paper, the dependency of process-variation and random-dopant-induced V_{th} fluctuation on the gate oxide thickness scaling in 16 nm metal–oxide–semiconductor field effect transistors (MOSFETs) is investigated. Fluctuations of the threshold voltage for the studied planar MOSFETs with equivalent oxide thicknesses (EOT) from 1.2 nm to 0.2 nm (e.g., SiO_2 for the 1.2 and 0.8 nm EOTs, Al_2O_3 for the 0.4 nm EOT and HfO_2 for the 0.2 nm EOT) are then for the first time compared with the results of 16 nm bulk fin-typed filed effect transistors (FinFETs), which is one of the promising candidates for next generation semiconductor devices. An experimentally validated simulation is conducted to investigate the fluctuation property. Result of this study confirms the suppression of V_{th} fluctuations with the gate oxide thickness scaling (using high-κ dielectric). It is found that the immunity of the planar MOSFET against fluctuation suffers from nature of structural limitations. Bulk FinFETs alleviate the challenges of device's scaling and have potential in the nanoelectronics application.

1. Introduction

As the dimension of complementary metal–oxide–semiconductor (CMOS) devices shrunk into sub-90 nm scale, threshold voltage (V_{th}) fluctuations resulting from such as the short channel effect and random dopant are pronounced [1–15]. The random-dopant-induced fluctuation is mainly from the random nature of ion implantation. The gate-length deviation and line-edge roughness could be attributed to the short channel effect. Fluctuation is getting worse due to serious short channel effect when the dimension of device is further scaled. Consequently, it affects the design window, yield, noise margin, stability, and reliability of ultra large-scale integration circuits. The tolerance of fluctuation has to be controlled even strictly with increases in the number of transistors as technology advances. The use of thin gate oxide is one of effective ways to suppress the process-variation- and random-dopant-induced V_{th} fluctuation [6]. Our recent work has demonstrated that the V_{th} fluctuation of a 15 nm planar metal–oxide–semiconductor field effect transistor (MOSFET) device could be suppressed by 20%, as the gate oxide scales is scaled down from 1.2 nm to 0.8 nm [6]. However, ongoing scaling of gate oxide thickness may raise problems of process controllability, leakage current, and reliability. The use of a high-κ dielectric is a key to enhance the performance of such devices [16–18]. For devices with vertical channel structures, such as fin-typed FETs (FinFETs), immunity against fluctuation is also fascinating, because they possess better channel controllability [7,19–22]. Study of the effectiveness of fluctuation suppression and the mechanism against fluctuations according to these two approaches will be an interesting and benefit the nanodevice technology.

In this paper, the dependency of process-variation- and random-dopant-induced threshold voltage fluctuation on the gate oxide thickness scaling in 16 nm nano-MOSFETs is examined. Together with statistically generated process-variation-induced gate lengths and the large-scale doping profiles, the V_{th} fluctuation for each studied devices is computed by solving a set of three-dimensional (3D) quantum correction transport equations [23–25]. We notice that the device's threshold voltage and the mobility of the explored planar device (the case of 1.2 nm EOT) are calibrated with the measured data [6]. Fluctuations of the studied planar MOSFETs with equivalent oxide thicknesses (EOT) ranging from 1.2 nm to 0.2 nm, where Al_2O_3 is for the 0.4 nm EOT and HfO_2 is for the 0.2 nm EOT are then compared with the results for 16 nm bulk FinFETs [7,19–22]. The 16-nm-gate planar MOSFET with the 0.2 nm EOT is demonstrated to offer similar immunity against fluctuation as the 16 nm-gate bulk FinFET device with the 1.2 nm EOT. Additionally, its found the immunity of the planar MOSFET against

* Corresponding author. Tel.: +886 3 571 2121x52974; fax: +886 3 5726639.
E-mail address: ymli@faculty.nctu.edu.tw (Y. Li).

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fluctuation is limited by structural limitations while the multiple-gate FET, such as FinFETs, can overcome challenges with device scaling and is favorable in the era of nanoelectronics.

This article is organized as follows. In Section 2, we describe the analyzing technique. In Section 3, we present and discuss the results. Mechanism of process-variation- and random-dopant-induced fluctuation are shown and discussed. Finally, we draw conclusions and suggest future work.

2. Simulation methodology

The threshold voltage fluctuation is assumed to be contributed from the random-dopant and short channel effect. Effects of gate-length deviation (L_g), and the line-edge roughness (LER) are resulted from process-variation and belong to the short channel effects The random-dopant and short channel effect are independent sources of fluctuation, and the standard deviation of the total threshold voltage, $V_{th,total}$, can be expressed by the following relation

$$\sigma^2_{V_{th,total}} = \sigma^2_{V_{th,RD}} + \sigma^2_{V_{th},L_g/LER}, \quad (1)$$

where $\sigma_{V_{th,RD}}$ is the random-dopant-induced fluctuation, $\sigma_{V_{th},L_g/LER}$ is fluctuations caused by the gate-length deviation and line-edge roughness.

Fig. 1 presents the structures of the studied devices, where Fig. 1a and b are the planar MOSFETs and the bulk FinFETs. The EOT of planar MOSFET ranges from 1.2 nm to 0.2 nm and the EOT of bulk FinFET is fixed at 1.2 nm. The used dielectric materials are summarized in Table 1, where SiO_2 is used for a gate oxide thickness of 1.2 nm and 0.8 nm, Al_2O_3 is for a gate oxide thickness of 0.4 nm, and HfO_2 is for a gate oxide thickness of 0.2 nm. The nominal channel doping concentration of the devices herein is 1.48×10^{18} cm^{-3}. The devices have a 16 nm gate and a workfunction of 4.4 eV.

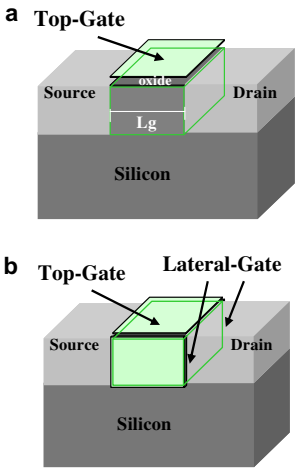

Fig. 1. An illustration of the studied: (a) planar MOSFET and (b) bulk FinFET.

Table 1
The used dielectric materials in this study, SiO_2 is used for the cases of the 1.2 and 0.8 nm EOTs, Al_2O_3 is for the case of the 0.4 nm EOT and HfO_2 is for the case of the 0.2 nm EOT

Material	Dielectric constant	This work (nm)
SiO_2	3.9	EOT = 1.2/0.8
Al_2O_3	8–11.5	EOT = 0.4
HfO_2	25–30	EOT = 0.2

To elucidate the effect of random fluctuations of the number and location of discrete dopants in the device channel, 758 doping islands are initially generated in an $(80\ nm)^3$ cube, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 2a. The $(80\ nm)^3$ cube is then partitioned into 125 sub-cubes of volume $(16\ nm)^3$. The number of dopants may vary from zero to 14, and the average number is six, as shown in Fig. 2b–d, respectively. These 125 sub-cubes are then equivalently mapped into the channel region of the device for discrete dopant simulation, as shown in Fig. 2e and f. All statistically generated discrete dopants are incorporated into the large-scale 3D device simulation using the parallel computing system [26–28]. Characteristic of each device is obtained by solving a set of Poisson equation, electron-hole current continuity equations, and density-gradient equation [23–25]. This approach enables us to calculate the fluctuations of electrical characteristics that induced by the randomness of the number and position of dopants in the channel region to be investigated. This statistically sound full-scale 3D "atomistic" device simulation technique considers the computational cost and accuracy simultaneously.

Furthermore, we apply the statistical approach to evaluate the effect of process-variation-induced V_{th} fluctuation, $\sigma_{V_{th},L_g/LER}$ [29]. The magnitude of the gate-length deviation and the line-edge roughness are extracted from the projections of the ITRS 2005 for different technology nodes [30]. A look-up table of the threshold voltage vs. gate length is established, as shown in Fig. 3. It enables us to evaluate the threshold voltage with respect to the deviation of gate-length deviation and line-edge roughness, which following

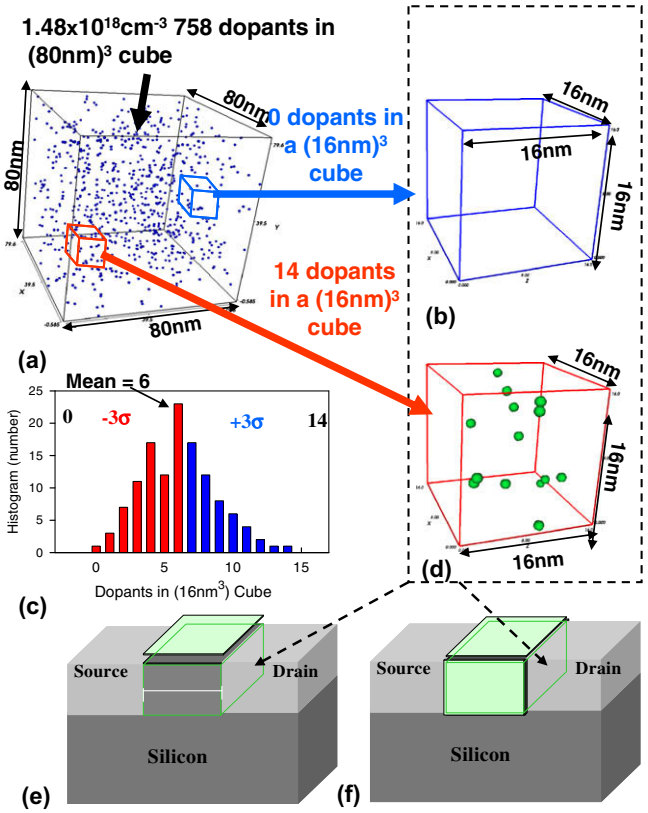

Fig. 2. (a) Discrete dopants randomly distributed in $(80\ nm)^3$ cube with an average concentration of 1.48×10^{18} cm^{-3} and then partitioned into 125 sub-cubes of $(16\ nm)^3$, where the numbers of dopant in sub-cubes may vary from zero to 14, as shown in (b), (c), and (d). These sub-cubes are then equivalently mapped into channel region of studied devices, (e) and (f), for dopant position/number-sensitive simulation. It means that for each explored device there are 125 cases of the 3D device simulation have to be performed.

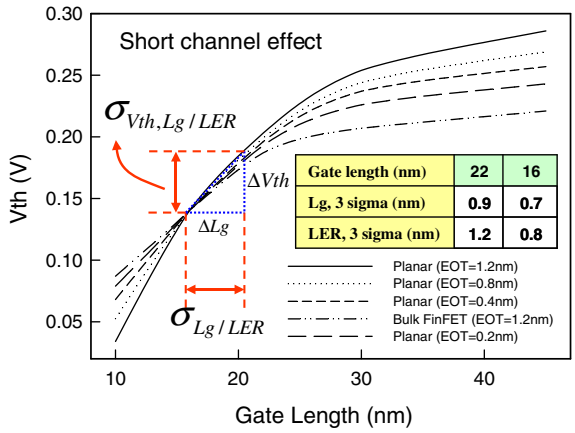

Fig. 3. The threshold voltage roll-off of the studied devices, where the variation follows the projection of ITRS 2005 roadmap. These results are used to estimate the V_{th} fluctuation resulting from the gate-length deviation and the line-edge roughness.

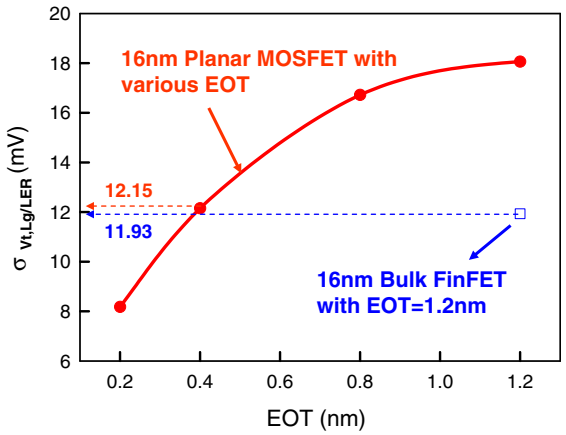

Fig. 5. The process-variation-induced threshold voltage fluctuation for the studied devices.

the roadmap of ITRS that $3\sigma L_g$ = 0.9 nm and 3σLER = 1.2 nm for the 22 nm node and $3\sigma L_g$ = 0.7 nm and 3σLER = 0.8 nm for the 16 nm technology node, as the inset table of Fig. 3. Thus, we can calculate the standard deviation of threshold voltage resulting from the deviation of gate length and the roughness of line-edge. The accuracy of the simulation is verified by comparing the simulated fluctuation results and the measured data of experimentally fabricated 20 nm devices [6]. The threshold voltages of the studied devices are adjusted to 140 mV. The threshold voltage is derived from a current criterion of 10^{-7} (W/L) (A), where the W and L are the width and length of device, respectively.

3. Results and discussion

Fig. 4 plots the gate capacitance (C_g) as a function of the EOT, where the solid line shows the planar MOSFETs with various EOT and the square symbol indicates the bulk FinFET device with 1.2 nm EOT. The planar MOSFET with 0.4 nm EOT, where Al_2O_3 is used for gate dielectric, exhibits a similar gate capacitance with the bulk FinFET device with 1.2 nm EOT. Since the value of gate capacitance is one of the indexes for the channel controllability of device, the bulk FinFET device with 1.2 nm EOT is expected to have similar immunity against process-variation induced fluctuation with the planar MOSFET with 0.4 nm EOT. This assumption is then verified in Fig. 5, which presents the process-variation-induced V_{th} fluctuation, $\sigma_{V_{th},L_g/LER}$, of the planar MOSFETs and bulk FinFETs. The use of thin gate oxide and high-κ dielectric material is effective in suppression of process-variation-induced V_{th} fluctuation. As expected the process-variation-induced V_{th} fluctuation of the planar MOSFET with 0.4 nm EOT is very similar that of the bulk FinFET device with 1.2 nm EOT. From the viewpoint of process-variation-induced fluctuation, the bulk FinFET device with 1.2 nm EOT exhibits a similar immunity against process-variation-induced fluctuation with the planar MOSFET with 0.4 nm EOT. However, will the trend still valid in the random-dopant-induced fluctuation?

Fig. 6 shows the random-dopant-induced V_{th} fluctuation, $\sigma_{V_{th,RD}}$, of the studied devices. The random-dopant-induced V_{th} fluctuation decreases significantly as the EOT is scaled down. However, even thought the planar MOSFET with 0.4 nm EOT has a similar gate capacitance with bulk-FinFET with 1.2 nm EOT, the immunity against random-dopant-induced fluctuation of these two devices is rather different. The bulk FinFET device shows a better immunity against fluctuation than expected. It exhibits a similar V_{th} fluctuation as the planar MOSFET device with 0.2 nm EOT, where HfO_2 is used for gate dielectric.

To further investigate the reason why bulk FinFET can provide a better immunity against random-dopant-induced fluctuation, the potential distributions extracted 1 nm below the top gate of channel are examined, where the applied gate voltage (V_G) is 1 V and the applied drain voltage (V_D) is 0 V. The potential barriers, shown in Fig. 7b–f, are induced by the corresponding dopants at positions:

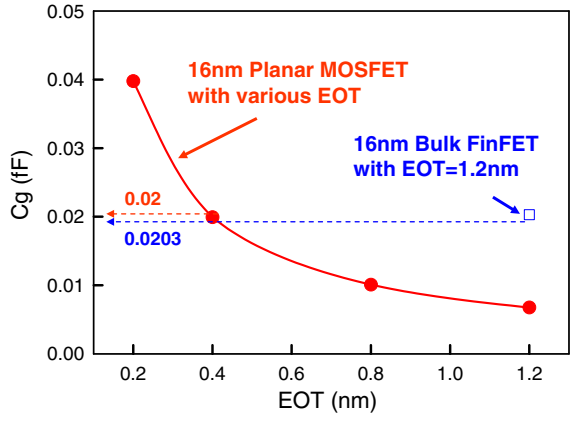

Fig. 4. The gate capacitance (C_g) as a function of the EOT, where the solid line shows the planar MOSFETs with various EOT and the square symbol indicates the bulk FinFET device with 1.2 nm EOT.

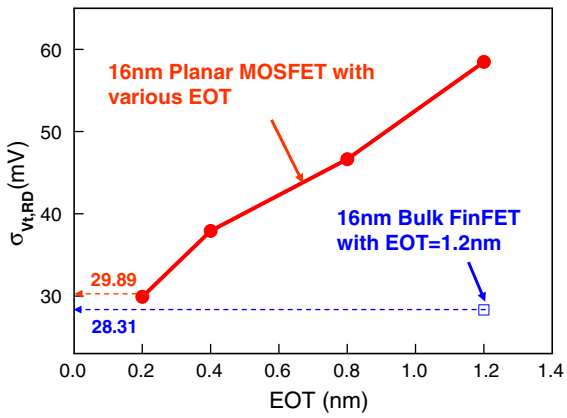

Fig. 6. The random-dopant-induced threshold voltage fluctuation for the studied devices.

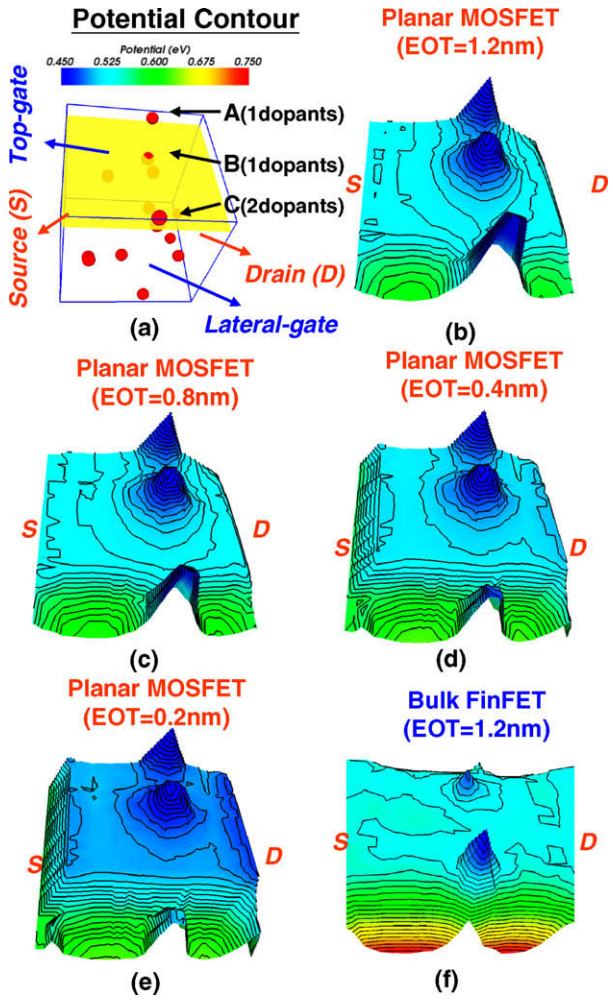

Fig. 7. Top-gate potential contours of the planar MOSFETs with various EOT (b) EOT = 1.2 nm, (c) EOT = 0.8 nm, (d) EOT = 0.4 nm, (e) EOT = 0.2 nm) and (f) bulk FinFETs with 1.2 nm EOT. The distributions of potential barriers are induced by the corresponding dopants location (i.e., A, B and C). The corresponding distribution of discrete dopants is shown in (a) and all the plots are extracted 1 nm below the gate oxide.

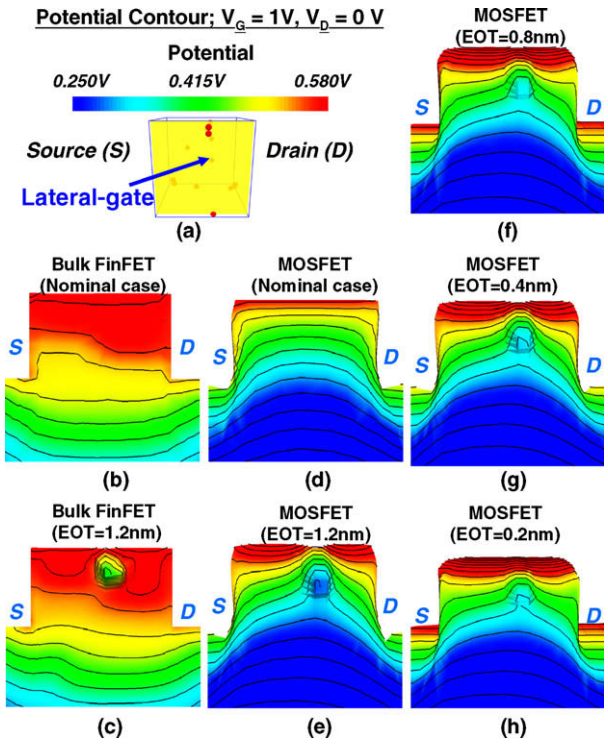

Fig. 8. Lateral-gate off-state potential contours for the studied planar MOSFET and bulk FinFET devices, where (b) and (c) show the nominal (continuously doped) and discrete dopant fluctuated cases of bulk FinFETs. The nominal and discrete dopant fluctuated cases of planar MOSFETs with different EOTs are shown in (d)–(h).

A, B, and C, respectively, as shown in Fig. 7a. The potential barrier is largest at C, because two discrete dopants are located close to each other there. For planar MOSFETs with different EOTs, the sizes of the potential barriers are suppressed as the equivalent gate oxide thickness is reduced. The results for planar MOSFETs, as displayed in Fig. 7b–e are then compared with that of a bulk FinFET device, as shown in Fig. 7f, indicating that the potential barriers of bulk FinFET are smaller than those of planar MOSFETs, especially at position A. The potential barrier induced by corresponding dopant in A is significantly reduced in bulk FinFET device because the channel potential is effectively controlled by the top- and lateral-gates of the device at position A. The difference between the gate structures shows the difference between the mechanisms against fluctuations of the planar and bulk FinFET devices.

Fig. 8 shows the lateral side potential distributions of the studied devices. Fig. 8b and c show the potential contours of the nominal (continuous channel doping concentration: 1.48×10^{18} cm^{-3}) and discrete dopant fluctuated cases of bulk FinFETs with 1.2 nm EOT. Fig. 8d–h show the nominal and discrete dopant fluctuated cases of planar MOSFETs with EOT scaling. For the discrete dopant fluctuated bulk FinFET device in Fig. 8c, although the potential distribution is disturbed by a dopant that is located on lateral side of the channel, the overall potential distribution in the case of fluctuation is still quite similar to that in the nominal case. However, for MOSFET, as shown in Fig. 8e, the overall potential distribution is distorted significantly. The distortion is mitigated as the equivalent gate oxide thickness is scaled down, as shown in Fig. 8f–h. This result reconfirms the effect of the lateral gate in bulk FinFET devices in suppressing potential fluctuations.

Fig. 9 plots the top and lateral views of the on-state current density (V_G = 1 V; V_D = 1 V) of planar and bulk FinFET devices with 1.2 nm EOT. All cross-sectional plots are from 1 nm below the top and lateral side of channel surface. The top views of the channel, as presented in Fig. 9b and e, reveal that bulk FinFET device provides a larger and more uniform current distribution than the planar MOSFET due to the smaller fluctuation of potential. The lateral views of channel, as shown in Fig. 9c and d; f and g, show that the current conducting paths of planar MOSFETs are easily disturbed by discrete dopants. In the bulk FinFET device, even current conducting paths are retarded in parts of channel surface; the tri-gate structure of bulk FinFETs provides more alternative conducting paths that prevent a significant fluctuation of conduction current. Thus, benefiting from the superiority of the vertical channel structure, the bulk FinFET device suppresses potential fluctuations and maintains a more stable conduction current than the planar MOSFET.

Fig. 10 plots the on-/off- state current characteristics of the studied devices. For devices with similar on-state current (I_{on}), the maximum difference of off-state current (I_{off}) is declined from approximately 2000 nA/um–800 nA/um as the EOT is scaled from 1.2 nm to 0.2 nm. Comparing the results for planar MOSFETs with those of bulk FinFETs, even though the planar device with 0.4 nm and 0.2 nm EOT has a better on-off state characteristic, the bulk FinFET device exhibits a smaller current fluctuation (about 600 nA/um). The bulk FinFET device can provide a more uniform potential distribution and a more stable current flow than that of the planar MOSFET. The additional structural improvement of bulk

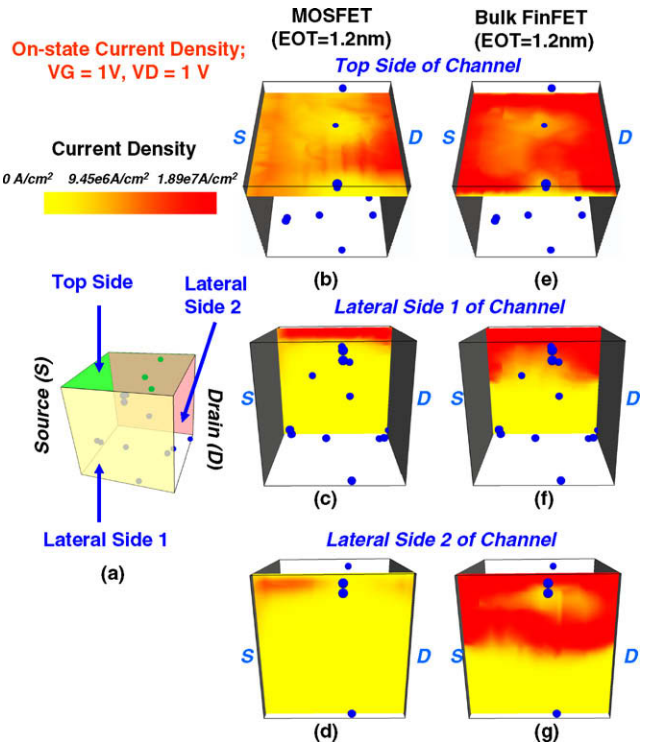

Fig. 9. Cross-sectional views of on-state current density distribution in channel of device, where (b), (c), and (d) show the planar MOSFET device and (e), (f), and (g) show the bulk FinFET device. The corresponding distribution of discrete dopants is shown in (a) and all the cross-section plots are extracted 1 nm below the channel surface.

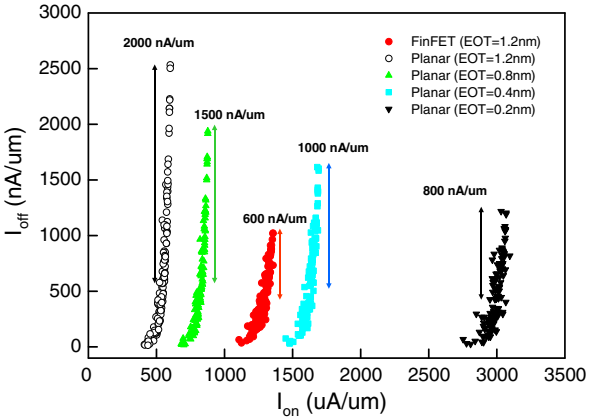

Fig. 10. I_{on}–I_{off} current characteristics of the studied 16-nm-gate planar MOSFET and bulk FinFET devices.

FinFET devices enhances the immunity of device against random-dopant-induced fluctuation, which cannot be evaluated from the trend of gate capacitance.

The process-variation- and random-dopant-induced V_{th} fluctuations are summarized in Fig. 11. In this study, the device with best immunity against process-variation- and random-dopant-induced V_{th} fluctuations are the planar MOSFETs with 0.2 nm EOT and the bulk FinFETs with 1.2 nm EOT. Considering the total V_{th} fluctuation according to the relation of Eq. (1), the V_{th} fluctuation is dominated by random-dopant effect and the bulk FinFETs with 1.2 nm EOT shows a similar immunity against fluctuation with the planar MOSFETs with 0.2 nm EOT, as shown in Fig. 12. Table 2 summarizes the components and total V_{th} fluctuations for the studied

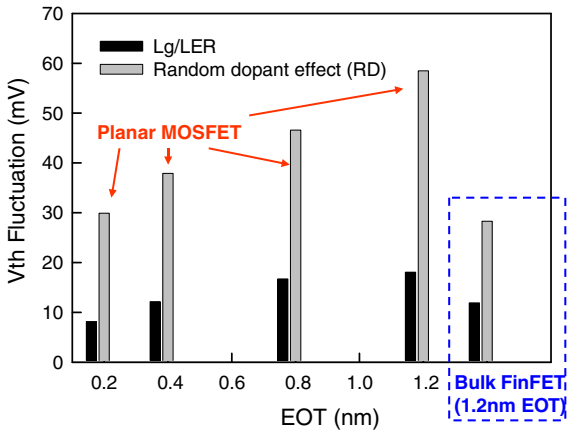

Fig. 11. Components of the V_{th} fluctuation of the explored devices. The right most set of bars are the V_{th} fluctuation of 16 nm bulk FinFET with EOT 8 1.2 nm and the others are the planar MOSFETs with various EOT.

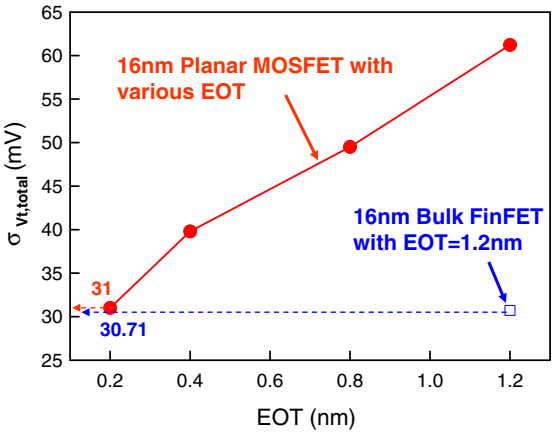

Fig. 12. Total threshold voltage fluctuation for the studied devices.

Table 2
Components of the threshold voltage fluctuation of the explored planar MOSFETs and bulk FinFETs

	Planar MOSFET				Bulk FinFET
EOT (nm)	1.2	0.8	0.4	0.2	1.2
L_g/LER	18.1	16.7	12.2	8.18	12.6
RD	58.5	46.6	37.9	29.9	28.3
Total	61.2	49.5	39.8	31.0	30.7

devices. Result of this study confirms the suppression of fluctuations with the gate oxide thickness scaling. The immunity of the planar MOSFET against fluctuation suffers from nature of structural limitations and the bulks FinFET device can alleviates the challenges of device's scaling and have potential in the nanoelectronics application.

4. Conclusions

The threshold voltage fluctuations caused by the random dopant effect, the gate-length deviation, and the line-edge roughness has been calculated and compared for the nanoscale planar MOSFETs and bulk FinFETs. Fluctuations of the studied planar MOSFETs with EOT from 1.2 nm to 0.2 nm were compared with the results for 16 nm bulk FinFETs. Result of this study has confirmed the suppression of fluctuations with the gate oxide thickness scaling. The

immunity of the planar MOSFET against random-dopant-induced fluctuation suffers from nature of structural limitations. The bulk FinFETs with 1.2 nm EOT shows a similar immunity against fluctuation with the planar MOSFETs with 0.2 nm EOT. Multiple-gate FETs, such as the examined bulk FinFET may alleviate the challenges of device's scaling and could be a potential candidate in the era of nanoelectronics. We notice that for the bulk FinFETs besides the gate-length deviation and line-edge roughness, the effects of Si thickness variation, Si sidewall roughness, and local field enhancement at the top or bottom Si fin are the important sources of fluctuation, which are currently under consideration.

Acknowledgements

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