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Channel-width dependence of low-frequency noise in process tensile-strained *n*-channel metal-oxide-semiconductor transistors

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Low-frequency noise measurement in process tensile-strained *n*-channel metal-oxide-semiconductor field-effect transistors yields the density of the interface states, exhibiting a decreasing trend while decreasing the channel width. This finding corroborates the group of P_b centers caused by the lattice mismatch at (100) Si-SiO$_2$ interface as the origin of the underlying interface states. The inverse narrow width effect appears to be insignificant, substantially confirming the validity of the noise measurement. The present noise experiment therefore points to the enhancement of the tensile strain in the presence of channel narrowing, which in turn reduces the lattice mismatch. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2172287]

Channel strain engineering is currently recognized as an indispensable performance booster in producing next-generation metal-oxide-semiconductor field-effect transistors (MOSFETs).[1] To achieve this goal, two fundamentally different methods have been proposed:[1] (i) Strained silicon (SSi) on a relaxed SiGe buffer layer; and (ii) process strained silicon (PSS) through the trench isolation, silicide, and cap layer. On the other hand, in the areas of unstrained counterparts, low-frequency noise has been extensively utilized since it can provide the opportunity to examine the interfacial physics.[2–4] Thus, it is a challenging issue for the low-frequency noise measurement to find further potential applications in the strain case. Recently, one such study[5] has been demonstrated that an improved noise performance can be achieved on biaxial tensile-strained substrates. In the present work, we conduct a channel-width-dependent low-frequency noise experiment on a process tensile-strained *n*-channel MOSFET. The resulting noise data are useful in addressing the effect of enhanced tensile strain in the channel width direction.

The device under test was an *n*-channel MOSFET fabricated using the concept of process tensile strain, mainly through the trench isolation.[6] The physical gate oxide thickness was 1.4 nm as determined by capacitance-voltage fitting. The channel length was 0.5 μm while the channel width spanned a wide range of 0.11, 0.24, 0.6, 1, and 10 μm. Here, a reduction in channel width means an enhancement in tensile strain in the channel width direction. This can be easily understood by means of the current drive enhancement factor against channel width as shown in Fig. 1. The inset of the figure displays measured drain current per unit channel width versus drain voltage with the gate overdrive as a parameter. As expected, the drain current per unit channel width increases as the channel width is decreased. The in-

creased drain current can be well related to the mobility enhancement; that is, the tensile stress causes subbands energy shift, which in turn suppresses the intervalley phonon scattering while reducing the effective conductivity mass, thereby enhances the mobility.[1,7]

The low-frequency noise measurement setup used was the same as that detailed elsewhere.[4] The measurement frequency ranged from 3 Hz to 100 kHz while operating the devices at a drain voltage of 0.2 V. Here, the noise experiment was carried out in terms of the input-referred noise voltage spectral density S_{Vg}. Figure 2 depicts measured S_{Vg} versus frequency for a gate overdrive of 0.6 V, where three devices, as labeled A, B, and C with the same channel width
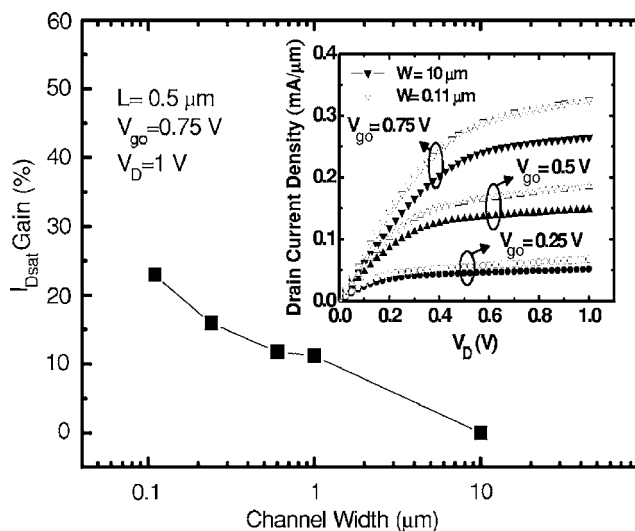

FIG. 1. The experimental drain current enhancement factor vs channel width for gate overdrive $V_{go}=0.75$ V and drain voltage $V_D=1$ V. The inset shows measured drain current per unit channel width vs drain voltage with gate overdrive as a parameter.
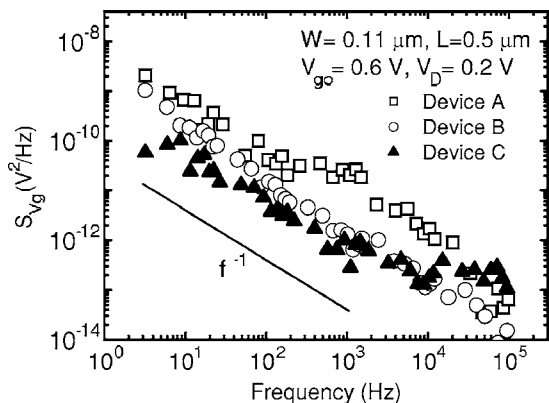
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FIG. 2. The measured input-referred noise voltage spectral density at V_{go} =0.6 V and V_D=0.2 V vs frequency for three different positions on the wafer.

FIG. 4. The extracted effective interface state density corresponding to Fig. 3.

of 0.11 μm, represent three different positions on the wafer. Apparently, a considerable variation of low-frequency noise exists between devices, which can be attributed to statistical fluctuations of the number of the interface traps.[8] Hence, it is argued that the measured noise data essentially can follow the $1/f^\gamma$ relationship with the power coefficient γ close to unity.

Figure 3 shows measured S_{Vg} against channel width for a certain gate overdrive of 0.6 V at a specific frequency of 100 Hz. In this figure, each of the five error bars represents the standard deviation of the distribution created from a total of fifteen samples; and the data point stands for the mean of the distribution. This figure reveals that the low-frequency noise, on the average, increases with decreasing channel width. We also further conducted the case of varying gate overdrive and found that no significant deviation from that in Fig. 3 can be observed, provided that the gate overdrive of more than 0.4 V is applied.

Also shown in Fig. 3 is the corresponding average threshold voltage shift with respect to the wide structure (i.e., 10 μm) such as to address the possibility of the inverse narrow width effect (INWE) caused by the impurity segregation

and the fringing electric field at the isolation sidewall.[9,10] It can be seen that the threshold voltage shift is rather small (<5%), indicating that the inverse narrow width effect is not a significant issue in the undertaken devices. Furthermore, since the noise data are obtained in strong inversion, the channel current part along the edge of the channel is not significant relative to the overall channel one. As a result, the inverse narrow width effect can be substantially weakened. Therefore, it is reasonably drawn that the present low-frequency noise is a good tool to monitor the Si-SiO$_2$ interface over the whole channel area.

The weak dependence of low-frequency noise on gate overdrive (>0.4 V) as mentioned above suggests that the carrier number fluctuations prevail in the strong inversion mode. In other words, under such situations the Coulomb scattering can be ignored due to the screening of the trapped charge by the gate electrode and the inversion-layer charge. Hence, the following input-referred noise voltage spectral density expression can be adequately cited[3,11]

$$S_{Vg} = \frac{q^2 k_B T \lambda}{C_{\text{eff}}^2} \frac{N_t}{WL} \frac{1}{f^\gamma}, \tag{1}$$

where q is the elementary charge, k_B is Boltzman's constant, T is the absolute temperature, λ is the tunneling distance (~0.1 nm), W is the channel width, L is the channel length, C_{eff} is the effective gate oxide capacitance per unit area, and N_t is the effective near-interface oxide trap density. With known $C_{\text{eff}}(\approx 1.75 \ \mu\text{F/cm}^2)$ from the undertaken manufacturing process, fitting all the S_{Vg} data using Eq. (1) led to the distribution of N_t as shown in Fig. 4 versus channel width. Again on the average, the interface state density decreases with decreasing channel width. Specifically, a reduction in channel width by a factor of about 100 produces a tenfold reduction in interface state density. Once again, a reduction in channel width means an enhancement of tensile strain in that direction; therefore, the present noise experiment points to a reduction in interface state density in the presence of enhanced tensile strain in the channel width direction.

It is interesting to further examine the physical origin of the underlying interface states. Analogous to the electron-spin resonance (ESR) experiment on a (111) Si-SiO$_2$ interface,[12–14] the interface states investigated in our low-frequency noise work can be attributed to the group of P_b centers (or equivalently the dangling-bond defects as charac-terized in terms of Si$_3$≡Si·) caused by the lattice mismatch
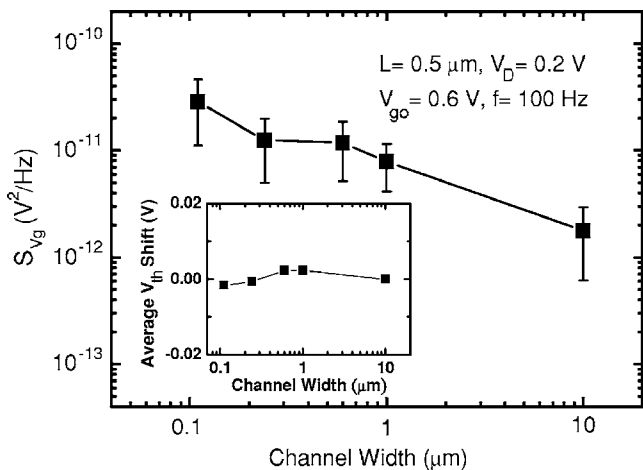

FIG. 3. The measured input-referred noise voltage spectral density at a specific frequency of 100 Hz vs channel width for V_{go}=0.6 V and V_D =0.2 V. The error bar represents the standard deviation of the distribution and the data point the mean of the distribution. The inset shows the corresponding average threshold voltage V_{th} shift with the wide structure (i.e., 10 μm) as a reference point. Here, the threshold voltage was determined at V_D=0.025 V.
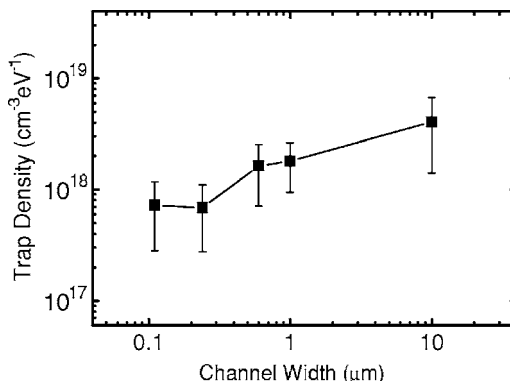
at the (100) Si-SiO$_2$ interface. Here, the lattice-mismatch stress is primarily related to the thermal oxidation process since in this process about 2.2 unit volumes of oxide are produced for each unit volume of silicon consumption. Obviously, the lattice mismatch can be reduced using a tensile strain, thereby leading to a reduction in P_b centers.[14] Note that there were few studies on the usage of the ESR technique to detect P_b centers in the case of (100) Si-SiO$_2$ interface. The noise experiment on the (100) Si-SiO$_2$ interface in this work again corroborates the action of applying a tensile strain: *Enlarging the Si-Si interatomic distance before the silicon oxidation process is carried out, which leads to reduced lattice-mismatch stress during the subsequent thermal oxidation process.*

Channel-width-dependent low-frequency noise measurement has been applied on a process tensile strained n-channel MOSFET. One important finding has been straightforwardly created: *Enhanced tensile strain in the channel narrowing direction can reduce the lattice-mismatch defects.*

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