Overview on Electrostatic Discharge Protection Designs for Mixed-Voltage I/O Interfaces: Design Concept and Circuit Implementations

Ming-Dou Ker, *Senior Member, IEEE,* and Kun-Hsien Lin, *Member, IEEE*

***Abstract*—Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces has been one of the key challenges of system-on-a-chip (SOC) implementation in nano-scale CMOS processes. The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths. This paper presents an overview on the design concept and circuit implementations of the ESD protection designs for mixed-voltage I/O interfaces without using the additional thick gate-oxide process. The ESD design constraints in mixed-voltage I/O interfaces, the classification and analysis of ESD protection designs for mixed-voltage I/O interfaces, and the designs of high-voltage-tolerant power-rail ESD clamp circuit are presented and discussed.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection design, gate-oxide reliability, high-voltage tolerant, mixed-voltage I/O interfaces, power-rail ESD clamp circuit.**

I. INTRODUCTION

TO IMPROVE circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS integrated circuits (ICs). With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mix semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the interfaces between semiconductor chips or sub-systems which have different internal power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O interface circuits must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent the undesired leakage current paths between the chips [3], [4]. For example, a 3.3-V I/O interface is generally required by the ICs realized in CMOS processes with the normal internal power-supply voltage of 2.5 V or 1.8 V. The traditional CMOS I/O buffer with VDD of 2.5 V is shown in Fig. 1(a) with both output and input stages. When an external 3.3-V signal is applied to the I/O pad, the channel of the output pMOS (Mp_out) and the parasitic drain-to-well junction diode in the Mp_out cause the leakage current paths from the I/O pad to VDD, as the dashed lines shown in Fig. 1(a). Moreover, the gate oxides of the output nMOS (Mn_out), the gate-grounded nMOS (Mn1) for input electrostatic discharge (ESD) protection, and the input inverter stage are over-stressed by the 3.3-V input signal to suffer the gate-oxide reliability issue. By using the additional thick gate-oxide process (or called as dual gate-oxide CMOS process [5], [6]), the gate-oxide reliability issue can be avoided. However, the process complexity and fabrication cost are increased.

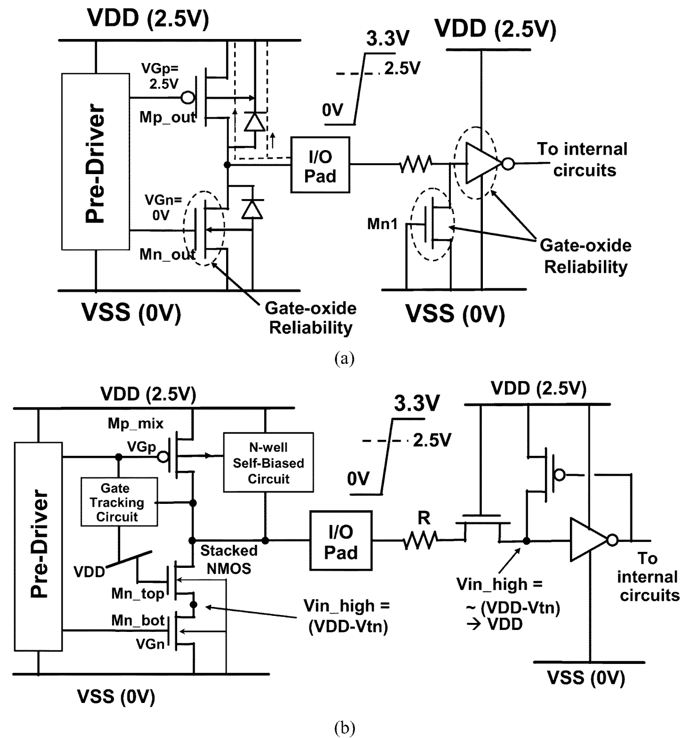

Fig. 1. Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-nMOS and the N-well self-biased pMOS.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-MOS configuration has been widely used in the mixed-voltage I/O circuits [7]–[13]. The typical 2.5 V/3.3 V-tolerant mixed-voltage I/O

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M.-D. Kerr is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

K.-H. Lin is with the Faraday Technology Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

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circuit is shown in Fig. 1(b) [8]. The independent control on the top and bottom gates of stacked-nMOS device allows the devices to meet reliability limitations during normal circuit operation. The gate of top nMOS (Mn_top) in the stacked-nMOS device is biased at VDD (e.g., 2.5 V in a 2.5 V/3.3 V mixed-voltage I/O interface). The gate of bottom nMOS (Mn_bot) is biased at VSS by the pre-driver circuit to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g., 3.3 V in a 2.5 V/3.3 V mixed-voltage I/O interface), the common node between the Mn_top and Mn_bot in the stacked-nMOS structure has approximately a voltage level of VDD-Vth ($\sim$ 1.9 V), where Vth ($\sim$ 0.6 V) is the threshold voltage of nMOS device. Therefore, the stacked-nMOS can be operated within the safe range for both dielectric and hot-carrier reliability limitations. The pull-up pMOS (Mp_mix), connected from the I/O pad to the VDD power line, has the gate tracking circuits for tracking the gate voltage and the n-well self-biased circuits for tracking n-well voltage, which are designed to ensure that the Mp_mix does not conduct current when the 3.3-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. In this paper, an overview on the ESD protection designs for mixed-voltage I/O interface circuits without using the additional thick gate-oxide process is presented. The content covers the ESD design constraints in mixed-voltage I/O circuits, the classification and analysis of the proposed ESD protection designs for mixed-voltage I/O circuits, and the designs for high-voltage-tolerant power-rail ESD clamp circuit.

II. ESD Design Constraints in Mixed-Voltage I/O Circuits

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) [14]. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [15], [16], the turn-on-efficient power-rail ESD clamp circuit was placed between VDD and VSS power lines [17]. The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit is shown in Fig. 2(a), where a PS-mode ESD pulse is applied to the I/O pad. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [17]. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits. Without the diode connected from the I/O pad to VDD in the

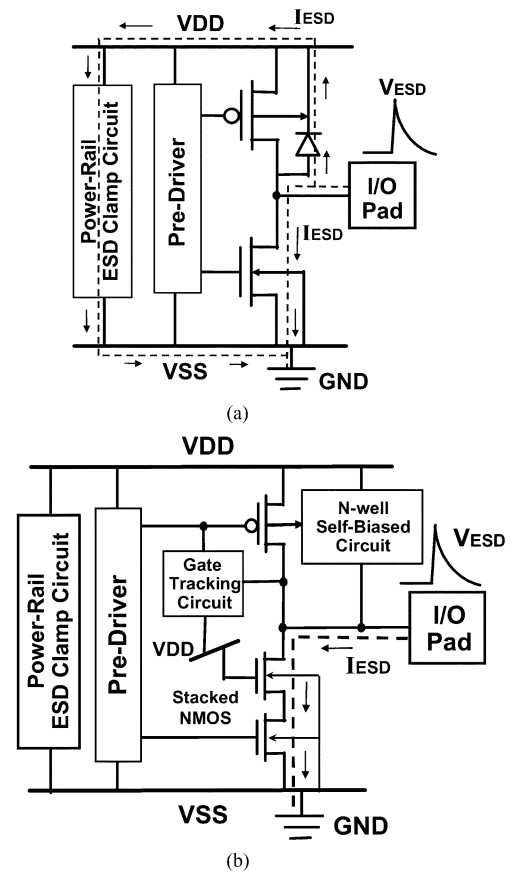

Fig. 2. ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. The ESD current path in the mixed-voltage I/O circuits with power-rail ESD clamp circuit under PS-mode ESD stress in illustrated in Fig. 2(b). Such ESD current at the I/O pad is mainly discharged through the stacked-nMOS by snapback breakdown. However, the nMOS in stacked configuration has a higher trigger voltage and a higher snapback holding voltage, but a lower secondary breakdown current (It2), as compared to that of the single nMOS [18], [19]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD level under PS-mode ESD stress, as compared to the traditional I/O circuits with a single nMOS [18]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses.

The finger-type layout pattern and the corresponding cross-sectional view of stacked-nMOS device in mixed-voltage I/O

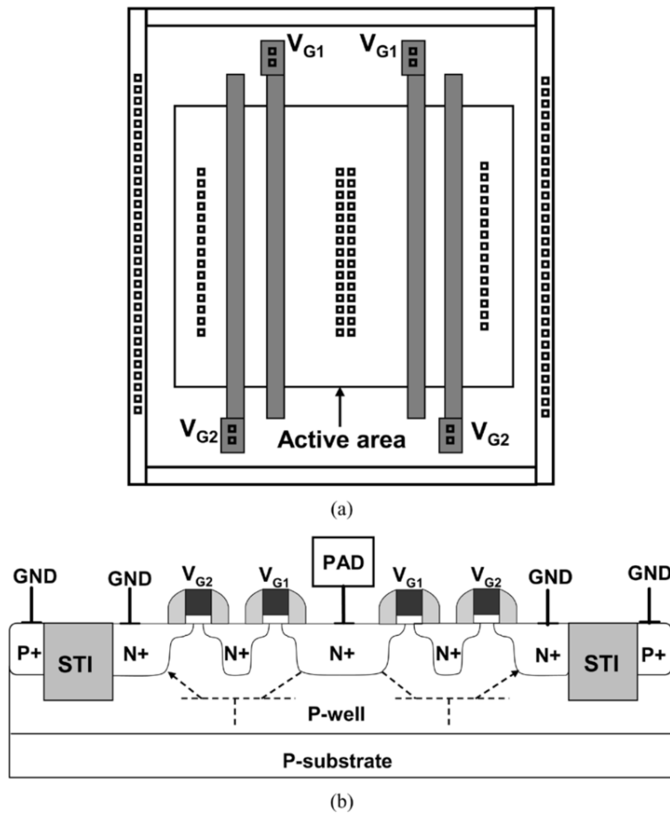

Fig. 3. (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-nMOS device with the shared active configuration for the mixed-voltage I/O circuits in a p-substrate CMOS process.

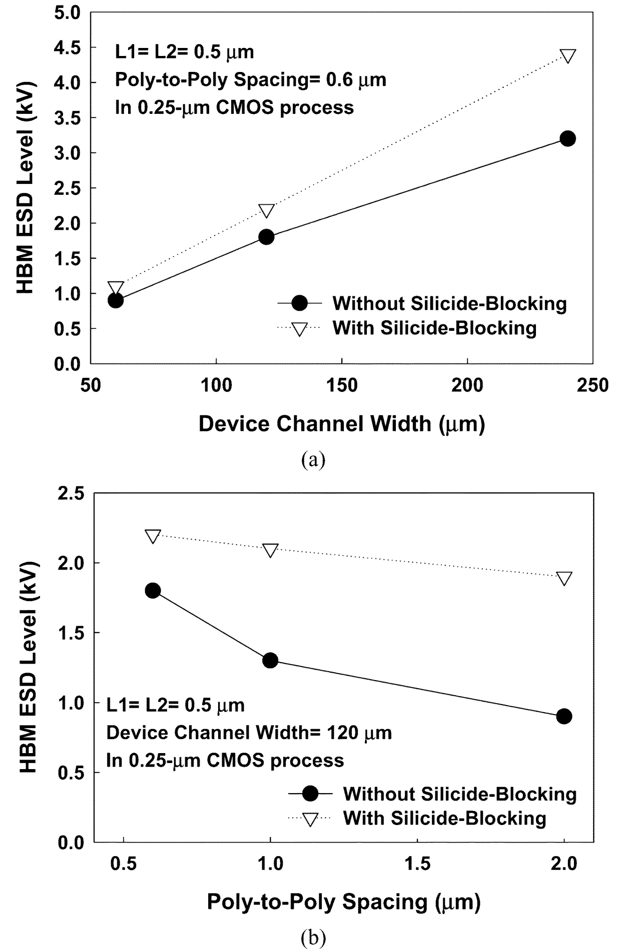

Fig. 4. Comparisons of HBM ESD robustness of the stacked-nMOS device with or without the silicide-blocking process, under (a) different channel widths, and (b) different poly-to-poly spacings, of the stacked-nMOS device fabricated in a 0.25-μm CMOS process.

circuits are shown in Fig. 3(a) and (b). The stacked-nMOS device can be used as both of the pull-down device and ESD protection device in the mixed-voltage I/O circuits. The stacked-nMOS structure includes a first transistor (top nMOS), having a drain connected to an I/O pad, and a gate (V_{G1}) connected to the VDD power supply. A second transistor (bottom nMOS) is merged into the same active area of the first transistor, having a gate (V_{G2}) connected to the pre-driver of the mixed-voltage I/O circuits. The source of the top nMOS and the drain of the bottom nMOS are constructed together by sharing the common $n+$ diffusion region. Under the PS-mode ESD stress condition, the stacked nMOS is operated in snapback breakdown, where the bipolar effect taking place between the drain of the top nMOS and the source of the bottom nMOS. These two diffusions act as the emitter and collector of the parasitic lateral n-p-n bipolar junction transistor (BJT), respectively. The snapback mechanism of stacked-nMOS device for conducting large amounts of ESD current involves both avalanche breakdown and the parasitic n-p-n bipolar junction transistor.

The dependences of the human-body-model (HBM) [14] ESD level on the device channel width and poly-to-poly spacing (common $n+$ diffusion spacing) of stacked-nMOS device in a 0.25-μm CMOS process are shown in Fig. 4. In Fig. 4(a), the HBM ESD level of the stacked-nMOS device is increased while the device channel width is increased. Moreover, the stacked-nMOS device with silicide-blocking process can sustain higher ESD level than that with fully silicided process. The nonuniform turn-on issue of the parasitic n-p-n BJT in stacked-nMOS device can be improved by the silicide-blocking process. In Fig. 4(b), the HBM ESD level of stacked-nMOS device with fully silicided process is decreased obviously while the poly-to-poly spacing is increased. However, the HBM ESD level of stacked-nMOS device with silicide-blocking process is only decreased slightly. The turn-on efficiency and performance of the parasitic n-p-n BJT in stacked-nMOS device can be improved by reducing the poly-to-poly spacing. Although the ESD robustness of stacked-nMOS device can be somewhat improved by layout optimization, the stacked-nMOS device by snapback breakdown still cannot provide efficient ESD protection in the mixed-voltage I/O circuits. By using extra process modification such as ESD implantation, the ESD robustness of stacked-nMOS device can be further improved [20], [21], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top nMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-nMOS device in the mixed-voltage I/O circuits [22]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.

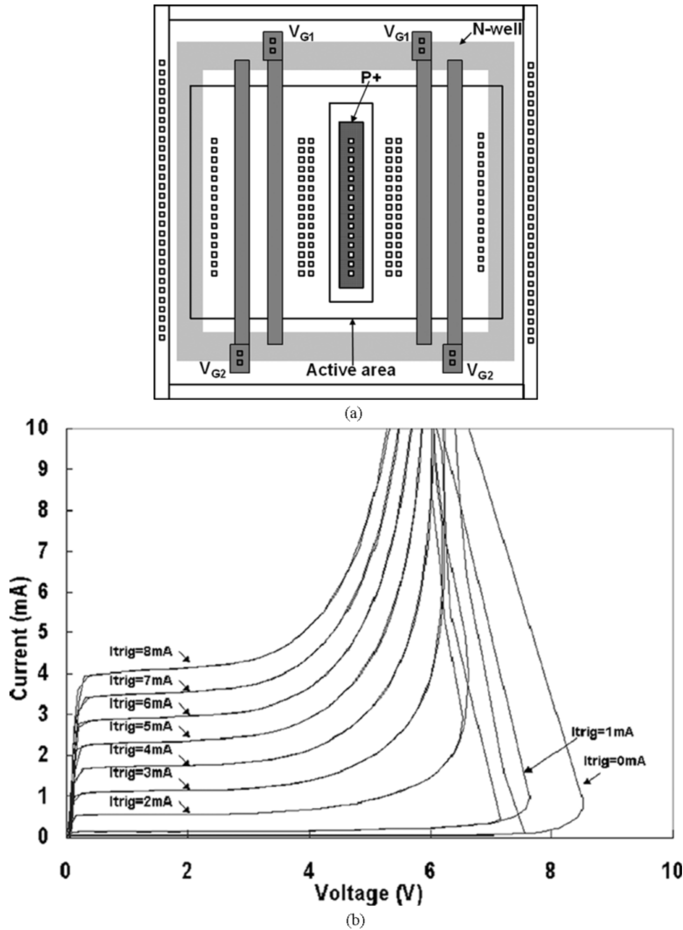

Fig. 5. (a) Finger-type layout pattern of the substrate-triggered stacked-nMOS device for mixed-voltage I/O circuits. (b) Measured I–V characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (Itrig).

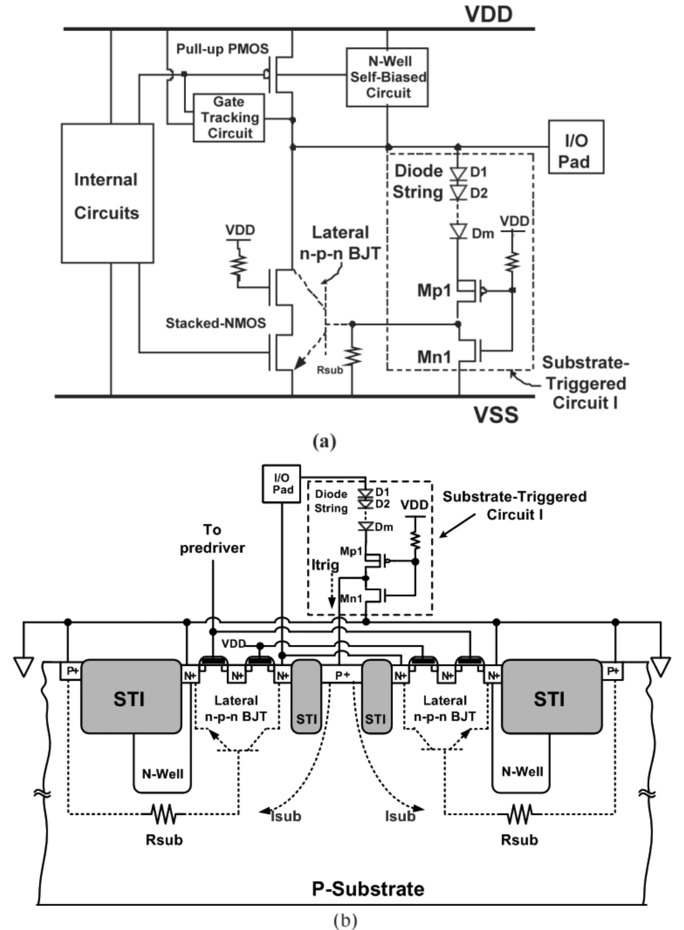

Fig. 6. (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit I for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit I.

III. ESD Protection Designs for Mixed-Voltage I/O Circuits

A. Substrate-Triggered Stacked-nMOS Device

The snapback operation of the parasitic n-p-n BJT in the stacked-nMOS structure can be controlled by its substrate potential. Therefore, the substrate resistance (Rsub) and substrate current are the important design parameters for ESD protection [23]. The substrate-triggered technique [24]–[26] can be used to generate the substrate current in ESD protection circuits. With the substrate-triggered current, the trigger voltage of the stacked-nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection [27], [28]. The finger-type layout pattern of the substrate-triggered stacked-nMOS device is shown in Fig. 5(a). As shown in the layout top view, an additional $p+$ diffusion is inserted into the center drain region of stacked-nMOS device as the substrate-triggered node. The trigger current is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance for improving turn-on efficiency of the parasitic lateral BJT in the stacked-nMOS device. The measured current-voltage $(I$–$V)$ characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (measured by a Tek370A curve tracer) are shown in Fig. 5(b). The trigger voltage of the parasitic n-p-n BJT in the stacked-nMOS device can be effectively decreased while the substrate-triggered current is increased. The substrate-triggered circuit should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough trigger current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked-nMOS device. The substrate-triggered circuit should meet above constraints for providing effective ESD protection to the mixed-voltage I/O interface.

The substrate-triggered circuit I for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 6(a) [27]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate-triggered circuit I is shown in Fig. 6(b). The substrate-triggered circuit I is composed of the diode string, a pMOS Mp1, and an nMOS Mn1, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. Under normal circuit operating condition, the turn-on voltage of the substrate-triggered circuit roughly equals to $V_{\text{pad}} \geqq V_{\text{string}}(I) + |V_{tp}| + VDD$, where $V_{\text{string}}(I)$ is the

total voltage drop across the diodes and V_{tp} is the threshold voltage of the pMOS. The turn-on voltage can be adjusted by varying the numbers of the diodes in the diode string. To satisfy the requirement in the 2.5 V/3.3 V mixed-voltage application, the number of the diodes in the diode string should be adjusted to make the turn-on voltage greater than 3.3 V. When a 3.3-V input voltage is applied at I/O pad, Mp1 is kept off, and the local substrate of the stacked nMOS is biased at VSS by the turn-on of Mn1. With the diode string to block the 3.3-V input voltage at the I/O pad, the Mp1 with thin gate oxide has no gate-oxide reliability issue under normal circuit operating condition. The Mp1 in conjunction with the diode string is used to reduce the leakage current through the substrate-triggered circuit in normal operating condition. The choice of a particular diode string is also determined by the specified pin leakage current at a given temperature. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Under PS-mode ESD stress condition, the gate of the Mp1 has an initial voltage level of $\sim$ 0 V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the Mp1 into the p-substrate, when $V_{\rm pad} \geqq V_{\rm string}(I) + |V_{tp}|$. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of Mp1. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be discharged from the I/O pad to VSS. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been improved from the original 3.4 kV to 5.6 kV in a 0.25-μm CMOS process.

Another substrate-triggered circuit II for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 7(a) [28]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate-triggered circuit II is shown in Fig. 7(b). The substrate-triggered circuit II is composed of the pMOS Mp1, pMOS Mp2, nMOS Mn1, and nMOS Mn2, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. The gates of Mp1 and Mp2 are connected together to VDD through a resistor Rd. In the 2.5 V/3.3 V mixed-voltage IC application, the gates of Mp1 and Mp2 are biased at 2.5-V VDD supply under normal circuit operating condition. When the input voltage transfers from 0 V to 3.3 V at the I/O pad, the gate voltage of Mn1 could be increased through the coupling capacitor C. However, the Mn2 and Mp2 can clamp the gate voltage of Mn1 between $\mathrm{VDD} - V_{tn}$ and $\mathrm{VDD} + |V_{tp}|$, where Vtn is the threshold voltage of nMOS. Once the gate voltage of Mn1 is over VDD + $|V_{tp}|$, the Mp2 will turn on to discharge the over-coupled voltage and to keep the gate voltage within VDD + $|V_{tp}|$. Since the upper boundary on the gate voltage of Mn1 is within VDD + $|V_{tp}|$, the source voltage of Mp1 is clamping below VDD, which keeps the Mp1 always off under normal circuit operation condition. The Mn2 and Mp2 can further clamp the gate voltage of Mn1 to avoid gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level. Under PS-mode ESD-stress condition, the gates of Mp1 and Mp2 have an initial voltage level of $\sim$ 0 V, while the VSS pin is grounded but the VDD pin is floating. The positive ESD transient voltage on the I/O pad is coupled through the capacitor C to the gate of Mn1. In this situation, both of the Mn1 and Mp1 are operated

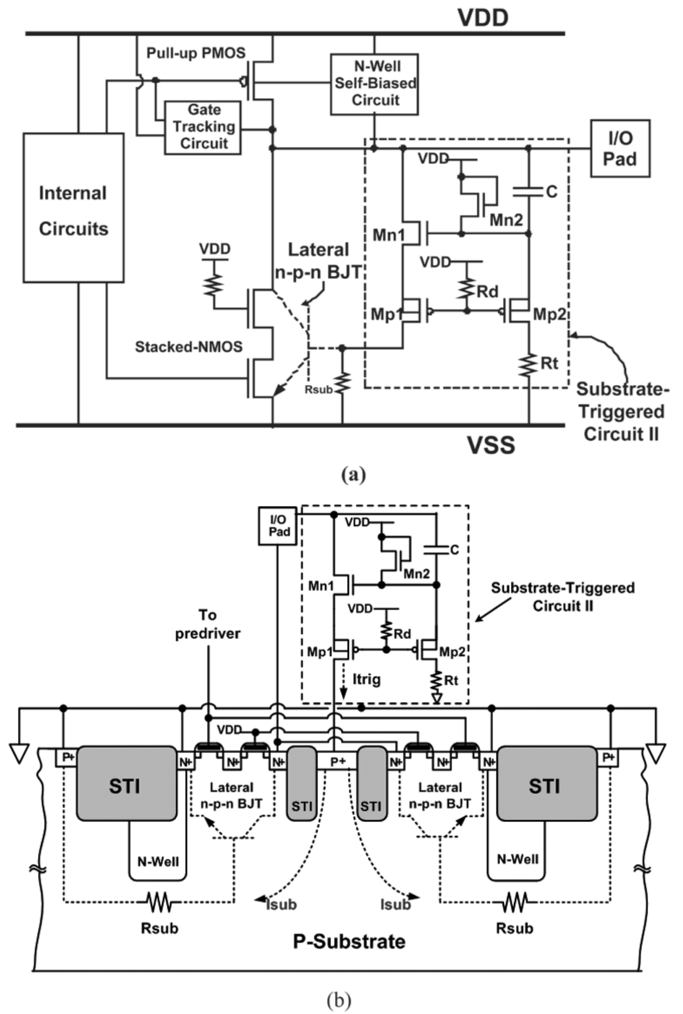

Fig. 7. (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit II for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit II.

in the turn-on state. Therefore, the substrate-triggered circuit II will conduct some ESD current flowing from I/O pad through Mn1 and Mp1 into the p-substrate. The trigger current provided by the substrate-triggered circuit II is determined by the size of Mn1, Mp1, and the capacitor C. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be mainly discharged from the I/O pad to VSS. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been improved from the original 3.5 kV to 5.5 kV in a 0.25-μm CMOS process.

Both two substrate-triggered designs can significantly reduce the trigger voltage and ensure effective ESD protection for the mixed-voltage I/O circuits. By using such substrate-triggered designs, the gates of stacked-nMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n-p-n BJT in the stacked-nMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

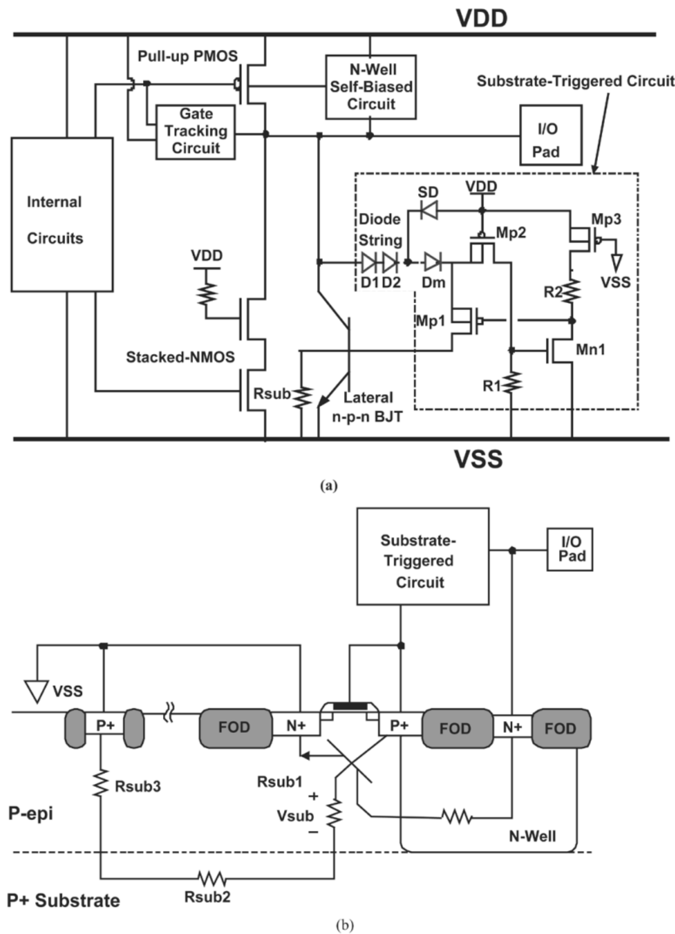

Fig. 8. (a) ESD protection design with substrate-triggered lateral n-p-n BJT device to protect the mixed-voltage I/O circuits. (b) Cross-sectional view of the lateral n-p-n BJT device in a thin-epi CMOS process.

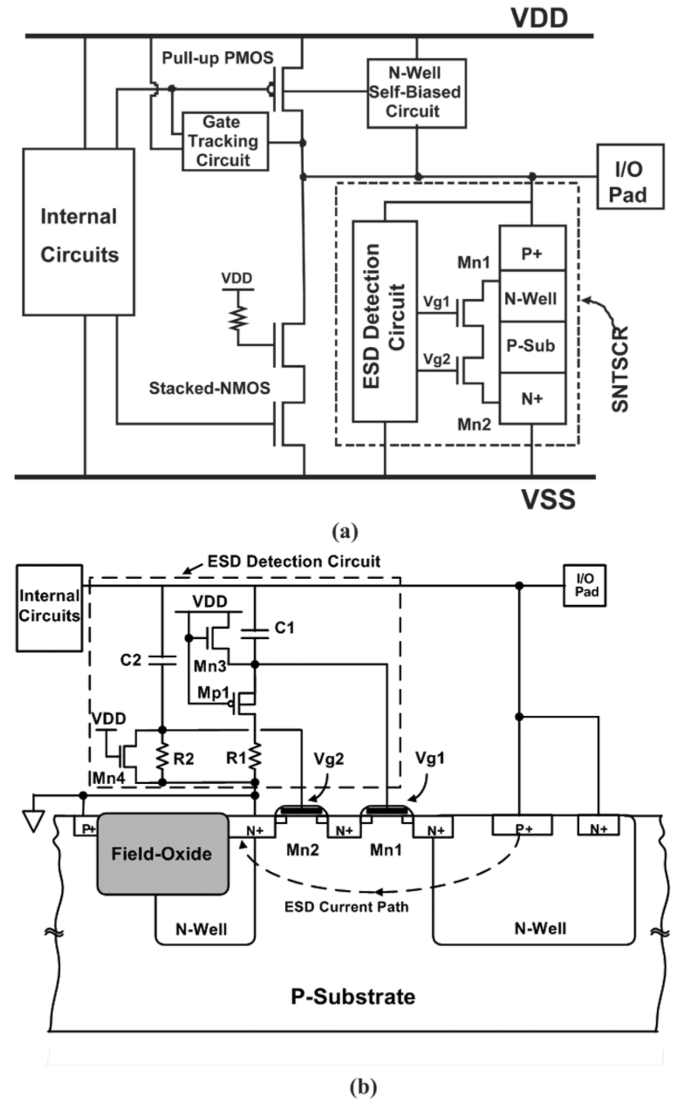

Fig. 9. (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

B. Extra ESD Device Between I/O Pad and VSS

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VSS power line [29], [30]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be directly discharged through this additional ESD device to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through this ESD device to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD.

One ESD protection design with the additional substrate-triggered lateral n-p-n BJT device has been used to protect the mixed-voltage I/O circuits in a fully salicided, 0.35-μm, thin-epi CMOS process [29]. The ESD protection design with substrate-triggered circuit and the lateral n-p-n BJT device for the mixed-voltage I/O circuits is re-drawn in Fig. 8(a). The design concept of this substrate-triggered circuit is similar to that in the aforementioned designs. The substrate-triggered circuit should meet the design constraints for providing effective ESD protection to the mixed-voltage I/O circuits, but without suffering the gate-oxide reliability issue. In this design, the substrate-triggered circuit is mainly composed of the diode string and a pMOS Mp1 to provide the substrate current for triggering on the lateral n-p-n BJT during ESD stress. A positive feedback network is formed with Mp2, Mn1, and R1, which maintains Mp1 in a highly conductive state to provide the substrate current during ESD stress. Moreover, to improve the turn-on efficiency of lateral n-p-n BJT device in a thin-epi CMOS process with much smaller substrate resistance (Rsub), the device structure of lateral n-p-n BJT is specifically designed in Fig. 8(b). The lateral n-p-n BJT device consists of an $n+$ diffusion (emitter), an n-well (collector), and a $p+$ diffusion as its base. A dummy gate is formed between the $p+$ base and $n+$ emitter regions. The collector n-well encloses a portion of the $p+$ base region. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been verified greater than 2 kV in a fully-salicided thin-epi CMOS process.

Another ESD protection design, by using the additional stacked-nMOS triggered silicon controlled rectifier (SNTSCR), has been reported to protect the mixed-voltage I/O circuits [30]. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 9(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 9(b). The ESD

detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the Mn3 in Fig. 9(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2 and Mn4. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the Mp1 is turned on but Mn3 is off since the initial voltage level on the floating VDD line is ~ 0 V. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage of nMOS to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced, so the SNTSCR can be quickly triggered on to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating n-well of the pull-up pMOS in the mixed-voltage I/O circuit, the SNTSCR device can have a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. From the experimental results in a 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8 kV, as compared with that ($\sim$2 kV) of the original mixed-voltage I/O circuits with only stacked nMOS device.

C. Extra ESD Device Between I/O Pad and VDD

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VDD power line [31]–[33]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be discharged through this additional ESD device to VDD power line, and then through the power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be directly discharged through this additional ESD device to the grounded VDD.

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [31], [32], or used to realize the power-rail ESD clamp circuit [34]. The ESD protection design with the diode string connected between the I/O pad and VDD power line for the mixed-voltage I/O circuits is shown in Fig. 10. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the VDD supply voltage. To reduce the turn-on resistance from I/O pad to VDD during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in the mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to VDD through the stacked diodes could trigger on the parasitic vertical p-n-p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p-n-p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 10, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [31], [32].

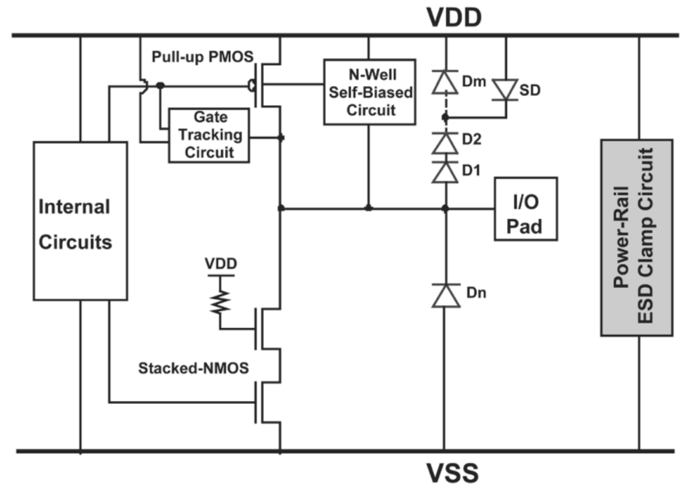

Fig. 10. ESD protection design with the diode string connected between the I/O pad and VDD power line to protect the mixed-voltage I/O circuits. An additional snubber diode (SD) is used to reduce the leakage current of the diode string due to the Darlington amplification.

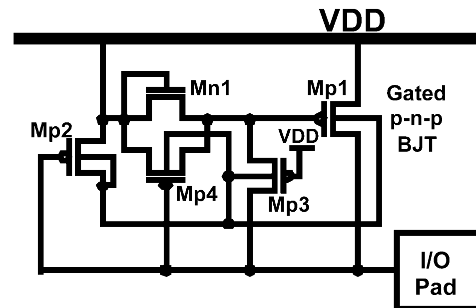

Fig. 11. ESD protection design with gated p-n-p BJT as the ESD protection device connected between I/O pad and VDD to protect the mixed-voltage I/O circuits.

Another ESD protection design, by using the gated p-n-p BJT as the additional ESD device connected between I/O pad and VDD, has been designed to protect the mixed-voltage I/O circuits [33], as that shown in Fig. 11. In this ESD protection design, the pMOS Mp1 acting as ESD clamp device should be kept off to avoid the leakage current path during normal circuit operating condition. Under PD-mode ESD stress condition, the parasitic lateral p-n-p BJT in the device structure of Mp1 is turned on to discharge ESD current. In the 3.6 V/5 V mixed-voltage IC application, when the input voltage at I/O pad is 0 V, the n-well voltage and gate voltage of Mp1 is clamped at VDD (3.6 V) through the turn-on of Mp2 and Mp4. When the input voltage at I/O pad is 5 V, the n-well voltage of Mp1 is maintained at 5-Vd (where Vd is the cut-in voltage of the parasitic drain-to-well diode), and the gate voltage of Mp1 is clamped at 5 V through the turn-on of Mp3. Therefore, this design can meet the gate-oxide reliability constraints without

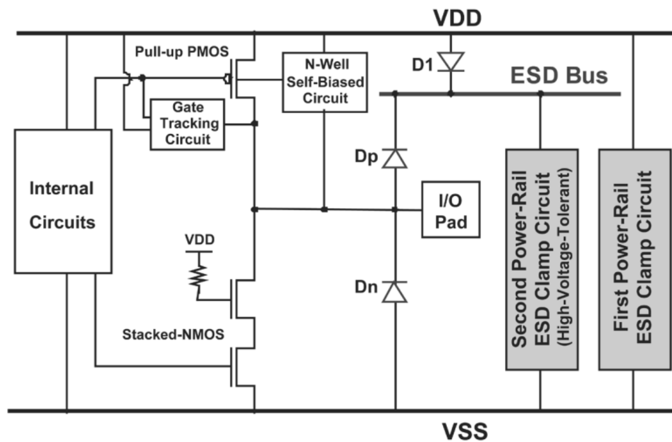

Fig. 12. The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between ESD bus line and VSS power line.

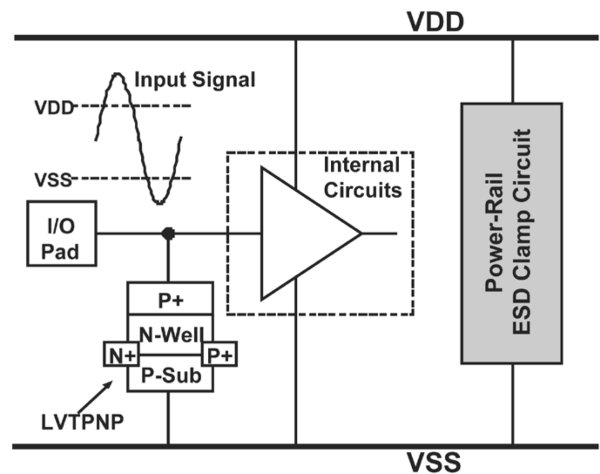

Fig. 13. ESD protection design with the low-voltage-triggered p-n-p (LVTPNP) device for the I/O interfaces with input voltage level higher than VDD or lower than VSS.

leakage current path from I/O pad to VDD during normal circuit operating condition. Under ESD stress condition, the parasitic lateral p-n-p BJT in Mp1 is turned on to discharge ESD current by avalanche breakdown. Such a gated p-n-p BJT should be designed to effectively clamp the overstress ESD pulse without causing ESD damage in the mixed-voltage I/O circuits.

D. ESD Protection Design With ESD Bus

The whole-chip ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application has been reported in [35]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 12. The additional ESD bus line is realized by a wide metal line in CMOS IC [35], [36]. To save layout area, the ESD bus can be realized by the different metal layer, which overlaps the VDD power line. The ESD bus is not directly connected to an external power pin, but biased to VDD through the diode D1 in Fig. 12. The diode D1 connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The diode Dp is connected between I/O pad and ESD bus, whereas the diode Dn is connected between VSS power line and I/O pad. One (the first) power-rail ESD clamp circuit is connected between VDD power line and VSS power line. Another (the second) power-rail ESD clamp circuit is connected between the ESD bus and VSS power line. The second power-rail ESD clamp circuit connected between ESD bus and VSS power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode Dp to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode Dp to the ESD bus, the second power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded VDD. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus.

E. Special Applications

One of the mixed-voltage circuit applications, such as the interface in ADSL, has the input signals with voltage level higher than VDD and lower than VSS. This application limits the ESD diodes connected between the input pad and VDD/VSS power lines. To meet such mixed-voltage I/O interface, the SCR device with floating p-well structure in an n-substrate CMOS process has been used as on-chip ESD protection device [37]. However, the SCR device with a floating well structure is very sensitive to latchup [38], [39]. The mixed-voltage I/O interfaces in the system applications often meet serious overshooting or undershooting signal transition, which could trigger on the SCR device in the ESD protection circuit of I/O pad to induce latchup troubles to the chip [37]. A new ESD protection design, by using the low-voltage-triggered p-n-p (LVTPNP) device, has been proposed to protect such I/O interfaces with input voltage level higher than VDD and lower than VSS [40], as shown in Fig. 13. Comparing to the traditional p-n-p device in CMOS process, the LVTPNP device with a lower breakdown voltage by avalanche breakdown across the p+/n-well or n+/p-sub junctions provides effective discharging path to protect the mixed-voltage I/O interfaces against ESD stresses. During normal circuit operation condition, the LVTPNP device is kept off without causing any leakage current path. In cooperating with the power-rail ESD clamp circuit, the ESD current is discharged through the LVTPNP device by avalanche breakdown under four modes of ESD stresses. The ESD robustness of the LVTPNP device can be further improved by layout optimization.

For high-frequency and analog circuit applications, the high-voltage-tolerant ESD protection design should meet the constraint of low parasitic capacitance. The traditional analog ESD protection with double diodes connected between I/O pad and VDD/VSS power lines [41] cannot meet the high-voltage tolerant requirement. A high-voltage-tolerant ESD protection design, by using the forward-biased diode in series with the stacked-nMOS device, has been reported for analog ESD protection to reduce the input parasitic capacitance [42], as shown in Fig. 14. The equivalent capacitance of analog pin in this design

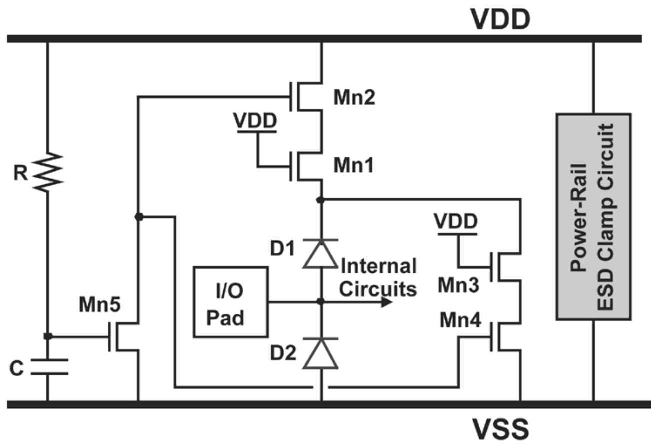

Fig. 14. High-voltage-tolerant ESD protection design with the forward-biased diode in series with one stacked nMOS for analog ESD protection to reduce the input parasitic capacitance.

is approximate the junction capacitance of D1 plus the junction capacitance of D2. The diodes D1 and D2 can be drawn with small layout area, because the ESD current is discharged through these diodes under forward-biased condition. Therefore, the total parasitic input capacitance seen by the analog pin was reduced. The gates of Mn1 and Mn3 are connected to VDD to meet the gate-oxide reliability. The gates of Mn2 and Mn4 are grounded by the dynamic-floating-gate technique [43] to improve turn-on uniformity among the multiple fingers of the stacked nMOS device. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked nMOS (Mn3 and Mn4) to the grounded VSS. The ESD current at the I/O pad under PD-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked nMOS (Mn1 and Mn2) to the grounded VDD. Because the ESD current is discharged through the stacked-nMOS device by snapback breakdown in this design, the turn-on efficiency and ESD robustness of stacked-nMOS devices (Mn1–Mn4) need to be further improved by the additional ESD-implantation process [44].

IV. Comparison Among the Designs

The comparison among various ESD protection designs for mixed-voltage I/O circuits has been summarized in Table I. The evaluated parameters are explained as following.

- ESD implantation required: Is this design realized with the additional ESD-implantation process? “Yes” or “No”
- Design complexity:
  - “Easy”: The stand-alone stacked-nMOS device is the ESD protection circuit without extra auxiliary circuit.
  - “Low”: Needs the well-designed ESD protection device or auxiliary circuit and such design is quite simple.
  - “Middle”: Needs the well-designed ESD protection device or auxiliary circuit and such design is deliberate.
  - “High”: Needs the well-designed ESD protection device or auxiliary circuit and such design is complicated.
- ESD level: Evaluates the ESD performance of the design.
- Area efficiency: Evaluates the total layout area of the ESD protection design if the HBM ESD level of this design is set to 2 kV.

The first consideration of on-chip ESD protection design for mixed-voltage I/O circuits is to meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit can provide effective ESD protection to the internal circuits. The performance of the proposed designs can be evaluated by the above parameters. For high-speed I/O applications with low parasitic capacitance and system-on-a-chip (SOC) applications with a much larger chip size but a reduced cell pitch for I/O cell, the SNTSCR design [30] will be a better choice to protect the mixed-voltage I/O circuits in the nanoscale CMOS technology.

V. High-Voltage-Tolerant Power-Rail ESD Clamp Circuit

In aforementioned description, the turn-on-efficient power-rail ESD clamp circuit is much helpful to improve ESD robustness of the mixed-voltage I/O circuits under the four modes of pin combination in ESD test. For some mixed-voltage circuit applications, the power supply voltage may exceed the ordinary VDD of the process to drive a high-voltage output signal [45]. Therefore, it is required to design the high-voltage-tolerant power-rail ESD clamp circuit with low-voltage devices but without suffering the gate-oxide reliability issue. In the high-voltage-tolerant power-rail ESD clamp circuit, the standby leakage current between the power rails is an important concern, especially when the IC is operating at high-temperature environment.

The diode string in stacked configuration has been used as the power-rail ESD clamp circuit [34]. However, the Darlington bipolar amplification of the parasitic p-n-p BJT devices in the diode string induces a huge leakage current between the power rails. To reduce the leakage current of the diode string between the power rails, some modified designs, such as the Cladded diode string, Boosted diode string, and Cantilevered diode string, were reported in [34]. An improved design by adding an nMOS-controlled SCR device into the diode string to significantly reduce the leakage current between the power rails was reported in [46]. Besides, with the extra triple well in the process technology, the leakage current of the diode string can be further reduced [47].

The stacked-MOS configuration has been also used in the high-voltage-tolerant power-rail ESD clamp circuit [48]–[50]. Besides the gate-oxide reliability issue, how to improve the turn-on efficiency of the stacked-MOS structure during ESD stress and how to have a low standby leakage current between the power rails during normal circuit operating condition will be the design challenges.

One high-voltage-tolerant power-rail ESD clamp circuit realized with the stacked-pMOS structure has been reported [48], [49], as shown in Fig. 15. In this power-rail ESD clamp circuit, the stacked-pMOS structure (Mp1 and Mp2) with large device width is designed to discharge ESD current between the power line VDD_h and VSS under ESD stress. The Mp3 and Mp4 are the long-channel devices which divide the high power supply voltage (VDD_h) by two for the midpoint with consideration of minimal leakage current. The gates of Mp1 and Mp2 are individually controlled by the *RC*-based ESD detection circuits. During

TABLE I
COMPARISON AMONG THE ESD PROTECTION DESIGNS FOR MIXED-VOLTAGE I/O CIRCUITS

ESD Protection Designs for Mixed-Voltage I/O Circuits		ESD Implantation Required	Design Complexity	ESD Level	Area Efficiency
Stacked-nMOS Device [18], [19]		No	easy	poor	poor
Stacked-nMOS Device with ESD Implantation [20], [21]		Yes	easy	good	middle
Substrate-triggered Stacked-nMOS Device	Substrate-triggered Circuit I [27]	No	low	better	better
	Substrate-triggered Circuit II [28]	No	middle	better	better
Extra ESD Device between I/O Pad and VSS	Substrate-triggered n-p-n BJT [29]	No	middle	better	good
	SNTSCR [30]	No	middle	best	better
Extra ESD Device between I/O Pad and VDD	Diode String with SD [31], [32]	No	low	better	better
	Gated p-n-p BJT [33]	No	high	Middle	middle
ESD Protection Design with ESD Bus [35], [36]		No	middle	better	good
Special Applications I: V_{input} >VDD and V_{input} <VSS	LVTPNP Device [40]	No	low	middle	middle
Special Applications II: Low Input Parasitic Capacitance	Diode in Series with Stacked-nMOS Device [42]	Yes	low	middle	middle

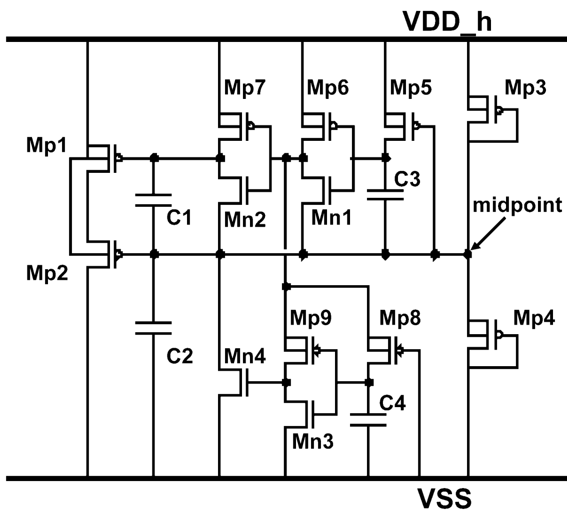

Fig. 15. High-voltage-tolerant power-rail ESD clamp circuit realized with stacked-pMOS structure for the power line (VDD_h) of twice the ordinary VDD.

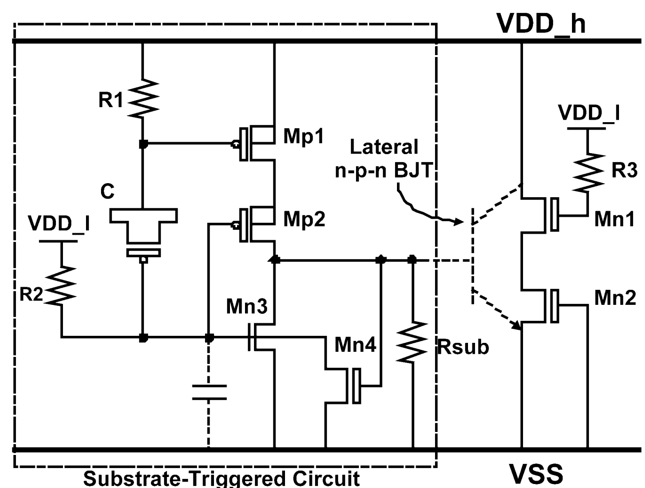

Fig. 16. High-voltage-tolerant power-rail ESD clamp circuit realized with the substrate-triggered stacked-nMOS device. The power-rail ESD clamp circuit is realized by only 1-V and 2.5-V devices for the 3.3-V power line (VDD_h) without suffering the gate-oxide reliability.

normal circuit operating condition, the gate of top pMOS Mp1 is biased at VDD_h, and the gate of bottom pMOS Mp2 is biased at half of VDD_h. Therefore, the Mp1 and Mp2 are kept off without the gate-oxide reliability issue. Under ESD stress condition, both gates of Mp1 and Mp2 are initially biased at ~ 0 V by the ESD detection circuits, therefore the ESD current is discharged through the turned-on stacked-pMOS structure. The design concept of stacked-pMOS configuration can be further applied to implement the power-rail ESD clamp circuit for $3 \times$ VDD power line [48]. The standby leakage current through the voltage divider in the ESD detection circuit between the power-rails should be further reduced for low-power applications.

Substrate-triggered stacked-nMOS design can be also applied to implement the high-voltage-tolerant power-rail ESD clamp circuit [50], as shown in Fig. 16. In this design, the power-rail ESD clamp circuit is realized by using only 1-V and 2.5-V devices for the power line of 3.3 V (VDD_h). The internal power supply voltage is only 1 V (VDD_l). The stacked-nMOS structure is formed by two 2.5-V nMOS transistors (Mn1 and Mn2). During normal circuit operating condition, the gate of top nMOS Mn1 is biased at VDD_l, and the gate of bottom nMOS Mn2 is biased at VSS. Therefore, the stacked-nMOS structure has no gate-oxide reliability problem under the power bias of VDD_h (3.3 V). The substrate-triggered circuit is composed of the two

2.5-V pMOS devices (Mp1 and Mp2), to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS structure during ESD stress. The gates of Mp1 and Mp2 are individually controlled by the *RC*-based detection circuit. During normal circuit operating condition, the substrate-triggered circuit can meet the gate-oxide reliability constraints and the local substrate of the stacked nMOS is biased at VSS by the turn-on of Mn3. Under ESD stress condition, both the gates of Mp1 and Mp2 have the initial voltage level of ~ 0 V, while the VSS pin is grounded but the VDD_l pin floating. The substrate-triggered circuit will provide the trigger current flowing through the Mp1 and Mp2 into the p-substrate. The Mn4 is added in the substrate-triggered circuit to keep the Mn3 off and Mp2 in a conductive state under ESD stress condition. Once the parasitic n-p-n BJT in the stacked-nMOS structure is triggered on, the ESD current is discharged from the VDD_h power line to the grounded VSS. By this design, the turn-on-efficient high-voltage-tolerant power-rail ESD clamp circuit can be realized with an extremely low leakage current. Such a high-voltage-tolerant power-rail ESD clamp circuit can be used as the second power-rail ESD clamp circuit of Fig. 12 cooperating with the ESD bus for the mixed-voltage I/O buffer to receive $3 \times$ VDD input signals [51].

VI. Conclusion

This paper presents a comprehensive overview on the ESD protection designs for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. To design the efficient ESD protection circuit for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important challenge to SOC implementation in the nanoscale CMOS technology.

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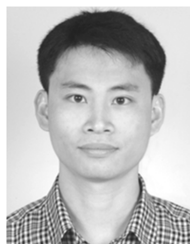
Ming-Dou Ker (S’92–M’94–SM’97) received the B.S. degree from the Department of Electronics Engineering and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

In 1994, he joined the VLSI Design Department of the Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan, as a Circuit Design Engineer. In 1998, he became a Department Manager in the VLSI Design Division of CCL/ITRI. In 2000, he joined the faculty of Department of Electronics Engineering, National Chiao-Tung University, Hisnchu, Taiwan. Currently he is a Full Professor in the Department of Electronics Engineering, National Chiao-Tung University. In the field of reliability and quality design for CMOS integrated circuits, he has published over 250 technical papers in international journals and conferences. He has invented over 180 patents on reliability and quality design for integrated circuits, which have granted with 98 U.S. patents and 115 R.O.C. (Taiwan) patents. His current research topics include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, especial sensor circuits, and on-glass circuits for system-on-panel applications in TFT LCD display. Dr. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the Science-Based Industrial Park, Hsinchu, Taiwan; in the Silicon Valley, San Jose, California, USA; in Singapore; and in the Mainland China.

Dr. Ker has served as member of the Technical Program Committee and Session Chair of numerous international conferences (including IEEE ISCAS, IEEE AP-ASIC, IEEE SOC, IEEE IRPS, IEEE ISQED, IPFA, EOS/ESD Symp., VLSI-TSA, …). Dr. Ker has served as the Chair of RF ESD committee of 2004 *International EOS/ESD Symp.*, and the vice-Chair of Latchup committee for 2005 *IEEE International Reliability and Physics Symp.* (IRPS). He also served as the Technical Program Committee Chair of 2002 Taiwan ESD Conference, the General Chair of 2003 Taiwan ESD Conference, the Publication Chair of 2004 IPFA, and the ESD Program Chair of 2004 International Conference on Electromagnetic Applications and Compatibility. He was the Organizer of the Special Session on *ESD Protection Design for Nanoelectronics and Gigascale Systems* in ISCAS 2005. He was elected as the President of *Taiwan ESD Association* in 2001. Dr. Ker has received many research awards from ITRI, National Science Council, National Chiao-Tung University, and the Dragon Thesis Award from Acer Foundation. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan by Junior Chamber International (JCI).



Kun-Hsien Lin (S’03–M’05) received the B.S. degree from the Department of Electronics Engineering and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1996, 1998, and 2005, respectively.

In 2000, he joined Taiwan Semiconductor Manufacturing Company (TSMC), as a Product Engineer responsible for the CMOS imaging products. In 2002, he joined the SoC Technology Center (STC), Industrial Technology Research Institute (ITRI), as an ESD Protection Design Engineer. Currently, he is a Senior Design Engineer in the Intellectual Property Development Department, Faraday Technology Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C. His main research includes on-chip ESD protection designs in advanced nano-scale and high-voltage CMOS processes.

Dr. Lin’s Ph.D. dissertation was awarded with the Dragon Thesis Award by Acer Foundation, Taiwan, R.O.C., in 2005.