A New Lossy Substrate De-Embedding Method for Sub-100 nm RF CMOS Noise Extraction and Modeling

Jyh-Chyurn Guo and Yi-Min Lin

***Abstract*—A new equivalent circuit method is proposed in this paper to de-embed the lossy substrate and lossy pads' parasitics from the measured RF noise of multifinger MOSFETs with aggressive gate length scaling down to 80 nm. A new *RLC* network model is subsequently developed to simulate the lossy substrate and lossy pad effect. Good agreement has been realized between the measurement and simulation in terms of *S*-parameters and four noise parameters, $\mathrm{NF}_{\min}$ (minimum noise figure), R_n (noise resistance), $\mathrm{Re}(Y_{\mathrm{sopt}})$, and $\mathrm{Im}(Y_{\mathrm{sopt}})$ for the sub-100-nm RF nMOS devices. The intrinsic $\mathrm{NF}_{\min}$ extracted by the new de-embedding method reveal that $\mathrm{NF}_{\min}$ at 10 GHz can be suppressed to below 0.8 dB for the 80-nm nMOS attributed to the advancement of f_T to 100-GHz level and the effectively reduced gate resistance by multifinger structure.**

***Index Terms*—De-embedding, noise, pad, RF CMOS, substrate.**

I. Introduction

THE aggressive CMOS device scaling to sub-100-nm regime has driven dramatic reduction of gate delay to approach 10 ps ($1\ \mathrm{p} = 10^{-12}$) and the remarkable increase of the unit-current-gain cutoff frequency (f_T) to well beyond 100 GHz [1]–[4]. However, it turns out a difficult task to extract RF CMOS noise accurately while its scalability with device scaling is quite important for low noise RF circuit design. The challenges arise from the strong dependence of RF noise on the parasitic and coupling effect associated with gate, substrate, interconnect, and pads, etc. [5]–[7] One of the primary noise sources comes from the gate resistance generated thermal noise and multifinger structures are generally used to reduce the gate resistance. In our paper, excess noise was identified to be critically related to the lossy pad and lossy substrate. The excess noise may dominate in sub-100 nm CMOS devices. A noise correlation matrix method [8] was proposed to de-embed these effects but the complicated matrices calculation sometimes suffers fluctuation at very low noise level and poor accuracy in frequency dependence. A previous study on pad de-embedding using matrices correlation method [6] revealed dramatic fluctuation of $\mathrm{NF}_{\min}$ in a wide range of 0.5–1.5 dB and smoothing was reported to get reasonable frequency dependence. In this paper, we propose a new method to de-embed pads' parasitic capacitance and substrate loss. We have established an equivalent circuit model to incorporate the lossy pad and lossy substrate effect. Good match with the measured extrinsic characteristics such as *S*-parameters and noise parameters has been achieved by ADS simulation for RF MOSFETs with different finger numbers using this lossy substrate equivalent circuit model. The intrinsic MOSFET model was obtained by subtracting all the parasitics from the extrinsic MOSFET. Our method can achieve agreement with the Fukui's model and is free from fluctuation over frequencies even for noise level down to below 1 dB that is generally suffered by the noise correlation matrix method. In addition, our results suggest that the as-measured extrinsic minimum noise figure ($\mathrm{NF}_{\min}$) without de-embedding was dominated by the lossy substrate and lossy pad effect as revealed by the particularly worse $\mathrm{NF}_{\min}$ of near 6 dB at 10 GHz measured from the smallest MOSFETs with finger number as small as 6 ($N_F = 6$). By using the new de-embedding method, the extracted intrinsic $\mathrm{NF}_{\min}$ do show an extremely low value of around 0.6–0.8 dB at 10 GHz for the 80 nm nMOS with gate biases optimized corresponding to different finger numbers (N_F). This lossy substrate de-embedding method is useful for accurate intrinsic noise extraction and modeling that is critically important to improve RF circuit simulation accuracy for low noise RF circuit design.

II. Device Characterization and Modeling Flow

To study the nanoscale CMOS scaling effect on speed and noise, sub-100-nm n-MOSFETs of gate length at 80 nm are used. Multifinger structures are employed to reduce the gate resistance generated RF noise. The finger width is fixed at 4 μm and finger numbers of 6, 18, 36 and 72 ($N_F = 6$, 18, 36, 72) are designed for study of performance optimization. Fig. 1 illustrates the flow chart to explain the device characterization and modeling procedure for this paper. At first, current–voltage (I–V) characterization was done to extract the transconductance (g_m) that is a key parameter governing f_T and noise figure. The gate bias (V_{gs}) corresponding to the maximum g_m for various N_F was around 0.7 V and drain bias (V_{ds}) was fixed at $V_{\mathrm{dd}} = 1.0$ V. Following the bias conditions and dc characterization, *S*-parameters were measured by using HP8510C vector network analyzer up to 40 GHz. Open and short de-embedding were done on the measured two port *S*-parameters to extract the

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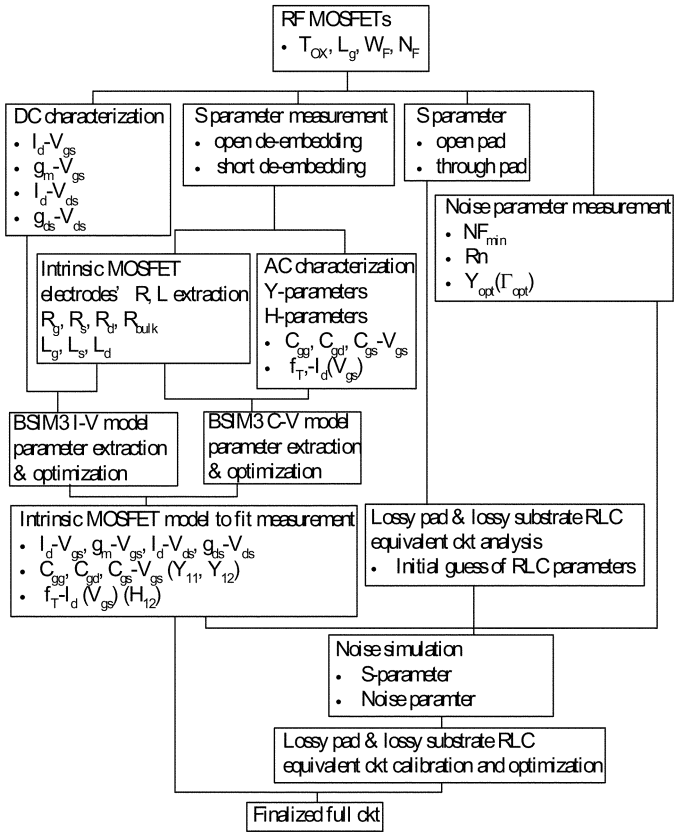


Fig. 1. Flow chart of RF MOSFET characterization and modeling.

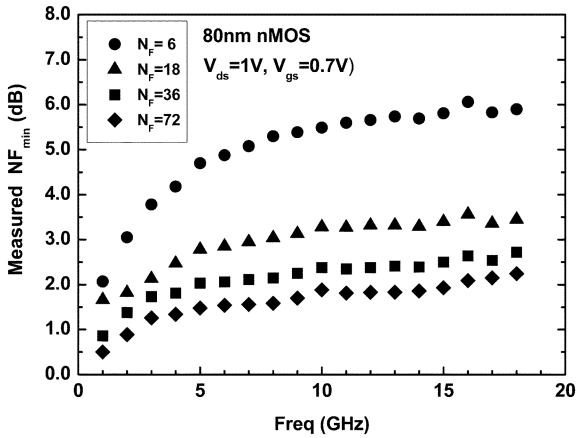
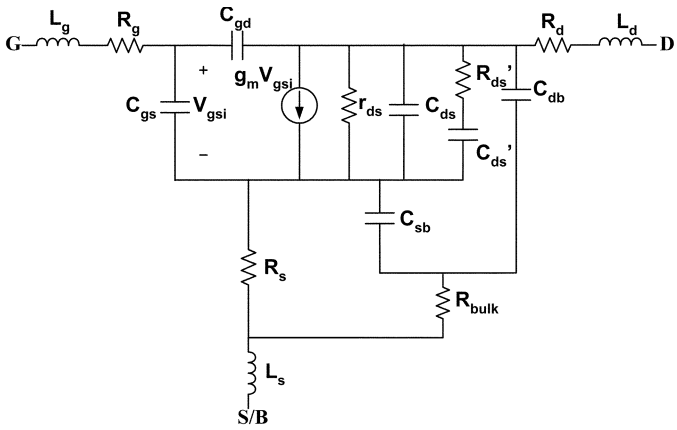


Fig. 2. Measured $\mathrm{NF_{min}}$ versus frequency for 80-nm n-MOSFETs with finger numbers of 6, 18, 36, 72 ($N_F = 6$, 18, 36, 72. Bias condition: $V_{\mathrm{ds}} = 1.0$ V, $V_{\mathrm{gs}} = 0.7$ V.



$$\mathrm{Re}(Z_{12}) = R_s + \frac{A_s}{\omega^2 + B} \tag{1}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_d + \frac{A_d}{\omega^2 + B} \tag{2}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g + \frac{A_g}{\omega^2 + B} \tag{3}$$

$$\frac{1}{\omega}\mathrm{Im}(Z_{12}) = L_s - \frac{E_s}{\omega^2 + B} \tag{4}$$

$$\frac{1}{\omega}\mathrm{Im}(Z_{22} - Z_{12}) = L_d - \frac{E_d}{\omega^2 + B} \tag{5}$$

$$\frac{1}{\omega}\mathrm{Im}(Z_{11} - Z_{12}) = L_g - \frac{E_g}{\omega^2 + B} - \frac{F_g}{\omega^2(\omega^2 + B)} \tag{6}$$

$$B = \left[\frac{g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}\right]^2$$

$$A_s = \frac{C_{gd}[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})]}{[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}]^2}$$

$$A_d = \frac{C_{gs}[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})]}{[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}]^2}$$

$$A_g = \frac{C_{ds}[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})]}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}^2} - \frac{g_{ds}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}$$

$$E_s = \frac{C_{gd}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}$$

$$E_d = \frac{C_{gs}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}$$

$$E_g = \frac{C_{ds}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}$$

$$F_g = \frac{g_{ds}[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})]}{[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}]^2}$$

Fig. 3. MOSFET small signal equivalent circuit model. Equations for parasitic R and L extraction from measured *Z*-parameters.

intrinsic ac characteristics in terms of *Y*-parameters for capacitance–voltage (C–V) model parameter extraction and *H*-parameters for f_T determination. *Z*-parameters of the intrinsic MOSFETs were obtained from *S*-parameters after de-embedding and used to extract the electrodes' R and L such as R_g, R_s, R_d, L_g, L_s, and L_d. The intrinsic MOSFET incorporating the parasitic R, L as extracted was adopted by ADS simulation to do I–V and C–V model parameter extraction and optimization simultaneously. The accuracy of intrinsic MOSFET model has been extensively verified and validated by good match with the measurement in terms of $I_d - V_{\mathrm{gs}}$, $g_m - V_{\mathrm{gs}}$, $I_d - V_{\mathrm{ds}}$, $g_{\mathrm{ds}} - V_{\mathrm{ds}}$, C_{gg}, C_{gd}, $C_{\mathrm{gs}} - V_{\mathrm{gs}}$, and $f_T - I_d(V_{\mathrm{gs}})$, etc. (not included due to limited pages). The noise parameters ($\mathrm{NF_{min}}$, R_n, and Y_{opt} or Γ_{opt}) were measured by ATN-NP5B system to 18 GHz that covers the important frequency band from handset to wireless LAN and future *X*-band communication. A through (thru) line was proposed in the equivalent circuit to emulate the transmission line between RF probe pad and the gate terminal. In this paper, we propose a new *RLC* equivalent circuit to model the lossy substrate, lossy pad, and thru lines parasitic to de-embed

TABLE I

80 nm RF nMOS SMALL-SIGNAL AND RF PERFORMANCE PARAMETERS, R_g, R_s, g_m, $C_{\rm gs}$, $C_{\rm gd}$, f_T, AND $\rm NF_{min}$. f_T ARE EXTRACTED BY UNIT-CURRENT-GAIN $|H_{21}| = 1$ AND CALCULATED BY ANALYTICAL FORM OF $g_m/2\pi\left(C_{\rm gg}^2 - C_{\rm gd}^2\right)^{1/2}$. $\rm NF_{min}$ ARE CALCULATED BY FUKUI'S MODEL OF $F_{\rm min} = 1 + k * f/f_T[g_m(R_g + R_s)]^{1/2}$, $\rm NF_{min} = 10 * \log(F_{min})$ BASED ON THE EXTRACTED f_T

L=80nm, W_F=4μm						$g_m/2\pi(C_{gg}^2-C_{gd}^2)^{1/2}$	max f_T, H_{21}=1	$NF_{min}(dB)=10*\log F_{min}$, $F_{min}=1+K*f/f_T[g_m(R_g+R_S))^{1/2}$, (K=2)			
N_F	$R_g(\Omega)$	$R_S(\Omega)$	Max g_m(mS)	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	(GHz)	f = 1GHz	f = 2.4GHz	f = 5.8GHz	f = 10GHz
6	26.56	1.23	23.46	35.81	7.35	87.8	86	0.0808	0.1914	0.4490	0.7474
18	11.05	0.83	66.3	78.02	26.98	104.0	108	0.0708	0.1680	0.3954	0.6607
36	6.27	0.73	126.98	142.04	57.96	105.6	104	0.0780	0.1849	0.4341	0.7234
72	3.98	0.67	233.12	254.31	125.69	103.5	102	0.0878	0.2078	0.4861	0.8070

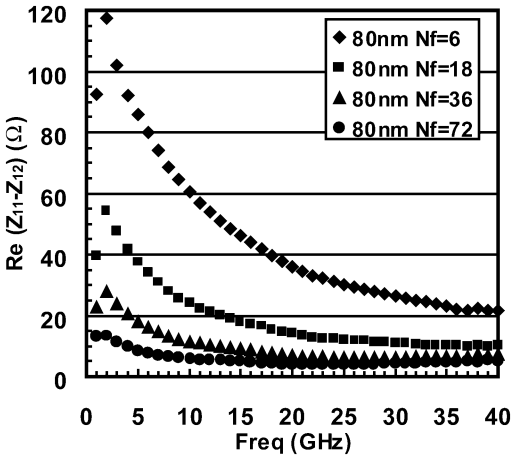


Fig. 4. Gate resistance R_g extracted from *Z*-parameters for 80-nm MOSFET with $N_F = 6$, 18, 36, 72.

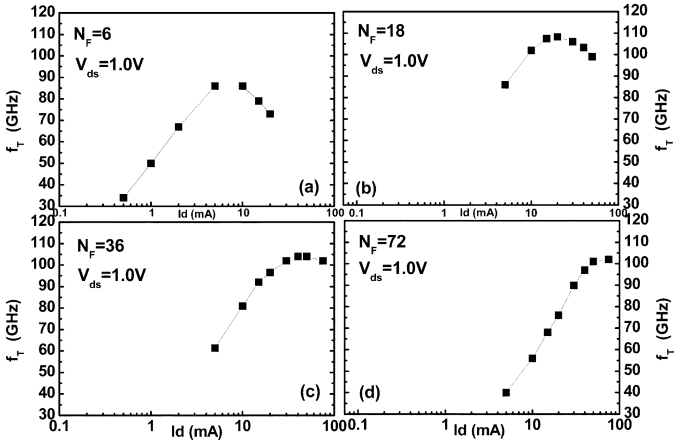


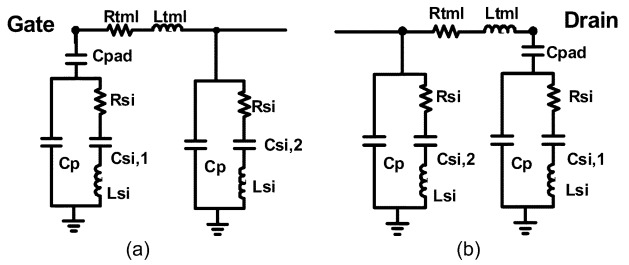
Fig. 5. Unit-current-gain cut off frequency f_T extracted from $|H_{21}| = 1$ for 80-nm n-MOSFETs (a) $N_F = 6$ (b) $N_F = 18$ (c) $N_F = 36$ (d) $N_F = 72$. Bias conditions at $V_{\rm ds} = 1.0$ and varying $V_{\rm gs}$ corresponding to drain currents from 0.5 to 100 mA.

their effect on RF noise. The details of *RLC* equivalent circuit development for modeling lossy substrate and lossy pad will be described in Section III. A full circuit model can be obtained by integrating the intrinsic MOSFET with the pad capacitance, the substrate and thru line related resistance (*R*), capacitance (*C*), and inductance (*L*), which represent the lossy pad and lossy substrate. Then, the extrinsic noise can be simulated by using the full circuit model. Through tuning of *RLC* parameters, the best fit to the measured *S*-parameters and noise parameters can be achieved and the full circuit can be finalized corresponding to optimized *RLC* parameters. The intrinsic MOSFET noise can be extracted by simulation through the lossy substrate and lossy pad de-embedding from the validated full circuit.

III. RESULTS AND DISCUSSION

A. 80-nm RF nMOSFETs—Measured Noise and Key Parameter Extraction

Fig. 2 shows the measured $\rm NF_{min}$ for 80-nm nMOSFETs with various finger numbers ($N_F = 6$, 18, 36, 72). It is demonstrated that RF noise without de-embedding decreases remarkably with increasing N_F. The lower gate resistance (R_g) associated with larger N_F may account for part of contribution but cannot explain the dramatic difference as larger as 4 dB between $N_F = 6$ and $N_F = 72$. In this paper, R_g were extracted from the *Z*-parameter at 40 GHz, which is sufficiently high to validate $R_g = \mathrm{Re}(Z_{11} - Z_{12})|_{\omega\to\infty}$ as derived from MOSFET small signal model illustrated by Fig. 3 and (1)–(6) in [9] and [10]. Fig. 4 indicates $\mathrm{Re}(Z_{11} - Z_{12})$ measured from the 80-nm n-MOSFETs. It reveals the frequency dependence described by (3) and a constant approached at 40 GHz, which represents R_g to be extracted. We got the result of lower R_g corresponding to larger N_F. However, varying N_F plays a tradeoff among R_g, g_m, and gate capacitances ($C_{\rm gs}, C_{\rm gd}$, and$C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$), i.e., the larger N_F will benefit from lower R_g and higher g_m but will suffer from larger gate capacitances. Table I lists all the key parameters such as R_g, g_m, $C_{\rm gs}$, and $C_{\rm gd}$, extracted from 80-nm n-MOSFETs with various N_F (6, 18, 36, 72). The resultant f_T calculated by $g_m/2\pi\left(C_{\rm gg}^2 - C_{\rm gd}^2\right)^{1/2}$ [11] are kept at similar level of higher than 100 GHz for larger devices with $N_F = 18$, 36, and 72. Regarding the smallest device with $N_F = 6$, f_T below 90 GHz is due to the nonscalable parasitic capacitances associated with the gate to interconnection lines, which cannot be de-embedded clean by conventional open de-embedding scheme. A new open de-embedding structure, which maintains all layers of metal originally existing in the DUT (device under test) may be a solution to get perfectly clean de-embedding and desired scalability in terms of device geometry like N_F. For this paper, the relatively smaller $g_m * R_g$ just compensates the lower f_T for the smallest device. According to Fukui's model [12], the minimum noise factor can be calculated by $F_{\rm min} = 1 + k * f/f_T[g_m(R_g + R_s)]^{1/2}$ as shown in Table I. The difference in $F_{\rm min}$ and $\rm NF_{min}$ between different N_F is not significant even assuming a constant k factor of 2 for all N_F. Fig. 5(a)–(d) indicates the actually measured f_T corresponding to $N_F = 6$, 18, 36, and 72, which are extracted from unit current gain ($|H_{21}| = 1$). It is noted that the gate bias, $V_{\rm gs}$ to achieve the maximum f_T just match with that responsible



Pad	L_{tml} (nH)	R_{tml} (Ω)	C_{pad}(pF)	C_P(pF)	$C_{Si,1}/C_{Si,2}$ (pF)	L_{Si} (nH)	R_{Si} (Ω)
Gate	0.03	0.25	0.19	0.0155	0.047/0.1265	0.5	408
Drain	0.02	0.25	0.19	0.0155	0.043/0.143	0.38	368

Fig. 6. RLC network circuits for open pads and lossy substrate coupled through the pad (a) gate pad as port-1 (b) drain pad as port-2.

for the maximum g_m, i.e., in the range of 0.7–0.75 V. The f_T extracted by $|H_{21}| = 1$ and those calculated by the analytical formula of $g_m/2\pi\left(C_{gg}^2 - C_{gd}^2\right)^{1/2}$ are put together in Table I for comparison. Good match obtained for all N_F justifies the accuracy of f_T as extracted and calculated. These sub-100-nm devices realize excellent RF performance in terms of f_T, which is comparable with the state-of-the-art standard logic based RF CMOS [1], [2]. However, the RF noise prior to de-embedding is abnormally high and particularly worse for the smallest devices with $N_F = 6$. To investigate the mechanisms responsible for the excess RF noise, an extensive analysis has been done on the RF device layout. We propose that the worse RF noise associated with MOSFET finger number scaling is due to the excessive lossy substrate and lossy pad effect. Transmission line may play some role in impedance matching. Our model suggests that the pad parasitics and lossy substrate must be de-embedded from the measured noise figure to achieve the accurate NF_{min} for intrinsic MOSFETs.

B. A New RLC Equivalent Circuit Model and Parameter Extraction Flow

Fig. 6(a) and (b) illustrates the equivalent circuits and the model parameters that we propose to simulate the lossy substrate effect through gate and drain pads respectively. The proposed *RLC* network incorporating pad capacitance $(C_{\rm pad})$, lossy substrate ($R_{\rm Si}$, $C_{\rm Si}$, $L_{\rm Si}$, and C_p), and transmission line ($R_{\rm tml}$, $L_{\rm tml}$) will be connected to the gate and drain terminals of the intrinsic MOSFET. The transmission line body is consisted of series resistor $(R_{\rm tml})$ and inductor $(L_{\rm tml})$. The shunt *RLC* path to ground at gate/drain pads is used to simulate the lossy pad and lossy substrate effect. The existence of both capacitive and inductive impedances, i.e., $C_{\rm Si}$ and $L_{\rm Si}$ in series with $R_{\rm Si}$ is quite different from the conventionally used simple shunt *RC* circuit. This new *RLC* network was created to accurately capture the unique frequency response associated with the lossy substrate. The *RLC* network has been extensively verified by comparison with measured results in terms of *S*-parameters, *Y*-parameters, and noise parameters before de-embedding. Fig. 7(a) presents the schematic block diagram derived by circuit analysis theory to extract the circuit elements ($R_{\rm Si}$, $C_{\rm Si}$, $L_{\rm Si}$, C_p, $R_{\rm TML}$, and $L_{\rm TML}$). Fig. 7(b) illustrates the model parameter extraction flow based on the circuit analysis. The pad capacitance, $C_{\rm pad} = 190$ fF is a physical parameter calculated

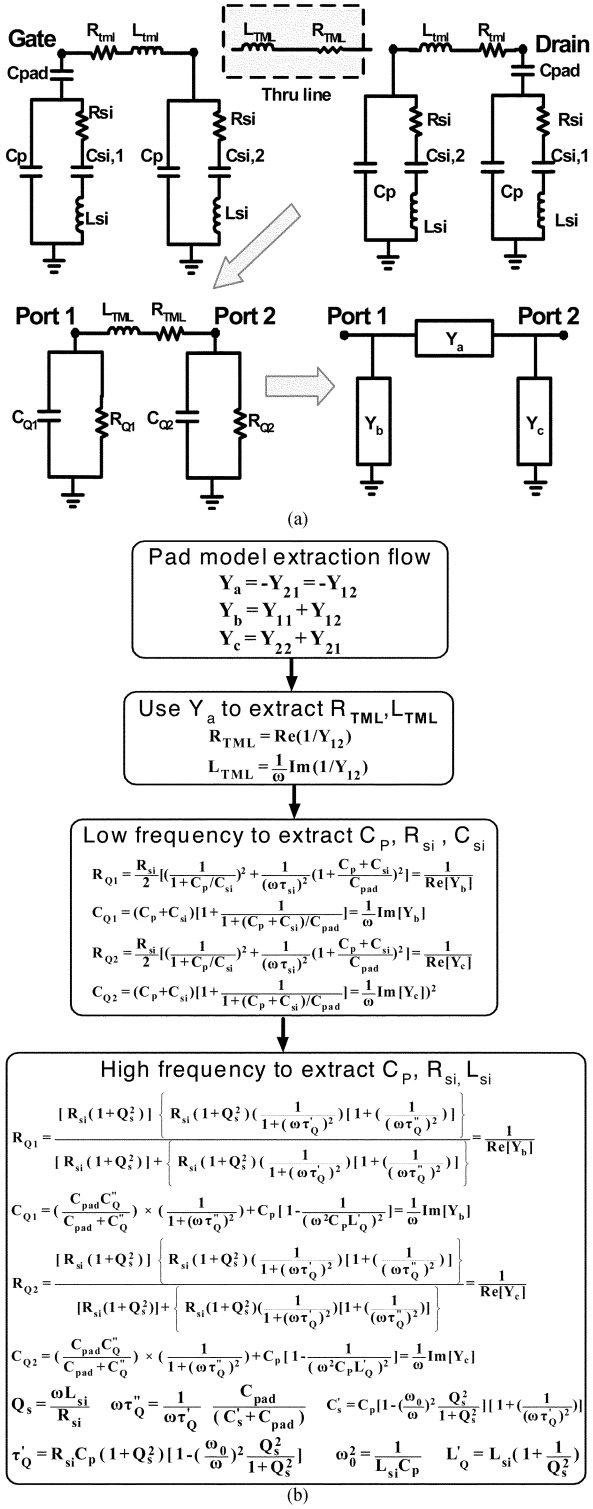


Fig. 7. (a) Schematic block diagram derived by circuit analysis theory to extract the circuit elements and (b) *RLC* circuit model parameter extraction flow.

by layout and process parameters rather than from extraction. It is noted that the first run of model parameters extracted based on approximation valid under relatively low/high frequencies (0.2/40 GHz in this paper) just serve as the initial guess for further optimization. The optimization was done by using ADS simulation to get best fit to *S*- and *Y*-parameters for both open

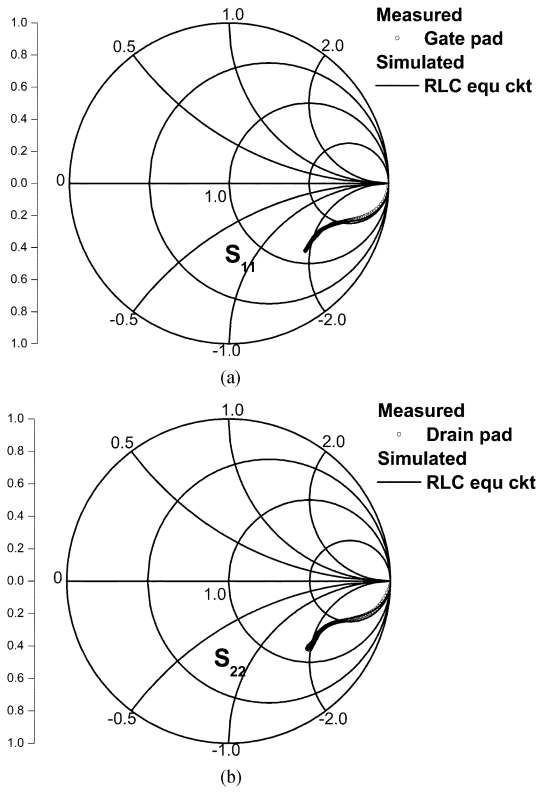


Fig. 8. Smith chart of measured S_{11} and S_{22} for open pad (symbol) and the good match by simulation (line) using the proposed *RLC* circuit (a) S_{11} for gate pad as port-1 (b) S_{22} for drain pad as port-1.

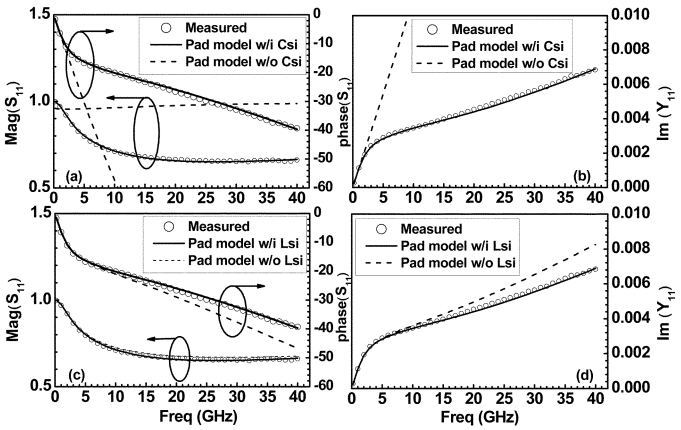


Fig. 9. Measured S_{11} and $\mathrm{Im}(Y_{11})$ for gate pad (symbol) and goof fit by simulation (line) using the proposed *RLC* circuit (a) S_{11} (magnitude and phase) and C_{Si} effect (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect (c) S_{11} (magnitude and phase) and L_{Si} effect (d) $\mathrm{Im}(Y_{11})$ and L_{Si} effect.

pad and full circuit (pad and intrinsic MOSFET together). Fig. 8(a) and (b) shows the good agreement in smith chart between simulation and measurement for open pads S_{11} (Gate pad as port-1) and S_{22} (Drain pad as port-2). Fig. 9(a)–(d) reveal the good fit to measured S_{11} (magnitude and phase) and $\mathrm{Im}(Y_{11})$ for gate pad in which the effect of C_{Si} and L_{Si} can be obviously identified. Fig. 10(a)–(d) indicates the good match with measured S_{22} (magnitude and phase) and $\mathrm{Im}(Y_{22})$ corresponding to drain pads where C_{Si} and L_{Si} effect is revisited and confirmed. The match simultaneously achieved for both *S*-parameters and *Y*-parameters manifests the fact that

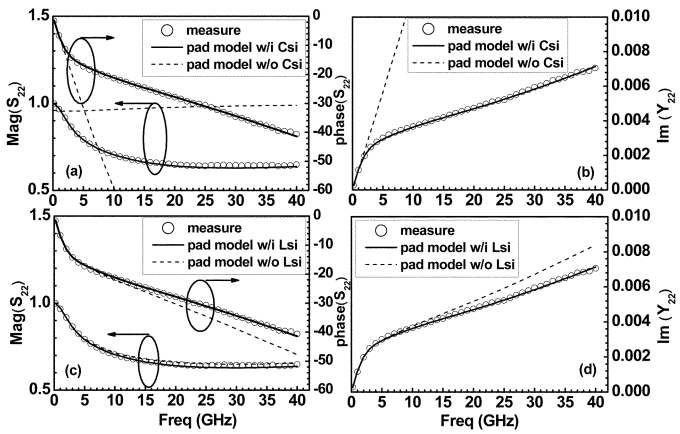
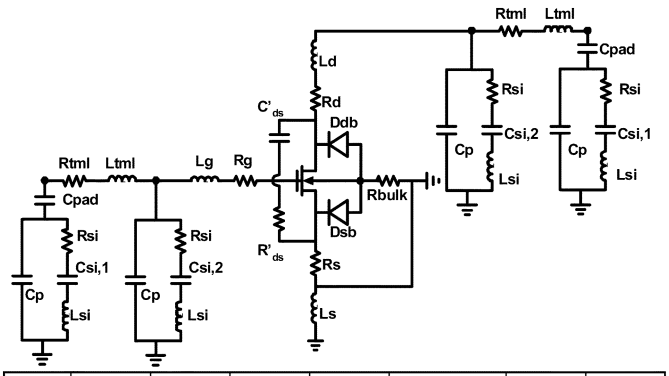


Fig. 10. Measured S_{22} and $\mathrm{Im}(Y_{22})$ for drain pad (symbol) and goof fit by simulation (line) using the proposed *RLC* circuit (a) S_{22} (magnitude and phase) and C_{Si} effect (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect (c) S_{22} (magnitude and phase) and L_{Si} effect (d) $\mathrm{Im}(Y_{22})$ and L_{Si} effect.



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N_F	R_g (Ω)	R_s(Ω)	R_d (Ω)	R_{bulk} (Ω)	L_g(pH)	L_d(pH)	L_s(pH)
6	26.56	1.23	1.26	166.43	33.8	18.6	15.7
18	11.05	0.83	0.42	87.04	31.4	16.4	16.1
36	6.27	0.73	0.21	67.19	32.7	17.5	15.5
72	3.98	0.67	0.10	57.26	30.3	15.1	16

Fig. 11. Full circuit model with intrinsic MOSFET integrated with *RLC* network in which R, L, C parasitics account for lossy pad (C_{pad}), lossy substrate (R_{Si}, L_{Si}, C_{Si}, and C_p), and transmission line (R_{tml}, L_{tml}) connected to the gate and drain of MOSFET.

the proposed *RLC* network is accurate to account for the lossy substrate effect. Our paper suggests that R_{Si}, C_{Si}, and L_{Si} are three key parameters playing the role to capture the lossy substrates feature over wide bandwidth. C_{Si} is the primary element responsible for the phase deviation in lower frequencies and nonlinear frequency response of $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{22})$. On the other hand, L_{Si} reveals increasing effect at higher frequencies. The nonlinear frequency response of $\mathrm{Im}(Y_{11})$ or $\mathrm{Im}(Y_{22})$ introduced by C_{Si} accounts for the nonconstant capacitance as extracted by $\mathrm{Im}(Y_{11})/\omega$ or $\mathrm{Im}(Y_{22})/\omega$. The obvious two-slope curvature results in larger effective capacitance in lower frequencies corresponding to larger slope, and apparently smaller effective capacitance at higher frequencies due to much reduced slope to near saturation.

C. Full Circuit Model for S-Parameter and Noise Simulation

Fig. 11 depicts the full circuit model for sub-100-nm MOSFETs in which the *RLC* networks representing lossy

pads, lossy substrate, and transmission line are linked with the intrinsic MOSFET. For accurate RF modeling, the body of intrinsic MOSFET is obviously different from the conventional one limited for DC modeling. The parasitic R and L associated with MOSFETs electrodes (G/S/D) were extracted by *Z*-parameter method [9], [10] shown in Fig. 2. The extracted R_g, R_s, R_d, L_g, L_s, and L_d for various N_F are tabulated and attached with Fig. 11. The full circuit for noise simulation contains the MOSFET body incorporating G/S/D electrodes' R and L as the intrinsic part (modeled by BSIM3) and the proposed *RLC* networks at two ports as extrinsic part. Besides the generally considered thermal noise, which is originated from drain current and gate resistance, pads' capacitive coupling and substrate loss are identified as more important factors responsible for the abnormally worse RF noise measured without effective de-embedding. The R_g associated with the intrinsic MOSFET represents the distributed gate and channel resistances. For devices with large finger number, e.g., $N_F = 72$, R_g is effectively reduced and $R_{\rm tml}$ may be not negligible in determining $\rm NF_{min}$. Regarding ultra high frequency, e.g., up to 40 GHz in this paper, inductive impedance L_g and $L_{\rm tml}$ become important parasitic elements, which can be evidenced by *S*-parameters to be shown as follows.

To certify the effectiveness and accuracy of the proposed *RLC* network for lossy pads and lossy substrate, *S*-parameter was calculated by using the full circuit schematics in Fig. 11 as the fundamental characteristics to be verified. Fig. 12(a) and (b) demonstrates good match in S_{11} and S_{22} (0.2–40 GHz) between the measurement and simulation for 80-nm n-MOSFETs with various N_F. It is revealed in the Smith chart that S_{11} and S_{22} are translated from capacitive to inductive mode under higher frequencies for the devices with large finger number ($N_F = 72$). It indicates the dominance of parasitic inductance existing in the transmission line connected to the gate electrode and pad (L_g and $L_{\rm tml}$). This result suggests the gate transmission line effect plays an increasingly important role in high frequencies. Fig. 13(a)–(d) shows the $\rm NF_{min}$ calculated by using the full circuit model for various N_F. Good agreement between the measured and modeled $\rm NF_{min}$ over wide range of frequencies up to 18 GHz justifies the accuracy of our lossy substrate model represented by the equivalent circuit in Fig. 11. Besides, the significant effect played by $C_{\rm Si}$ in terms of nonlinear frequency response is presented by comparison between the models with and without $C_{\rm Si}$. For rigorous validation of the model accuracy, four noise parameters R_n, $\rm Re(Y_{sopt})$, $\rm Im(Y_{sopt})$, and $\rm NF_{min}$ representing noise characteristics under best impedance matching for minimizing noise have been verified through extensive comparison with measurement. Good match between the measurement before de-embedding and lossy substrate modeling results will be shown in Section III-D with intrinsic characteristics after lossy substrate de-embedding put together for comparison.

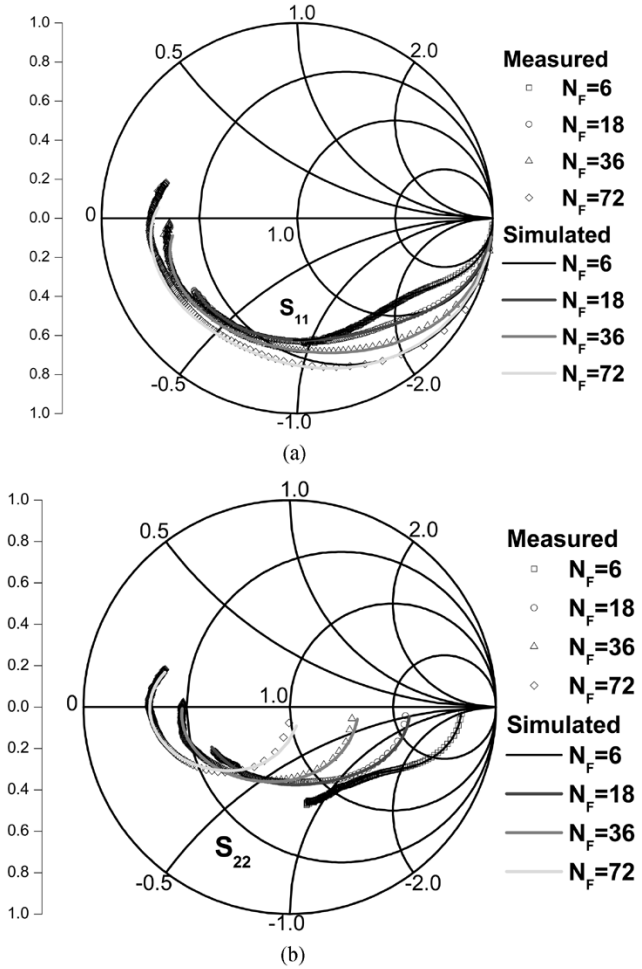

Fig. 12. Smith chart of measured S_{11} and S_{22} for full circuit with MOSFET and pads and the good match by simulation using the proposed *RLC* network (a) S_{11} (b) S_{22}. n-MOSFETs with $N_F = 6$, 18, 36, 72. and operating frequencies of 0.2–40 GHz. Symbol is the measured data and line is the simulation.

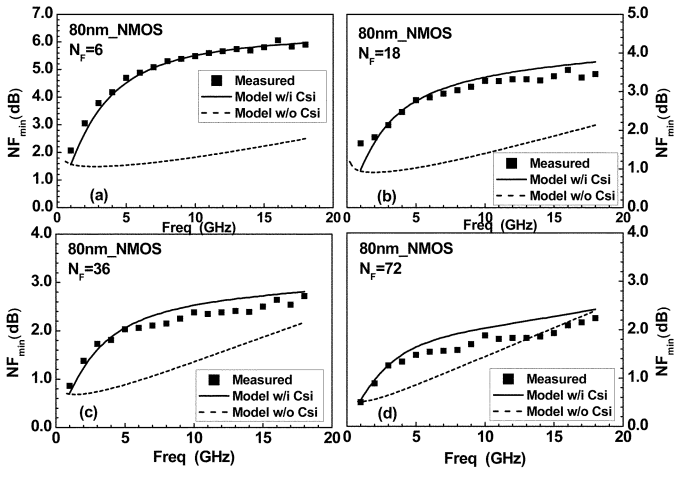

Fig. 13. Comparison of extrinsic $\rm NF_{min}$ between measurement (symbol) and simulation (line) for 80-nm n-MOSFETs (a) $N_F = 6$ (b) $N_F = 18$ (c) $N_F = 36$ (d) $N_F = 72$. $C_{\rm Si}$ effect is demonstrated for each device.

D. Lossy Substrate De-Embedding for Intrinsic Noise Extraction and Modeling

Based on the equivalent circuit model that has been well justified by *S*-parameters, *Y*-parameters, and $\rm NF_{min}$, we further analyzed the intrinsic MOSFETs by de-embedding the lossy pad, lossy substrate, and gate transmission line effect. The de-embedding procedure used in this paper is simply abstracting the pad *RLC* networks in Fig. 6, (pad capacitance ($C_{\rm pad}$), shunt *RLC* ($R_{\rm Si}$, $C_{\rm Si}$, $L_{\rm Si}$, and C_p) for lossy substrate,

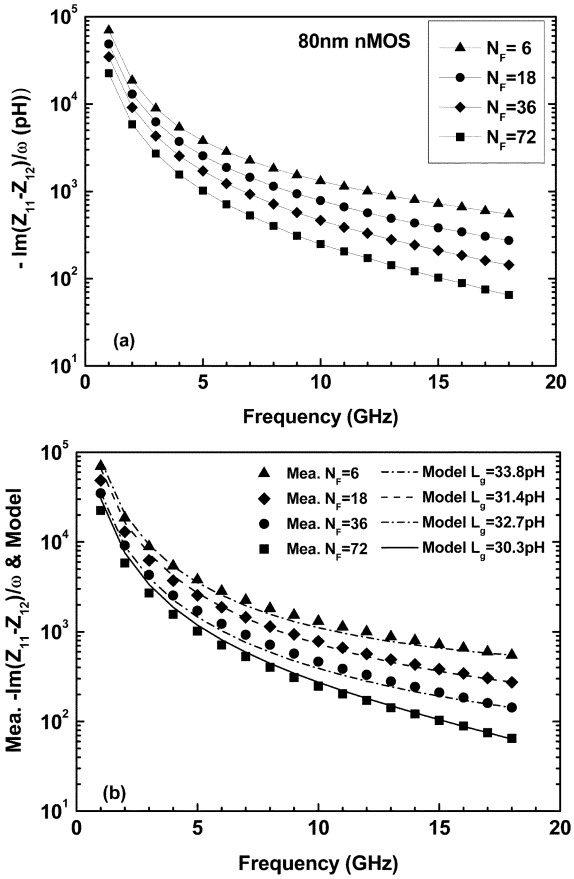

Fig. 14. Gate inductive impedance extracted from *Z*-parameters for 80-nm n-MOSFETs (a) different finger numbers, $N_F = 6$, 18, 36, 72 (b) good fit to $\mathrm{Im}(Z_{11} - Z_{12})/\omega$ by $L_{\mathrm{tml}} = L_g = 30$ pH as extracted.

and transmission line series resistance (R_{tml}) and inductance (L_{tml})) from the full circuit model in Fig. 11. The de-embedded *S*-parameters present pure capacitive nature of S_{11} (not shown), which manifests itself contribution from gate capacitances. The parasitic inductance originated from the transmission line also explains well the inductive behavior at higher frequencies before de-embedding. Fig. 14(a) illustrates the inductive mode impedance extracted from *Z*-parameters for the 80-nm devices with various N_F. The less negative values at higher frequencies account for the gradual dominance of inductive mode impedance. Basically, transmission line in series with the gate behaves like inductive mode impedance at higher frequencies and the inductive mode effect increases for larger N_F as shown in Fig. 14(b). It reflects the fact of larger gate capacitance associated with larger N_F and the subsequently smaller compensation to the inductive mode impedance at the input. The gate inductances (L_g) extracted from devices of various N_F present nearly a constant of around 30 pH. Fig. 14(b) indicates good fit to the imaginary part of *Z*-parameters, i.e., $\mathrm{Im}(Z_{11} - Z_{22})/\omega$ given by the model (6) [9], [10] using $L_g = 33.8$, 31.4, 32.7, and 30.3 pH extracted for $N_F = 6$, 18, 36, and 72 respectively. Adopting this new de-embedding method, we simulated the RF noise for 80-nm nMOSFETs with $N_F = 6$, 18, 36, 72. Fig. 15(a)–(d) and 16(a)–(d) indicate the extracted intrinsic $\mathrm{Re}(Y_{\mathrm{sopt}})$ and $\mathrm{Im}(Y_{\mathrm{sopt}})$ where good agreement between the simulation

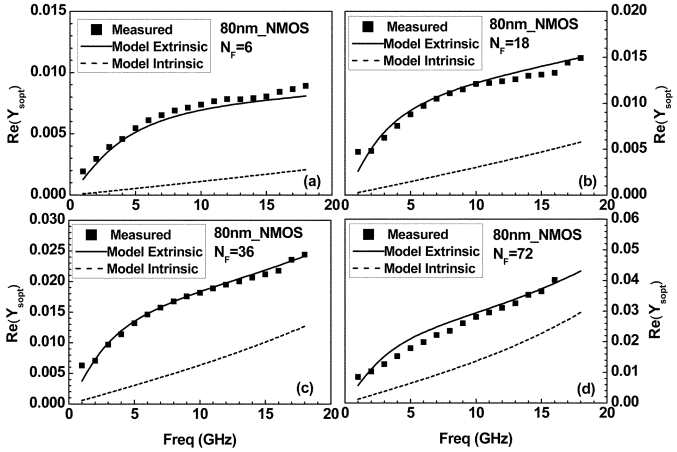

Fig. 15. Comparison of real part of Y_{sopt}, $\mathrm{Re}(Y_{\mathrm{sopt}})$ between measurement (symbol) and lossy substrate model (solid line), and the extracted intrinsic $\mathrm{Re}(Y_{\mathrm{sopt}})$ (dashed line) for 80-nm n-MOSFETs (a) $N_F = 6$, (b) $N_F = 18$, (c) $N_F = 36$, and (d) $N_F = 72$.

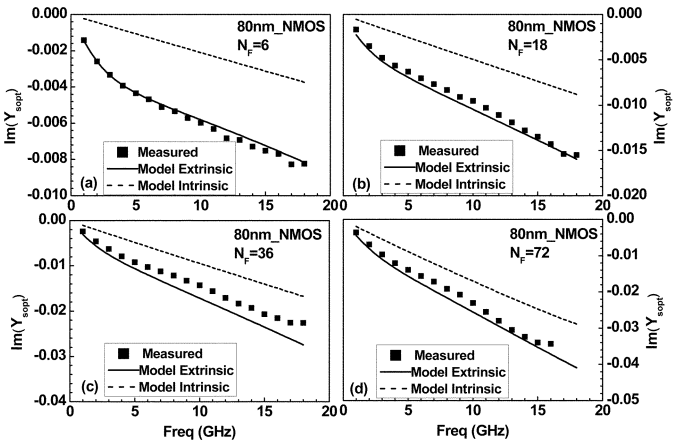

Fig. 16. Comparison of imaginary part of Y_{sopt}, $\mathrm{Im}(Y_{\mathrm{sopt}})$ between measurement (symbol) and lossy substrate model (solid line), and the extracted intrinsic $\mathrm{Im}(Y_{\mathrm{sopt}})$ (dashed line) for 80-nm n-MOSFETs (a) $N_F = 6$, (b) $N_F = 18$, (c) $N_F = 36$, and (d) $N_F = 72$.

and measurement for extrinsic $\mathrm{Re}(Y_{\mathrm{sopt}})$ as well as extrinsic $\mathrm{Im}(Y_{\mathrm{sopt}})$ are shown together to justify the accuracy of lossy substrate model. Both $\mathrm{Re}(Y_{\mathrm{sopt}})$ and $\mathrm{Im}(Y_{\mathrm{sopt}})$ reveal obvious reduction in magnitude for the intrinsic components subject to lossy substrate de-embedding. As for the noise resistance R_n shown in Fig. 17(a)–(d), intrinsic R_n show smaller values than extrinsic R_n but the difference tends to decrease for increasing N_F and become insignificant for large N_F. It is noted that both extrinsic and intrinsic R_n exhibit decreasing function with frequencies and good match with the measurement validates the lossy substrate model. Fig. 18(a)–(d) presents the extracted intrinsic $\mathrm{NF}_{\mathrm{min}}$ and comparison with extrinsic $\mathrm{NF}_{\mathrm{min}}$ before lossy substrate de-embedding. The extrinsic $\mathrm{NF}_{\mathrm{min}}$ calculated by lossy substrate model can reproduce the special feature of nonlinear frequency dependence and match the measurement. The intrinsic $\mathrm{NF}_{\mathrm{min}}$ extracted through lossy substrate de-embedding indicate good linearity w.r.t. frequency and remarkable reduction in noise level in comparison with extrinsic $\mathrm{NF}_{\mathrm{min}}$. It is noted that the intrinsic MOSFET model used to calculate intrinsic $\mathrm{NF}_{\mathrm{min}}$ incorporates R_g, R_s, R_d, and R_{bulk} at four

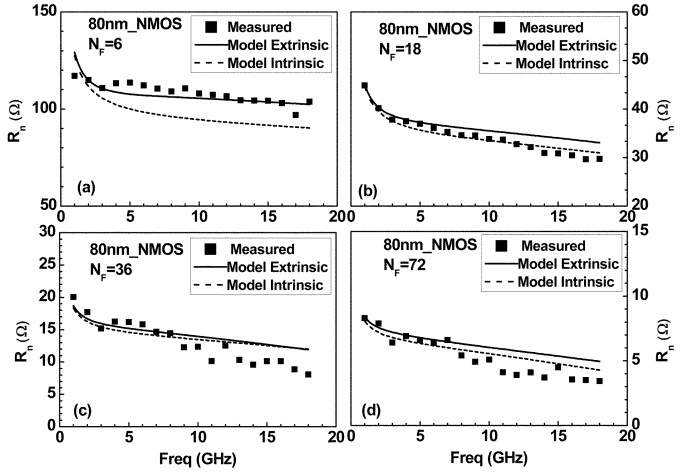

Fig. 17. Comparison of extrinsic noise resistance R_n between measurement (symbol) and lossy substrate model (solid line), and the extracted intrinsic R_n (dashed line) for 80-nm n-MOSFETs (a) $N_F = 6$, (b) $N_F = 18$, (c) $N_F = 36$, and (d) $N_F = 72$.

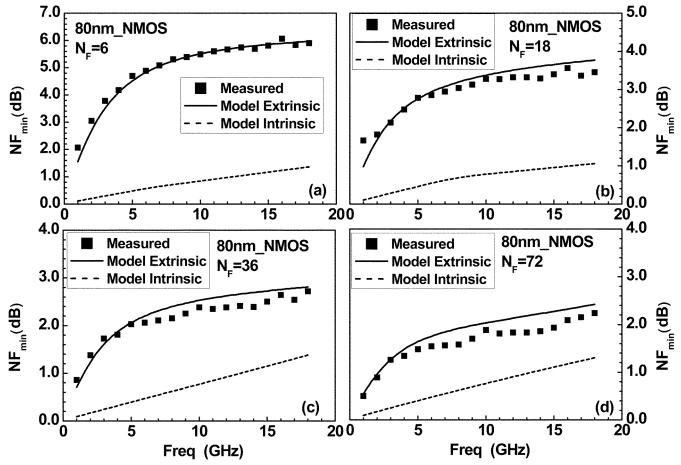

Fig. 18. Comparison of extrinsic noise figure $\mathrm{NF_{min}}$ between measurement (symbol) and lossy substrate model (solid line), and the extracted intrinsic $\mathrm{NF_{min}}$ (dashed line) for 80-nm nMOS (a) $N_F = 6$, (b) $N_F = 18$, (c) $N_F = 36$, and (d) $N_F = 72$.

terminals, which cannot be de-embedded. Due to the fact, drain current noise S_{id} and resistance induced gate noise S_{ig} are two major components contributing the intrinsic noise. In this paper through ADS simulation using modified BSIM3 model, the intrinsic induced gate noise was not included and the influence is considered negligible for sub-100-nm devices. Fukui's formula ($F_{\min} = 1 + k \times f/f_T[g_m(R_g + R_s)]^{1/2}$, $\mathrm{NF_{min}} = 10 \times \log F_{\min}$) [12], which holds valid under the mentioned condition [13] is adopted to verify the accuracy of the simulated intrinsic $\mathrm{NF_{min}}$. Because $\mathrm{NF_{min}}$ is critically dependent on the bias voltages and currents, two sets of bias conditions are specified in our simulation to certify the intrinsic noise model accuracy. Fig. 19(a) indicates the simulation done by fixed V_{ds} and V_{gs} for all N_F where V_{ds} is set as $V_{\mathrm{dd}} = 1.0$ V and V_{gs} is selected at 0.7 V corresponding to the maximum g_m. The simulated intrinsic $\mathrm{NF_{min}}$ follow linear relationship w.r.t. the frequency quite well and the intrinsic $\mathrm{NF_{min}}$ can be maintained below 0.9 dB for frequency up to 10 GHz. However, k factor tuning required for Fukui's model to fit $\mathrm{NF_{min}}$ for

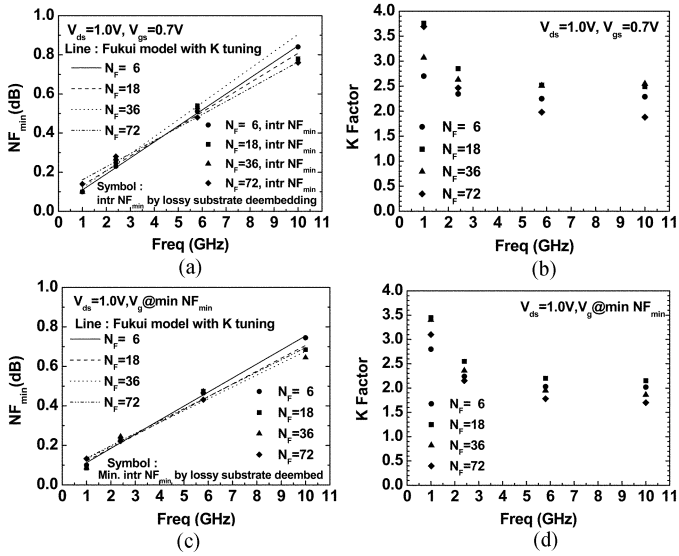

Fig. 19. Comparison of intrinsic $\mathrm{NF_{min}}$ extracted by lossy substrate de-embedding method (symbols) and calculated by Fukui's model (line) with k factor tuning (a) $\mathrm{NF_{min}}$ versus frequency for all N_F under $V_{\mathrm{ds}} = 1.0$ V and $V_{\mathrm{gs}} = 0.7$ V, (b) k factor versus frequency for all N_F under $V_{\mathrm{ds}} = 1.0$ V and $V_{\mathrm{gs}} = 0.7$ V, (c) $\mathrm{NF_{min}}$ versus frequency for $N_F = 6$, 18, 36, 72 under $V_{\mathrm{ds}} = 1.0$ V, $V_{\mathrm{gs}} = 0.45$, 0.53, 0.54, 0.5 V, respectively to achieve minimum $\mathrm{NF_{min}}$, and (d) k factor versus frequency for $N_F = 6$, 18, 36, 72 under $V_{\mathrm{ds}} = 1.0$ V, $V_{\mathrm{gs}} = 0.45$, 0.53, 0.54, 0.5 V.

all N_F revealed wide spread between different N_F as shown in Fig. 19(b). The k factor variation is worst at the lowest frequency, that is 2.7–3.76 at 1 GHz. We proposed from our paper that the fixed gate bias, $V_{\mathrm{gs}} = 0.7$ V was not the optimized bias point for all N_F to achieve the minimum $\mathrm{NF_{min}}$ and separated bias tuning for each N_F is needed. Fig. 19(c) shows the simulation done by the second set of bias conditions in which different V_{gs} were selected for different N_F to realize the minimum $\mathrm{NF_{min}}$. The gate biases, V_{gs} are located in the range of 0.45–0.55 V. We see that the intrinsic $\mathrm{NF_{min}}$ are reduced by around 0.1 dB at 10 GHz for all N_F and the difference from device sizes associated with N_F is much reduced to be less than 0.1 dB, i.e., $\mathrm{NF_{min}}$ below 0.8 dB at 10 GHz can be achieved even for the smallest device with $N_F = 6$. Furthermore, good match with Fukui's model can be obtained by k factor tuning confined to tighter range within 2.2 ± 0.3 for frequencies of 2.4, 5.8, and 10 GHz as shown in Fig. 19(d). The obvious frequency dependence revealed by k factor in lower frequency region of 1–2.4 GHz is considered to stem from the same origin responsible for the frequency dependence of noise resistance R_n, which has been reported by Goo in Dutton's group [14], [15]. The good match with Fukui's model in which the intrinsic induced gate noise was not considered suggests that the RF noise of 80-nm n-MOSFETs is dominated by the drain current noise rather than the intrinsic induced gate noise. Regarding the potential impact on the calculated noise parameters caused by neglecting the intrinsic induced gate noise, some existing literatures reported minor difference of around 5% on $\mathrm{NF_{min}}$ at 10 GHz and even not visible influence on noise resistance R_n based on their study on 0.18–μm devices [16]. It remains an interesting topic to be investigated for sub-100-nm devices.

Our study suggests that the lossy substrate lumped with lossy pad effect plays a major role contributing the extra RF noise. The

impact increases significantly with reducing the device size like finger number (N_F). As for the smallest device in this paper, i.e., $N_F = 6$, extra noise of around 4 dB at 10 GHz was introduced through the lossy pad and lossy substrate. The intrinsic $\mathrm{NF_{min}}$ extracted by our model can be pushed below 0.8 dB at 10 GHz, even for the smallest devices with $N_F = 6$ and largest R_g, which just meets the target set by most updated International Technology Roadmap Semiconductors (ITRS) for RF nMOS at 100-nm node [17] and suitable for wireless communication from handset to future *X*-band.

The advantage of our proposed method compared to the noise correlation matrix method [8] is the better accuracy in frequency dependence and immunity from fluctuation at extremely low noise levels.

IV. Conclusion

We have successfully extracted the intrinsic RF noise for multifinger RF MOSFETs by using a new and accurate lossy substrate de-embedding method. The extracted intrinsic $\mathrm{NF_{min}}$ reveals RF noise below 0.8 dB at 10 GHz for the 80-nm n-MOSFETs with various finger numbers under corresponding optimized bias condition. Our results just meets the speed and noise performance target set by most updated ITRS [17] and suggests the advantage of continuous gate length scaling beyond 80 nm in aspect of speed (higher f_T) and noise (lower $\mathrm{NF_{min}}$). The encouraging results from our paper consistently match the RF CMOS scaling trend published by Woerlee *et al.* [3]. This lossy substrate de-embedding method is useful for accurate intrinsic noise extraction and modeling that is critically important to improve RF circuit simulation accuracy for low noise RF circuit design.

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