A New Extraction Algorithm for the Metallurgical Channel Length of Conventional and LDD MOSFET's

Yuh-Sheng Jean, *Student Member, IEEE* and Ching-Yuan Wu, *Member, IEEE*

***Abstract*— A new extraction algorithm for the metallurgical channel length of conventional and LDD MOSFET's is presented, which is based on the well-known resistance method with performing a special technique to eliminate the uncertainty of the channel length as well as to reduce the influence of the parasitic source/drain resistance on threshold-voltage determination. In particular, the metallurgical channel length is determined from a wide range of gate-voltage-dependent effective channel length at an adequate gate overdrive. The 2-D numerical analysis clearly show that the adequate gate overdrive is strongly dependent on the dopant concentration in the source/drain region. Therefore, an analytic equation is derived to determine the adequate gate overdrive for various source/drain and channel doping. It shows that higher and lower gate overdrives are needed to accurately determine the metallurgical channel length of conventional and LDD MOSFET devices, respectively. It is the first time that we can give a correct gate overdrive to extract $L_{\rm met}$ not only for conventional devices but also for LDD MOS devices. Besides, the parasitic source/drain resistance can also be extracted using our new extraction algorithm.**

I. Introduction

THE channel length is one of the most important parameters for MOSFET's. In addition to performance analysis and fabrication process control, the channel length plays a major role on device design and circuit simulation. The so-called channel length has two different definitions in literatures. One is the effective channel length $(L_{\rm eff})$, which represents the 'effective' channel region that can be strongly modulated by the gate bias, while the metallurgical channel length $(L_{\rm met})$ is defined to be the distance between the metallurgical junctions of source and drain diffusions in the channel surface of a MOSFET, as illustrated in Fig. 1(a).

The extraction algorithms for effective channel length proposed in literatures were usually based on the resistance [1]–[8] and capacitance [9], [10] measurements. In addition to the problems of parasitic capacitance, equipment with high resolution is required to measure the small intrinsic gate capacitance down to the order of femto farads. Therefore, the capacitance method is impractical for applications. Comparing with the capacitance methods, the extraction algorithms based on the resistance methods are much simpler. Based on the resistance measurements, the methods [1], [2], [4] determined $L_{\rm eff}$ in a high gate overdrive range, which are applicable for conventional MOSFETs; while the method presented in [8] used a low gate overdrive range for LDD MOSFET's. There is no definite method to determine the magnitude of gate overdrive.

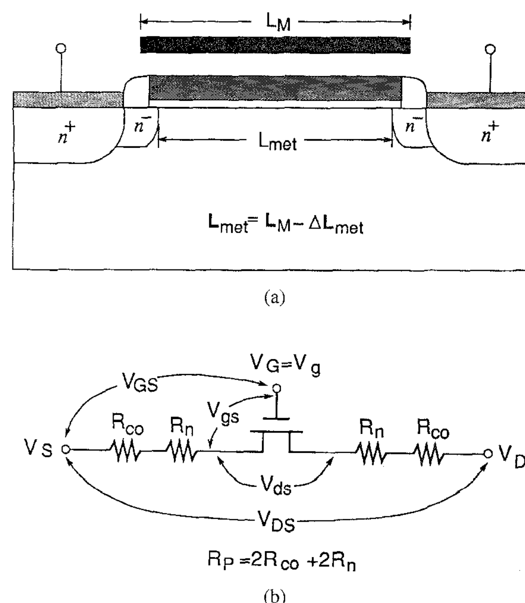


Fig. 1. (a) The cross ection view of a LDD nMOSFET showing the definitions and the relationship among L_M, $L_{\rm met}$ and $\Delta L_{\rm met}$, and (b) the equivalent circuit of a practical MOSFET device.

In this paper, an analytic equation is derived to predict the correct gate overdrive in order to determine the unique $L_{\rm met}$ from the extracted $L_{\rm eff}$ for both conventional and LDD MOSFET's. In Section II, a new extraction algorithm for the metallurgical channel length of MOSFET's is described. Our new extraction algorithm is based on the resistance measurement, from which we can determine the effective channel-length reduction $(\Delta L_{\rm eff})$. According to our analysis, the metallurgical channel-length reduction $(\Delta L_{\rm met})$ can be determined from a wide range of gate-bias dependent $\Delta L_{\rm eff}$. To improve the accuracy, the threshold-voltage correction is performed iteratively. In Section III, the 2-D numerical analysis shows that the major deviation in $\Delta L_{\rm met}$ extraction arises from the nonideal resistance distribution due to carrier redistribution. In addition, an analytic model is proposed to evaluate this phenomenon, and comparisons between 2-D numerical

Manuscript received August 11, 1995; revised December 7, 1996. The review of this paper was arranged by Editor K. Tada. This work was supported by the National Science Council, Taiwan, ROC, under Contracts NSC85-2215-E-009-041 and NSC84-2215-E009-019.

The authors are with the Advanced Semiconductor Device Research Laboratory and Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan, ROC.

Publisher Item Identifier S 0018-9383(96)04041-5.

0018–9383/96$05.00 © 1996 IEEE

analysis and analytic model evaluation are performed. The proposed extraction algorithm is verified by comparing the extraction results from 2-D simulation and experimental devices in Section IV. Finally, conclusions are given in Section V.

II. Descriptions of the Extraction Algorithm

For an ideal MOSFET device operated in the linear (low drain bias) region, the drain current can be expressed as

$$I_{\mathrm{ds}} = \frac{\mu C_{\mathrm{ox}} W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\left(V_{\mathrm{gs}} - V_T - \frac{V_{\mathrm{ds}}}{2}\right)V_{\mathrm{ds}} \quad (1)$$

where μ is the effective channel mobility, which is a function of applied gate bias; C_{ox} is the gate oxide capacitance per unit area; W_{eff} and L_{eff} are the effective channel width and length, respectively; V_{gs} and V_{ds} are the intrinsic gate to source and drain to source voltage drops, as shown in Fig. 1(b); and V_T is the threshold voltage. If the total parasitic source/drain resistance is R_P and the source and drain are symmetrical, then we have $V_{\mathrm{gs}} = V_{\mathrm{GS}} - I_{\mathrm{DS}}R_P/2$ and $V_{\mathrm{ds}} = V_{\mathrm{DS}} - I_{\mathrm{DS}}R_P$, where I_{DS} is equal to I_{ds}. Substituting V_{gs} and V_{ds} into (1), then the total resistance R_T is given by

$$R_T = R_P + R_{\mathrm{ch}} = R_P + \frac{L_M - \Delta L_{\mathrm{eff}}}{\mu C_{\mathrm{ox}} W_{\mathrm{eff}}\left(V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}\right)} \quad (2)$$

where R_{ch} is the channel resistance; L_M is the mask channel length; and ΔL_{eff} is the difference between mask channel length and effective channel length. If ΔL_{eff} is assumed to be the same for all test devices in a testkey and the threshold voltage of all test devices are known exactly, we can determine ΔL_{eff} from (2) by the following steps:

1) Taking the R_T value versus L_M at the same gate overdrive for all devices, the slope (S_{lope}) and the intercept in y-axis (Y_{cept}) can be obtained by a least squares fitting as follow

$$S_{\mathrm{lope}} = \left[\mu C_{\mathrm{ox}} W_{\mathrm{eff}}\left(V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}\right)\right]^{-1} \quad (3)$$

$$Y_{\mathrm{cept}} = R_P - S_{\mathrm{lope}} \times \Delta L_{\mathrm{eff}}. \quad (4)$$

2) Varying the gate overdrive, we can get the variations of Y_{cept} with respect to S_{lope}.

3) Differentiating Y_{cept} in (4) by S_{lope}, we have

$$\Delta L_{\mathrm{eff}} \equiv -\frac{dY_{\mathrm{cept}}}{dS_{\mathrm{lope}}}. \quad (5)$$

Note that each ΔL_{eff} at a given gate overdrive is deduced by its small gate overdrive interval, which is a constant within this small gate overdrive interval. Moreover, the extraction procedure described above needs to accurately determine the threshold voltages for all devices with different channel lengths Similarly, the effective channel mobility and the parasitic source/drain resistance are assumed to be constant within a small gate overdrive interval for all mask channel lengths. The extracted overall effective channel-length reduction (ΔL_{eff}) in (5) is gate-bias dependent [1], [2], [5], [6], and the determination of the metallurgical channel-length reduction from the gate-bias dependent effective channel-length reduction will be the major emphasis of this paper.

There are two basic guides to determine ΔL_{met} from the gate-bias dependent ΔL_{eff}: (a) For conventional MOSFET devices, ΔL_{eff} is chosen at higher gate overdrive [1]; (b) For LDD (lightly doped source/drain) MOSFET devices, ΔL_{eff} is chosen at lower gate overdrive [8]. The major reasons for using these two guides will be described in details in the next section. Once ΔL_{met} has been determined, the parasitic source/drain resistance (R_P) can be derived. R_P can be determined from (2) and is the value of R_T when L_M is equal to ΔL_{met}. Therefore, the definition of R_P is the total resistance outside the metallurgical junctions of source and drain diffusions. As mentioned above, for each gate overdrive there is a different R_P because R_P is gate-bias dependent. Nevertheless, the key step in channel-length extraction is to accurately determine the threshold voltage of each device so that R_T can be evaluated at the same gate overdrive [7], [8]. With the improperly deduced threshold voltage, the extracted ΔL_{eff} will be far away from its exact value. Consequently, the threshold voltage must be determined accurately and carefully.

In our extraction method, the normalized current method is used to determine the threshold voltage. First, the longest channel-length device is chosen to ensure negligible short-channel and parasitic source/drain resistance effects; and its threshold voltage is determined by the conventional maximum transconductance extrapolation method. The current at the extracted threshold voltage divided by the channel length is defined as the 'normalized current'. Next, this 'normalized current' multiplied by other shorter channel length is used to determine the threshold voltage of shorter device. However, the channel length of shorter device before determining its threshold voltage is unknown except that the mask channel length is known. Therefore, initially the mask length is used instead of the channel length. This is a good approximation in the case of $L_M \gg \Delta L_{\mathrm{met}}$ and will produce serious errors for small L_M. In addition, it is known that the parasitic source/drain resistance R_P may greatly reduce the drain current of short channel devices. To reduce the influence of ΔL_{met} and R_P on the threshold-voltage determination, the 'iteration' method proposed in [8] is used. After extracting ΔL_{met} and R_P, from (2) we have

$$I'_{\mathrm{DS}} = \frac{V_{\mathrm{DS}}}{R_T - R_P} = \frac{\mu C_{\mathrm{ox}} W_{\mathrm{eff}}\left(V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}\right)V_{\mathrm{DS}}}{L_{\mathrm{met}}} \quad (6)$$

where I'_{DS} is the intrinsic drain current, which does not include the R_P effect. Therefore, we can determine V_T from the extracted ΔL_{met} and (6), and further to extract ΔL_{met}. This process is repeated until the extracted V_T and ΔL_{met} self-consistently converge to their true values, as expressed by a flowchart shown in Fig. 2.

III. Numerical Analysis and Analytic Model Evaluation

A. Numerical Analysis

In the previous section, we have assumed that the MOS devices exhibit the ideal characteristics. The ideal resistance distribution is shown in Fig. 3 by the dashed line, in which

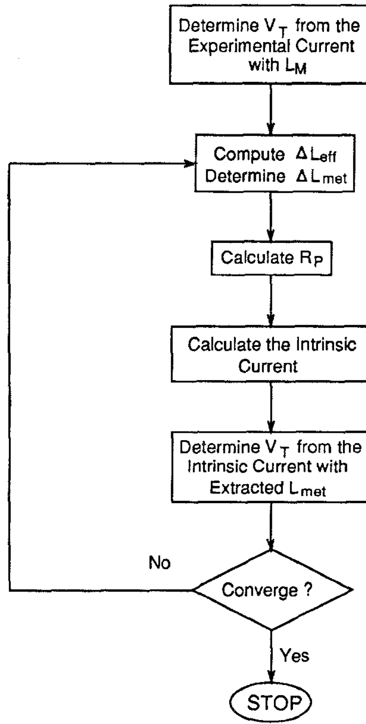


Fig. 2. The flowchart showing the extraction algorithm.

the x-axis is the distance along the channel $x(\mu\text{m})$, and the y-axis is the channel resistance per unit length $dR/dx(\Omega/\mu\text{m})$ computed by evaluating the change of the electron quasi-Fermi-level over a small interval divided by the distance and source-drain current [5]. Note that the area under the curve shown in Fig. 3 represents the resistance of a MOSFET. For an ideal device, the parasitic source/drain resistance (the resistance outside the L_{met} region) is a fixed value and is independent of gate overdrive, whereas the channel resistance (the resistance in the L_{met} region) is proportional to the metallurgical channel length L_{met} and is bias-dependent. The maximum dR/dx (signed $S_{\max}$) must be the same for all channel lengths at a given gate overdrive. This means that the deduced threshold voltage is accurate, i.e., all devices are operated at the same gate overdrive. From the ideal devices shown in Fig. 3, the total resistance can be expressed as

$$R_T = R_P + S_{\max} \times (L_M - \Delta L_{\text{met}}) \tag{7}$$

where $R_P = 2R_{\text{co}} + 2R_n$; R_{co} is the contact resistance, which is not shown in Fig. 3; R_n is the resistance between source/drain contact and channel region, as shown in Fig. 3. In general, R_{co} is constant, while R_n is bias-dependent. Nevertheless, R_{co} and R_n are all constants for the ideal characteristics. Now, S_{lope} and Y_{cept} in (5) can be obtained from (7): $S_{\text{lope}} = S_{\max}$ and $Y_{\text{cept}} = R_P - S_{\max} \times \Delta L_{\text{met}}$. According to (5), the channel-length reduction can be obtained by

$$\Delta L_e = -\frac{d}{dS_{\max}}(R_P - S_{\max} \times \Delta L_{\text{met}}) \tag{8}$$

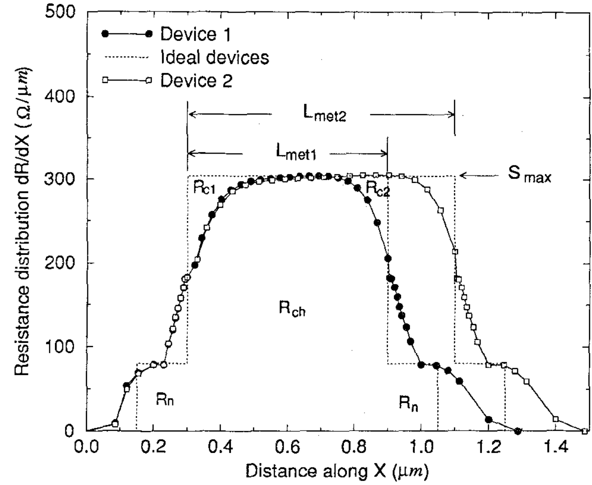


Fig. 3. The resistance distributions of ideal and practical LDD MOSFET devices with $L_{\text{met}} = 0.6$ and $0.8\ \mu\text{m}$.

where ΔL_e is the extracted channel-length reduction. Note that the subscript in ΔL_e is used to distinguish the exact (given) ΔL_{met} value. If R_P is independent of bias condition (assumption for ideal MOSFET's), ΔL_e will be exactly equal to ΔL_{met}.

However, for a practical MOSFET, the total resistance cannot be simply expressed by (7), and the reasons are shown in Fig. 3. It's clearly seen that the real dR/dx is not the same as that of an ideal device, so the channel resistance R_{ch} is less than $S_{\max} \times (L_M - \Delta L_{\text{met}})$ and can be represented by

$$R_{\text{ch}} = S_{\max} \times (L_M - \Delta L_{\text{met}}) - R_{c1} - R_{c2} \tag{9}$$

where R_{c1} and R_{c2} are the areas indicated in Fig. 3 and are bias-dependent, which represent the difference of channel resistance between ideal and practical MOSFET's. On the other hand, the R_n in the parasitic resistance R_P is also dependent on gate overdrive for a practical device. Now, the total resistance of a practical MOSFET in (7) can be rewritten as

$$R_T = 2R_{\text{co}} + A + S_{\max} \times (L_M - \Delta L_{\text{met}}) \tag{10}$$

where $A = 2R_n - R_{c1} - R_{c2}$. From (10), Y_{cept} becomes

$$Y_{\text{cept}} = 2R_{\text{co}} + A - S_{\max} \times \Delta L_{\text{met}}. \tag{11}$$

Applying (5), the extracted channel-length reduction becomes

$$\Delta L_e = \Delta L_{\text{met}} - \frac{dA}{dS_{\max}}. \tag{12}$$

In practice, (12) is the effective channel-length reduction ΔL_{eff} as mentioned in the previous section. This equation described the relation between the extracted ΔL_{eff} and the real ΔL_{met}. If $dA/dS_{\max}$ in (12) is equal to zero, the extracted ΔL_{eff} will be equal to ΔL_{met}. It is worth noting that ΔL_{met} in (11) and (12) is a constant, while ΔL_e and $dA/dS_{\max}$ are bias-dependent. The resistances R_n, R_{c1} and R_{c2} are all bias-dependent. Anyway, R_n, R_{c1} and R_{c2} cannot be extracted from the extraction algorithm as described in Section II. Therefore, we compute these resistances from

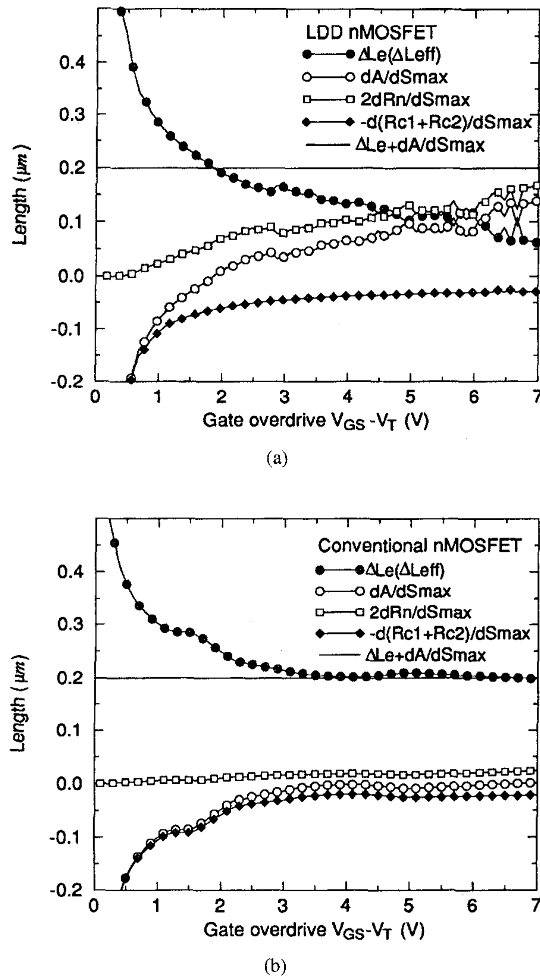


Fig. 4. The simulation results using 2-D numerical analysis for (a) LDD device, and (b) conventional device.

a 2-D device simulator-SUMMOS [11], as demonstrated in Fig. 4(a). In this figure, $\Delta L_{\rm eff}$, $dA/dS_{\max}$, $2dR_n/dS_{\max}$ and $-(dR_{c1}+dR_{c2})/dS_{\max}$ are computed as a function of $V_{\rm GS}-V_T$ and the given $\Delta L_{\rm met}$ is 0.2 μm. Note that $\Delta L_{\rm eff}$ in Fig. 4 is calculated by (5), where $S_{\rm lope}(S_{\max})$ is obtained from Fig. 3, $Y_{\rm cept}$ is calculated by $R_T - S_{\max}L_M$. As mentioned above, $\Delta L_{\rm eff}$ is bias-dependent and its value decreases from 0.5 μm to 0.1 μm when $V_{\rm GS}-V_T$ increases from 0 to 5 V. Similarly, $dA/dS_{\max}$ increases from negative to 0.1 μm. If we add $\Delta L_{\rm eff}$ and $dA/dS_{\max}$ together, the sum is nearly a constant, i.e., 0.2 μm, just the given value for $\Delta L_{\rm met}$. In other words, when $dA/dS_{\max}$ is equal to zero, $\Delta L_{\rm eff}$ is exactly equal to $\Delta L_{\rm met}$, and this situation happens at a gate bias of $V_{\rm GS}-V_T = 1.8$ V, as shown in Fig. 4(a). This means that the decrease rate of $R_{c1}+R_{c2}$ is just compensated by the decrease rate of $2R_n$.

Note that Figs. 3 and 4(a) are for LDD MOSFET's. For a conventional device, as shown in Fig. 5, it is clearly shown that R_n is nearly equal to zero because of the heavily doped source/drain region, so its gate modulation $2dR_n/dS_{\max}$ in Fig. 4(b) approaches to zero. On the other hand, R_{c1} and R_{c2}

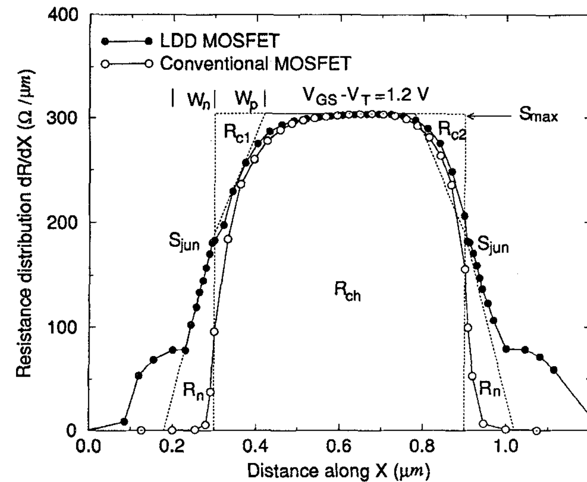


Fig. 5. Comparisons of the resistance distribution between a LDD and a conventional MOSFET with $L_{\rm met} = 0.6$ μm for gate overdrive of 1.2 V. The resistances for a practical MOSFET device approximated by the simple geometrical shapes are also illustrated.

are similar for conventional and LDD MOSFET's. Hence, the curve of $-(dR_{c1}+dR_{c2})/dS_{\max}$ in Fig. 4(b) is similar to that in Fig. 4(a). Again, the sum of $dA/dS_{\max}$ and $\Delta L_{\rm eff}$ is a constant. Apparent differences shown in this figure are $\Delta L_{\rm eff}$ and $dA/dS_{\max}$; unlike the LDD MOSFET's, $\Delta L_{\rm eff}$ and $dA/dS_{\max}$ approach to 0.2 and 0 μm at higher gate overdrive, respectively.

From the 2-D numerical analysis for LDD and conventional MOSFET's mentioned above, the principle to choose $\Delta L_{\rm met}$ from $\Delta L_{\rm eff}$ as described in the previous section has been given.

B. Analytic Model Evaluation

The resistance distribution of a typical MOSFET can be divided into 7 components, as shown in Fig. 6. They are:

1) Gate-controlled channel resistance,
2) Carrier diffusion related channel resistance,
3) Carrier diffusion related source/drain resistance,
4) Gate overlapped source/drain resistance,
5) Gate fringe field induced resistance,
6) Source/drain sheet resistance,
7) Contact resistance (not shown in Fig. 6).

The gate-controlled channel resistance locates at the center of the channel and is strongly modulated by the gate voltage. Components 2 and 3 come from carrier redistribution between source/drain region and channel region. Higher carrier concentration in source/drain region will diffuse to channel region where the carrier concentration is lower. This carrier redistribution decreases the channel resistance and increases the source/drain region resistance. Therefore, Component 2 is smaller than Component 1, while Component 3 is larger than Component 4, as shown in Fig. 6. Components 4 and 5 are also modulated by gate bias, which are weak and very weak functions of gate bias, respectively. Component 6 is related to source/drain doping concentration and Component 7 is constant.

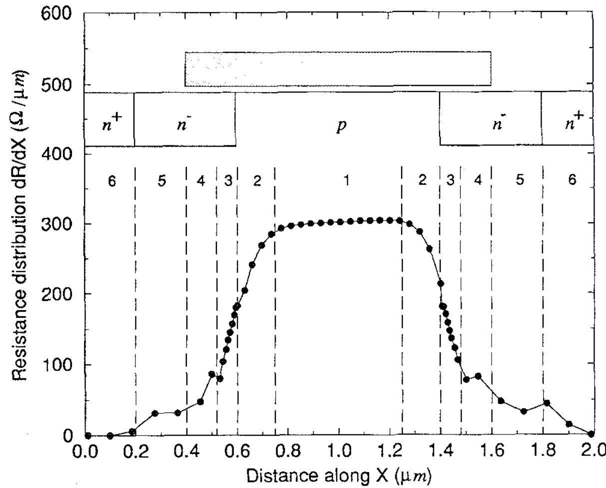


Fig. 6. Illustration of the practical MOSFET device divided into 7 regions according to the resistance distribution.

Note that $dA/dS_{\max}$ is an indicator of how ΔL_{eff} approaching to ΔL_{met}. As the value $dA/dS_{\max}$ approaches to zero, ΔL_{eff} approaches to ΔL_{met}. Here, $S_{\max}$ is a strong function of gate bias (Component 1), and A is related to Components 2, 3, 4, 5 and 6. However, Component 6 is independent of gate bias and Component 5 is a very weak function of gate bias, so we can neglect them. Component 4 is basically a weak function of gate bias. For modern MOSFET devices, ΔL_{met} is small and, therefore, the overlapped region is further smaller than it. Again, Component 4 is abandoned. Now, we only consider Components 1, 2 and 3 to compute $dA/dS_{\max}$.

For a small drain to source voltage (e.g., $V_{\text{DS}} = 0.05$ V), the shape of Fig. 5 is nearly symmetrical, i.e., $R_{c1} \simeq R_{c2}$. Therefore, $dA/dS_{\max}$ becomes

$$\frac{dA}{dS_{\max}} = \frac{d}{dS_{\max}}(2R_n - R_{c1} - R_{c2}) = \frac{d}{dS_{\max}}(2R_n - 2R_{c1}). \tag{13}$$

where R_n and R_{c1} can be approximated by the triangle areas shown in Fig. 5 and are given by $R_{c1} = W_p(S_{\max} - S_{\text{jun}})/2$ and $R_n = W_n S_{\text{jun}}/2$, in which W_p and W_n are the widths of carrier redistribution in the channel and source/drain regions, respectively; S_{jun} is the value of dR/dx at the metallurgical junction. Now, (13) becomes

$$\frac{dA}{dS_{\max}} = \frac{d}{dS_{\max}}[(W_p + W_n)S_{\text{jun}} - W_p S_{\max}]. \tag{14}$$

The exact values for W_p and W_n can be obtained by solving the current density and Poisson's equations. To simplify the problem, we consider that W_p and W_n are proportional to Debye length in this paper. Since the majority-carrier concentration deviated from the dopant concentration is governed by the extrinsic Debye length L_D [12], which is expressed by $L_D = [\frac{\epsilon_s kT}{q^2(n+p)}]^{\frac{1}{2}}$. Therefore, W_p and W_n can be expressed as

$$W_p = k_1 L_{Dp} \simeq k_2[C_{\text{ox}}(V_{\text{GS}} - V_T)/Y]^{-\frac{1}{2}}, \tag{15}$$

$$W_n = k_1 L_{Dn} \simeq k_2[qN_D + C_{\text{ox}}(V_{\text{GS}} - V_{\text{FB}n})/Y]^{-\frac{1}{2}} \tag{16}$$

where k_1 and k_2 are the constants; L_{Dp} and L_{Dp} are the extrinsic Debye length in the channel and source/drain region, respectively; C_{ox} is the oxide capacitance per unit area; Y is the effective thickness of inversion and accumulation carriers; N_D is the dopant concentration in the source/drain region; $V_{\text{FB}n}$ is the flat-band voltage in the source/drain region. The $S_{\max}$ can be approximated by (referred to (3))

$$S_{\max} \simeq k_3(V_{\text{GS}} - V_T)^{-1} \tag{17}$$

where k_3 is a constant, and we can evaluate S_{jun} from (17) simply by considering the channel resistance reduced by the built-in potential of the source/drain junction

$$S_{\text{jun}} \simeq k_3(V_{\text{GS}} - V_T + V_{\text{bip}})^{-1} \tag{18}$$

where V_{bip} is the built-in potential in the channel side. Substituting (15)–(18) into (14) and letting $dA/dS_{\max} = 0$, after some manipulations we have

$$\begin{aligned}(V_{\text{GS}} - V_T)^{-\frac{5}{2}} &= \frac{1}{3}\left[(V_{\text{GS}} - V_T)^{-\frac{3}{2}} + \left(\frac{qN_D Y}{C_{\text{ox}}} + V_{\text{GS}} - V_{\text{FB}n}\right)^{-\frac{3}{2}}\right] \\ &\quad \times (V_{\text{GS}} - V_T + V_{\text{bip}})^{-1} \\ &\quad + \frac{2}{3}\left[(V_{\text{GS}} - V_T)^{-\frac{1}{2}} + \left(\frac{qN_D Y}{C_{\text{ox}}} + V_{\text{GS}} - V_{\text{FB}n}\right)^{-\frac{1}{2}}\right] \\ &\quad \times (V_{\text{GS}} - V_T + V_{\text{bip}})^{-2}.\end{aligned} \tag{19}$$

Substituting Y [13], V_T, $V_{\text{FB}n}$ and V_{bip} into (19), we can solve V_{GS} by the iteration method. The results of the relationship among $V_{\text{GS}} - V_T$, N_D and N_A (dopant concentration in the channel region) are shown in Fig. 7. The adequate gate overdrive to determine ΔL_{met} for a fixed surface channel doping increases with the source/drain doping, because a larger gate overdrive is needed to accumulate the carrier density comparable to source/drain dopant concentration for heavily doped source/drain region, as shown in Fig. 4, where the higher source/drain doping results in weaker modulation for gate overdrive on the source/drain region. On the other hand, the gate modulation in the channel region becomes difficult as the gate overdrive increases due to strong inversion. So, a larger gate overdrive for heavily doped source/drain is needed to have $dA/dS_{\max}$ approaching to zero for extracting ΔL_{met}. This also can be observed from (13), in which $R_{c1} + R_{c2}$ can be approximated by $W_p(S_{\max} - S_{\text{jun}})$, as shown in Fig. 5, where W_p in (15) and $S_{\max}$ in (17) are independent of source/drain doping. Although S_{jun} in (18) depends on source/drain doping through V_{bip}—built-in potential in the channel side, it is a weak function of source/drain doping because source/drain doping is much higher than channel doping. Therefore, the gate modulation for $R_{c1} + R_{c2}$ is nearly the same for varied source/drain doping. However, $2R_n \simeq W_n S_{\text{jun}}$ strongly depends on source/drain doping through W_n in (16), and this indicates that the gate modulation becomes weak when source/drain doping increases. In this situation, a weak gate modulation for $R_{c1} + R_{c2}$ is needed to compensate it to let $dA/dS_{\max} = 0$, which requires a higher gate overdrive.

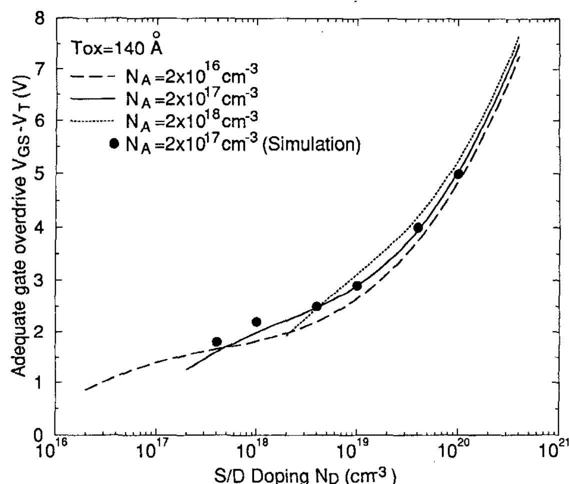


Fig. 7. The adequate gate overdrive for extracting the $L_{\rm met}$ versus source/drain doping calculated by analytic evaluation and 2-D numerical simulation for various channel dopings.

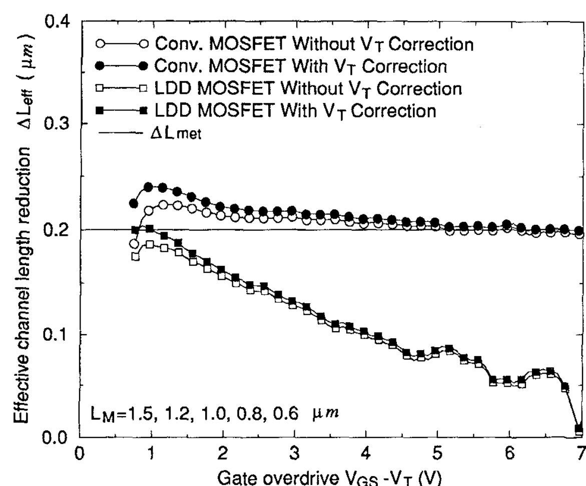


Fig. 8. The relations of the extracted $\Delta L_{\rm eff}$ versus the gate overdrive for conventional and LDD MOSFET's. The extraction results before and after V_T correction are shown.

On the other hand, the lower source/drain doping requires a lower gate overdrive to determine $L_{\rm met}$.

For the channel concentration varies as large as two orders in magnitude, however, the adequate gate overdrive to determine $\Delta L_{\rm met}$ does not show a large variation. This is convenient for our extraction algorithm, and we can determine $\Delta L_{\rm met}$ without taking care of the channel doping. Moreover, the n^- region doping for LDD devices is around 10^{18} cm^{-3}, and the adequate gate overdrive is about 1.5 V. For conventional devices, the gate overdrive must be large enough to about 5 V. Therefore, the principles for determining $\Delta L_{\rm met}$ from $\Delta L_{\rm eff}$ are verified again. Simulation results from Fig. 4 and other cases are also marked in Fig. 7, the results agree well with those using the analytic model evaluation. Therefore, the deduced range of gate overdrive is a useful reference for our extraction algorithm.

In general, the parasitic source/drain resistance extracted from the algorithm described in the previous section will be smaller than the exact value (if $\Delta L_{\rm met}$ is correct). This can be observed from (10), if we let $L_M = \Delta L_{\rm met}$, R_T will be equal to $2R_{\rm co}+2R_n-R_{c1}-R_{c2}$ and this value is smaller than $R_P = 2R_{\rm co}+2R_n$ by $R_{c1}+R_{c2}$. So, we can predict that the extracted R_P will deviate from its exact value, especially when the the gate overdrive is small and the deviation is extremely large (Fig. 9). However, the extracted R_P is very accurate at high gate overdrive.

IV. Extraction Results

The parameters given in our simulation are listed in Table I for conventional and LDD MOSFET's, and the definitions for the parameters are given in [11]. The mask channel lengths used are L_M = 1.5, 1.2, 1.0, 0.8, 0.6 μm. The extraction results for conventional and LDD MOSFET's with and without V_T correction are all shown in Fig. 8. The $\Delta L_{\rm eff}$ for conventional devices approaches to $\Delta L_{\rm met}$ at around $V_{\rm GS} - V_T$ = 5 V, this agrees with the conclusions in the previous analysis (Fig. 7). The V_T correction is not important because R_P of conventional device is small. For LDD devices without V_T correction, $\Delta L_{\rm eff}$ is always smaller than $\Delta L_{\rm met}$. After V_T correction, $\Delta L_{\rm eff}$ is equal to $\Delta L_{\rm met}$ at a gate overdrive of about 1 V. The gate overdrive does not precisely agree with the analysis (Fig. 7) due to the assumptions of constant R_P and μ, and the error is introduced in the extraction process. For convenience without losing the precision of $\Delta L_{\rm met}$ extraction, the maximum of $\Delta L_{\rm eff}$ is chosen to be $\Delta L_{\rm met}$ for LDD devices. On the contrary, we regard $\Delta L_{\rm eff}$ at high gate overdrive (e.g., 5 V) as $\Delta L_{\rm met}$ for conventional devices. However, it is not adequate to choose a very high gate overdrive because $S_{\rm max}$ (averaged channel resistance) decreases very slowly at high gate overdrive, therefore $dA/dS_{\rm max}$ is prone to induce enormous error by noise. On the other hand, as shown in Fig. 4(b), $-d(R_{c1}+R_{c2})/dS_{\rm max}$ approaches to zero at high gate overdrive, but $2dR_n/dS_{\rm max}$ increases slowly. If a very high gate overdrive is chosen, $\Delta L_{\rm met}$ will be underestimated. This means that at the very high gate overdrive a part of source/drain region becomes channel region, therefore reducing $\Delta L_{\rm eff}$. In practice, we take the average of $\Delta L_{\rm eff}$ in the range of 4 ~ 5 V in order to reduce the noise and the possible error.

TABLE I
THE STRUCTURE PARAMETERS OF CONVENTIONAL AND LDD DEVICES SIMULATED BY SUMMOS

Parameter	value	Parameter	value
T_{ox}(Å)	140	$N^+_{max}(10^{20}cm^{-3})$	3.41
$V_{FB}(V)$	-0.868	$R^+_{pd}(10^{-4}cm)$	0.238
$N_B(10^{15}cm^{-3})$	3.094	$R^+_j(10^{-4}cm)$	0.263
$\Phi_1(10^{12}cm^{-2})$	2.474	f	0.66
$\Delta R_{p1}(10^{-6}cm)$	5.220	$R_{co}(\Omega)$	10
$R_{p1}(10^{-6}cm)$	2.171	$\Delta L_{met}(\mu m)$	0.2
$\Phi_2(10^{12}cm^{-2})$	1.698	†$N^-_{max}(10^{18}cm^{-3})$	0.64
$\Delta R_{p2}(10^{-5}cm)$	1.559	†$R^-_{pd}(10^{-4}cm)$	0.152
$R_{p2}(10^{-5}cm)$	3.027	†$R^-_j(10^{-4}cm)$	0.221

†for LDD devices

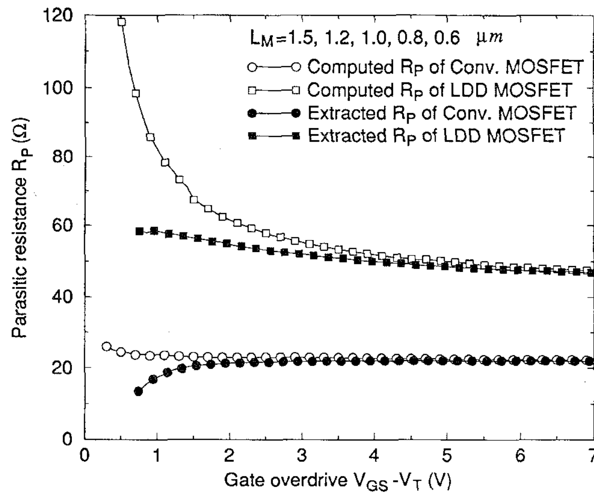


Fig. 9. Comparisons between the computed and extracted parasitic resistance versus gate overdrive for conventional and LDD MOSFET's.

TABLE II
THE EXTRACTION RESULTS FROM CONVENTIONAL AND LDD DEVICES BEFORE AND AFTER V_T CORRECTION FOR VARIOUS STRUCTURES. THE PARAMETERS LISTED ARE DIFFERENT FROM TABLE I

unit (μm)	Before V_T Correction (Conv./LDD)	After V_T Correction (Conv./LDD)
As Table I	0.203/0.187	0.207/0.200
$\Phi_1 = 1.15 \times 10^{12} cm^{-3}$	0.196/0.163	0.199/0.199
T_{ox} =100 Å	0.197/0.162	0.202/0.191
$f = 0.9$	0.197/0.188	0.201/0.201
$R_{co} = 25\Omega$	0.202/0.186	0.206/0.199
$\Delta L_{met} = 0.5\mu m$	0.506/0.452	0.509/0.503

The extracted and computed (from simulator) R_P are plotted in Fig. 9. As indicated, the larger R_P values emphasize the importance of V_T correction for LDD devices. For conventional devices, R_P at low gate overdrive is smaller than that at high gate overdrive. This is due to large R_{c1}, R_{c2} and small R_n at low gate overdrive. However, for LDD devices, the behaviors of R_{c1} and R_{c2} are similar to those of conventional devices, but R_n is large enough to compensate R_{c1} and R_{c2}. So R_P still increases; unlike the conventional devices, it decreases as the gate bias is reduced. Anyway, the extracted R_P is always smaller than the computed results using a simulator at any gate overdrive for both devices, because we cannot evaluate R_{c1} and R_{c2}.

To verify the validity of this extraction algorithm for various device structures, many cases are simulated by the SUMMOS. In addition to the previous case, other cases for different channel dopings, oxide thicknesses, lateral diffusion coefficients, contact resistances and ΔL_{met} are examined. The parameters used and the extraction results are listed in Table II for conventional and LDD devices. It is shown that fairly good agreements are obtained. Again, we find that the V_T correction is more important for LDD than conventional devices. Comparing the extracted ΔL_{met} with the given value, the variations for all cases are smaller than 0.01 μm. This indicates that our extraction algorithm is valid for all device structures.

TABLE III
COMPARISONS OF THE EXTRACTION RESULTS BETWEEN THIS ALGORITHM AND THE METHOD PROPOSED IN [15]

Wafer No.	T_{ox} (Å) / $N_A(cm^{-3})$	ΔL_{met} (Before)	ΔL_{met} (After)	ΔL_{met} (in [15])
L13343-05	100 / 10^{17}	0.163	0.171	0.205
L13343-15	140 / 6×10^{16}	0.180	0.195	0.215
L13343-17	140 / 10^{17}	0.165	0.170	0.190
L13343-19	140 / 2×10^{17}	0.181	0.188	0.185
L13343-32	200 / 10^{17}	0.166	0.170	0.210
† L23003-36	140 / 10^{17}	0.334	0.404	0.395

†LDD devices

The conventional devices consisting of different oxide thicknesses and channel concentrations are fabricated, and the I-V characteristics are measured by HP-4145B. Applying our extraction algorithm to the I-V characteristics of these devices, the extraction results are listed in Table III. In Table III, wafer Nos. 5, 17 and 32 have different oxide thicknesses with the same channel doping, the extraction results show that ΔL_{met} is 0.170 μm with small variation. A quite reasonable conclusion can be drawn for these cases—the oxide thickness doesn't influence ΔL_{met}. However, wafer Nos. 15, 17 and 19 have different channel implantation doses with the same oxide thickness, the extracted ΔL_{met} value varies from 0.170 to 0.195 μm. In theory, the higher channel concentration should reduce ΔL_{met} slightly. This phenomenon is not shown in Table III. The discrepancy may be resulted from the nonuniform channel profile in the lateral direction due to the reverse short channel effect, which is more serious for heavy channel implantation [14].

The test devices with the LDD structure are also fabricated and examined, as shown in Table III, in which a novel channel-length extraction method using the charge pumping technique [15] is also performed. Comparing with our extraction results, it is shown that very good agreements are obtained.

V. CONCLUSION

A new extraction algorithm for the metallurgical channel length and the parasitic resistance of conventional and LDD MOSFET's is described. With our proposed technique, the errors induced by channel-length uncertainty and the effects of parasitic source/drain resistance on the threshold voltage are reduced. A 2-D numerical analysis is performed to analyze the factors affecting the effective channel length, and the ex-

traction principles for ΔL_{met} are proposed. The principles for extracting the metallurgical channel length deduced from the 2-D numerical analysis are also evaluated by a simple analytic model. Comparing with 2-D numerical analysis, the analytic model evaluation is proven to be a reasonable approximation.

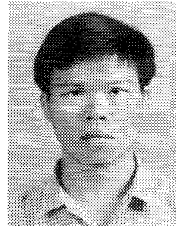
The proposed extraction algorithm has been verified by the simulated I-V characteristics, and the error is within 0.01 μm. Moreover, the parasitic source/drain resistance is also extracted, and it is shown that smaller parasitic resistance at low gate overdrive is inevitable. Compared with the computation results, the extraction results are fairly accurate. Applying this extraction algorithm to the experimental devices and comparing with the results extracted by the charge pumping method, it is shown that very good agreements between these two methods are obtained.

ACKNOWLEDGMENT

The authors would like to express their sincere thanks to the National Science Council, Taiwan, Republic of China, for continuous grant support. Special thanks are given to the Electronics Research and Service Organization (ERSO), Industrial Technology Research Institute (ITRI), Taiwan, Republic of China, for providing the test devices.

REFERENCES

[1] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, vol. 18, no. 5, p. 953, May 1979.
[2] J. G. J. Chern *et al.*, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. EDL-1, no. 9, p. 170, Sept. 1980.
[3] F. E. de la Moneda *et al.*, "Measurement of MOSFET constants," *IEEE Electron Device Lett.*, vol. EDL-3, no. 1, p. 10, Jan. 1982.
[4] K. L. Peng *et al.*, "Basic parameter measurement and channel length broadening effect in submicronmeter MOSFET," *IEEE Electron Device Lett.*, vol. EDL-5, p. 473, Nov. 1984.
[5] S. E. Laux, "Accuracy of an effective channel length/external resistance extraction algorithm for MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-31, no. 9, p. 1245, Sept. 1984.
[6] G. J. Hu *et al.*, "Gate-voltage-dependent effective channel length and serious resistance of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-34, no. 12, p. 2469, Dec. 1987.
[7] Y. Taur *et al.*, "A new 'shift and ratio' method for MOSFET channel-length extraction," *IEEE Electron Device Lett.*, vol. EDL-13, no. 5, p. 267, May 1992.
[8] J. Y.-C. Sun *et al.*, "On the accuracy of channel length characterization of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, no. 10, p. 1556, Oct. 1986.
[9] B. J. Sheu and P. K. Ko, "A capacitance method to determine channel length for conventional and LDD MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-5, no. 11, p. 10, Nov. 1982.
[10] S.-W. Lee, "A capacitance-based method for experimental determination of metallurgical channel length of submicron LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-41, no. 3, p. 403, Mar. 1994.
[11] R. K. Perng, "An efficient two-dimensional MOS simulator (SUMMOS) and its application," Ph.D. Dissertation, Inst. of Electronics, National Chiao-Tung University, Taiwan, R.O.C, July 1991.
[12] W. C. Johnson and P. T. Panousis, "The influence of Debye length on the C-V measurement of doping profiles," *IEEE Trans. Electron Devices*, vol. ED-18, no. 10, p. 965, Oct. 1971.
[13] S. A. Schwarz and S. E. Russek, "Semi-empirical equations for electron velocity in silicon: Part II—MOS inversion layer," *IEEE Trans. Electron Devices*, vol. ED-30, no. 12, p. 1634, Dec. 1983.
[14] M. Orlowski *et al.*, "Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion," *IEDM Tech. Dig.*, p. 632, 1987.
[15] H. H. Li and C. Y. Wu, "A novel extraction technique for the effective channel length of MOSFET devices," *IEEE Trans. Electron Devices*, vol. 42, no. 5, p. 856, May 1995.



Yuh-Sheng Jean (S'90) was born in Taiwan, Republic of China, on July 5, 1968. He received the B.S. degree in electrical engineering from the National Central University, Taiwan, in 1990. He is currently working toward the Ph.D. degree in the Institute of Electronics, National Chiao-Tung University. His research areas focus on deep-submicrometer MOS device physics and reliability issues.

Ching-Yuan Wu (M'72) was born in Taiwan, Republic of China, on March 18, 1946. He received the B.S. degree in electrical engineering from the National Taiwan University, Taiwan, in 1968, and the M.S. and Ph.D. degrees from the State University of New York at Stony Brook in 1970 and 1972, respectively.

During the 1972–1973 academic year, he was appointed as a Lecturer, Department of Electronical Sciences, SUNY-Stony Brook. During the 1973–1975 academic years, he was a Visiting Associate Professor at the National Chiao-Tung University (NCTU), Taiwan. In 1976, he became Full Professor in the Department of Electronics and the Institute of Electronics at NCTU. While there he was the Director of the Engineering Laboratories and Semiconductor Research Center from 1974 to 1980, the Director of the Institute of Electronics from 1978 to 1984, and the Dean of the College of Engineering from 1984 to 1990. He was a principal investigator of the National Electronics Mass Plan-Semiconductor Devices and Integrated-Circuit Technologies from 1976 to 1979, and had been a Coordinator of the National Microelectronics Researches and High-Level Man-Power Education Committee, National Science Council, Republic of China from 1982 to 1988. He has been the Research Consultant of the Electronics Research and Service Organization (ERSO), ITRI, a member of the Academic Review Committee in the Ministry of education, and the chairman of the Technical Review Committee on Information and Microelectonics Technologies at the Ministry of Economic Affairs. His research activities have been in semiconductor device physics and modeling, integrated-circuit designs, and technologies. His current research areas focus on the developments of efficient 2D and 3D simulators for deep-submicrometer semiconductor devices, design rules and optimization techniques for deep-submicrometer CMOS devices. He has published over 180 papers in the semiconductor field and has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES and *Solid State Electronics*.

Dr. Wu is a member of the Honorary Editorial Advisory Board of *Solid State Electronics*, and is a board member of the Chinese Engineering Society. He received the Academic Research Award in Engineering from the Ministry of Education (MOE), in 1979 and the Outstanding Scholar Award from the Chinese Educational and Cultural Foundation in 1985. He received the outstanding research Professor fellowship from the Ministry of Education and the National Science Council (NSC), Republic of China from 1982 to 1995. He received the Distinguished Engineering Professor Medal Award from the Chinese Engineering Society in 1992.