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Electrostatic discharge protection scheme without leakage current path for CMOS IC operating in power-down-mode condition on a system board

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Abstract

A new design on the electrostatic discharge (ESD) protection scheme for CMOS IC operating in power-down-mode condition is proposed. By adding a VDD_ESD bus line and diodes, the new proposed ESD protection scheme can block the leakage current from I/O pin to VDD power line to avoid malfunction during power-down-mode operating condition. During normal circuit operating condition, the new proposed ESD protection schemes have no leakage path to interfere with the normal circuit functions. The whole-chip ESD protection design can be achieved by insertion of ESD clamp circuits between VSS power line and both VDD power line and VDD ESD bus line. Experimental results have verified that the human-body-model (HBM) ESD level of this new scheme can be greater than 7.5 kV in a 0.35-μm silicided CMOS process. Furthermore, output-swing improvement circuit is proposed to achieve the full swing of output voltage level during normal circuit operating condition.
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1. Introduction

Nowadays power-down-mode feature plays an important role in portable and mobile SOC (System on a Chip) products that require effective power saving. In order to achieve IC power-down-mode operation, modification on I/O circuits and ESD protection circuits has been studied [1,2]. An example of two chips connected in an electronic system is shown in Fig. 1, where the output pad (O/P) of the chip_1 is connected to the input pad (I/P) of the chip_2. When the chip_2 goes into the power-down-mode operation, two situations are explained as follows. First, if VDD2 power line is grounded, a large leakage current may be induced from the input pad to the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the voltage level at the output pin of chip_1 is high. Second, if the VDD2 power line is floating, the internal circuits of chip_2 may be triggered to cause malfunction by charging the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the voltage level at the output pin of chip_1 is high. Therefore, the parasitic diode of pMOS connected

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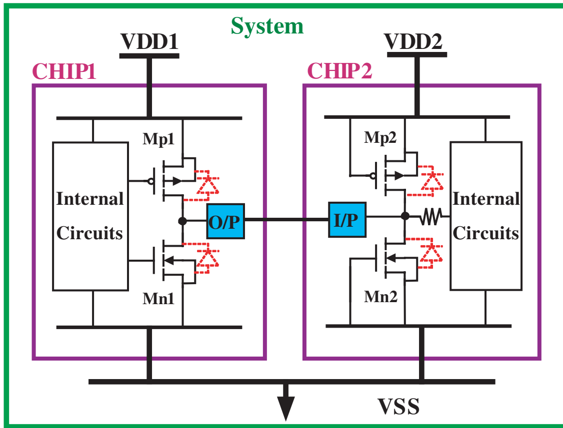


Fig. 1. An example to show the power-down-mode operation issue on a system with two chips, which are biased with separated VDD1 and VDD2 power supplies.

between the input pad and VDD2 power line must be removed to avoid leakage current or malfunction, when the chip_2 goes into the power-down-mode operation in this typical example.

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Fig. 2(a)–(d), respectively [3]. For the purpose of avoiding the unexpected ESD damage in the internal circuits of CMOS ICs [4–6], the turn-on-efficient power-rail ESD clamp circuit was often placed between VDD and VSS power lines [7]. In the traditional ESD protection scheme shown in Fig. 3, ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS and the power-rail ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the power-rail ESD clamp circuit can achieve a much higher ESD level [7]. However, the absence of the diode between I/O pad and VDD power line for power-down-mode operation will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses.

In order to solve the ESD protection and leakage issue for IC with power-down-mode operation, some modified designs had been reported [8,9]. The gate-grounded nMOS has been used to replace the diode between the I/O pad and VDD power line [8]. In [9],

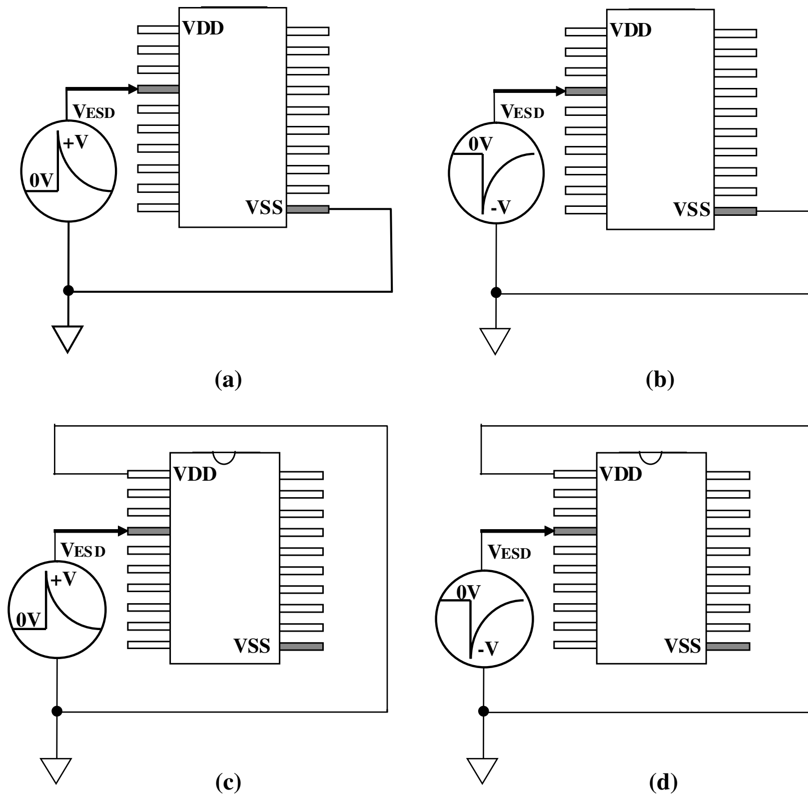


Fig. 2. The four pin-combination modes for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode) [3].

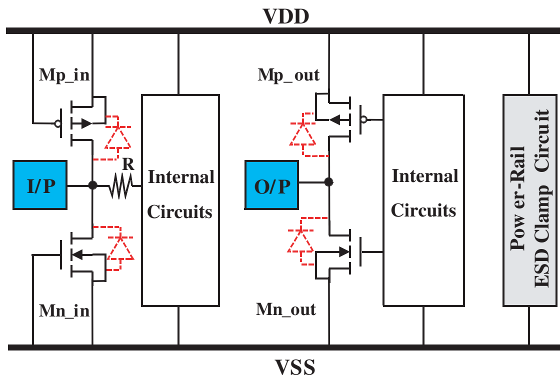


Fig. 3. Traditional ESD protection scheme in a CMOS IC with pMOS and nMOS as ESD protection devices for input and output pads.

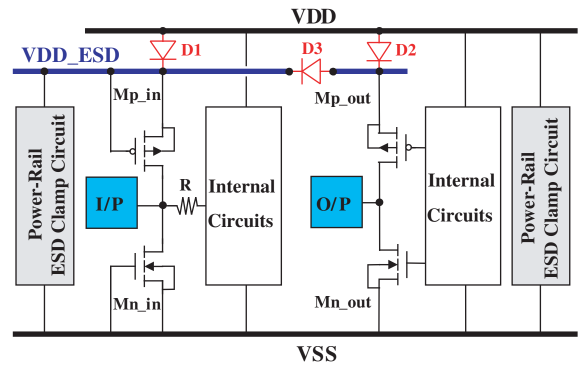


Fig. 4. The new proposed ESD protection scheme I for the IC with power-down-mode operation.

the design was focused on improving ESD robustness of the ESD protection circuit between the I/O pad and VSS power line. However, the turn-on efficiency of ESD protection device [8] or the complicated ESD protection circuit [9] could not be able to protect the internal circuits in such IC applications with power-down-mode operation, especially under the pin-to-pin ESD zapping condition [3]. Recently, a new ESD protection design with the extra VDD_ESD bus had been reported in [10,11] to solve this power-down-mode operation with consideration on ESD discharging paths for pin-to-pin ESD stresses.

In this work, two further modified ESD protection designs from [10] are proposed. These new schemes can overcome the leakage issue and have very high ESD level for IC with power-down-mode operation. Furthermore, the output-swing improvement circuit is proposed to achieve the full swing of output voltage level during normal circuit operating condition. These two modified ESD protection designs have been successfully verified in a 0.35-μm silicided CMOS process.

2. New ESD protection schemes for IC with power-down-mode operation

2.1. ESD protection scheme I

The proposed ESD protection scheme I for the IC with power-down-mode operation is shown in Fig. 4 with the additional ESD bus line (VDD_ESD), which is realized by wide metal line in CMOS IC. The VDD_ESD bus line is not directly connected to an external power supply pin, and it is separated into input stage and output stage by the diode D3. The VDD_ESD bus line of output stage is connected to the source of output pMOS (Mp_out). The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input pad to VDD when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of Mp_out to block the leakage current path from the output pad to VDD when the power of VDD is off. The gate voltage of Mp_out will be dropped down to induce leakage current between I/O pads when the power of VDD is off. The diode of D3 is used to block the leakage current between the I/O pads. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between VDD_ESD bus line and VSS power line. In some mixed-voltage I/O buffers, the output pMOS, connected from the I/O pad to the VDD power line, has self-biased circuits for tracking its gate and n-well voltages to avoid the leakage current path from the I/O pad to VDD when an over-VDD external signal is applied to the I/O pad [12]. However, during the power-down-mode operation, the tracking circuits have no function because the power of VDD is off. The channel of output pMOS cannot be kept off when the external voltage level connected to the output pad is high. Therefore, the leakage current may be induced from the output pad to VDD when the power of VDD is off. By using the new proposed ESD protection scheme, the leakage current path from the I/O pad to VDD can be completely blocked by the diode D2 during the power-down-mode operation.

The ESD current discharging paths of the input pad under PS-mode ESD stress condition, the output pad under PS-mode ESD stress condition, the input pad under PD-mode ESD stress condition, and the output pad under PD-mode ESD stress condition are shown in Fig. 5(a)–(d), respectively. The ESD current at the input (or output) pad under PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to the VDD_ESD bus, (the diode of D3,) and then discharged through the power-rail ESD clamp

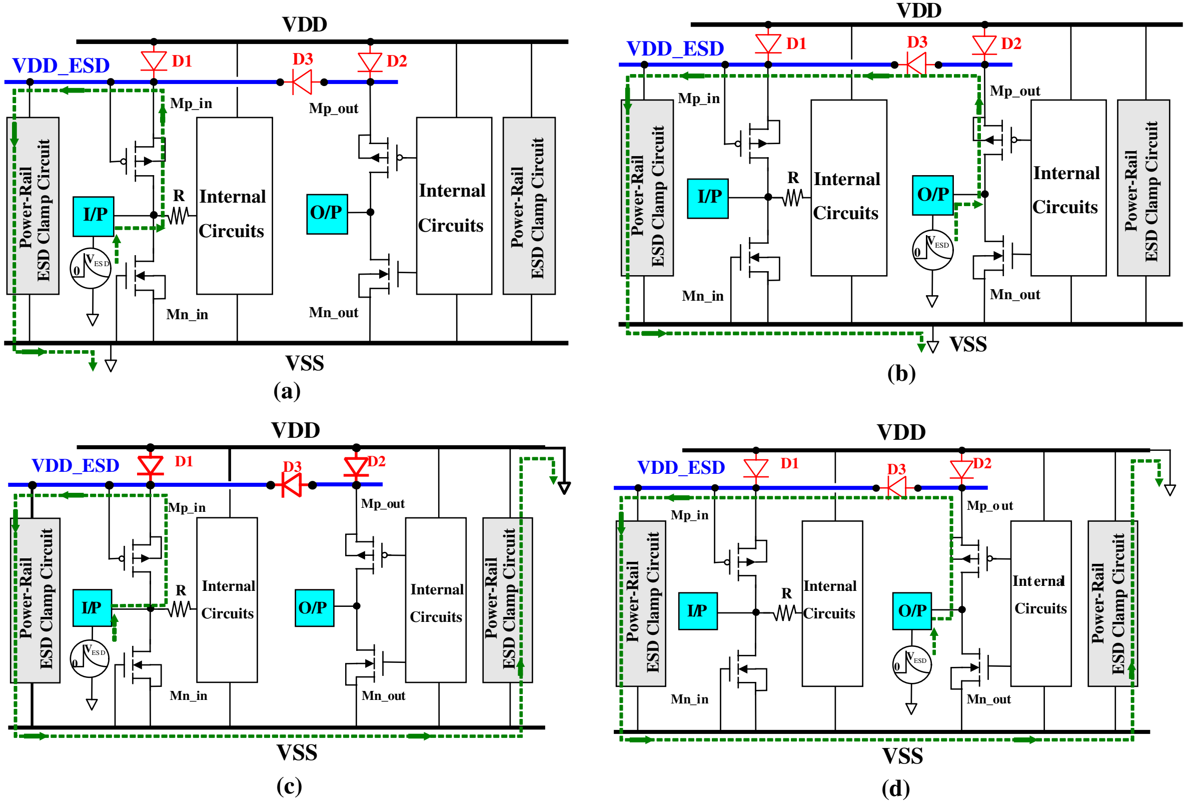


Fig. 5. The ESD current discharging paths of (a) the input pad under PS-mode ESD stress condition, (b) the output pad under PS-mode ESD stress condition, (c) the input pad under PD-mode ESD stress condition, and (d) the output pad under PD-mode ESD stress condition.

circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to VDD_ESD bus line, (the diode of D3,) the power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD power line. The negative ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The negative ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to VSS power line, and then discharged through the power-rail ESD clamp circuit to the grounded VDD power line. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed ESD protection scheme.

2.2. ESD protection scheme II

The proposed ESD protection scheme II for the IC with power-down-mode operation is shown in Fig. 6.

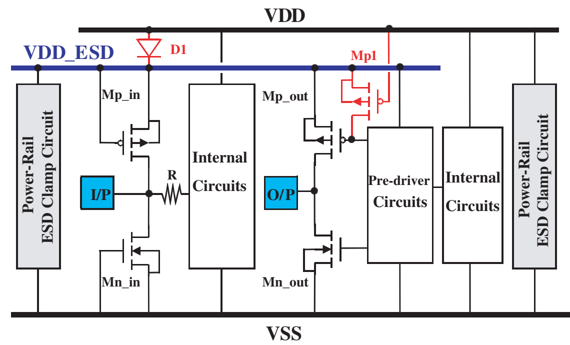


Fig. 6. The new proposed ESD protection scheme II for the IC with power-down-mode operation.

The design concept is similar to that of the ESD protection scheme I. The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input or output pad to VDD, when the power of VDD is off. The diode D3 in scheme I is replaced by the Mp1 in scheme II to block the leakage current between the I/O pads when the

power of VDD is off. The gate of Mp1 is connected to the VDD power line. Therefore, Mp1 is turned off under the normal circuit operating condition. Under power-down-mode operating condition, Mp1 is turned on to keep the Mp_out off. In addition, the power line of the pre-driver internal circuits which controlled the gate of Mp_out is connected to the VDD_ESD bus line to avoid the leakage current from the pre-driver internal circuits to VDD power line, when the power of VDD is off. The ESD current at the input (or output) pad under PS-mode ESD stress condition can be discharged through the parasitic diode of Mp_in (or Mp_out) and the power-rail ESD clamp circuit between the VDD_ESD bus line and the VSS power line to ground. The ESD current at the input (or output) pad under the PD-mode ESD stress condition can be discharged through the parasitic diode of Mp_in (or Mp_out) to VDD_ESD bus line, the power-rail ESD clamp circuit to VSS power line, and then the parasitic diode of ESD clamp circuit to the grounded VDD power line.

Therefore, with the new proposed ESD protection schemes, the leakage current or malfunction issues for the IC with power-down-mode operation can be avoided. The internal circuits of CMOS IC can be fully protected against ESD damage by the new proposed ESD protection schemes.

2.3. Layout consideration

For saving the layout area, the VDD_ESD bus line in the proposed ESD protection schemes can be realized by the different parallel metal layer, which overlaps the VDD power line. The junction perimeter of the diodes (D1, D2, and D3) in the proposed ESD protection schemes can be drawn with small layout area, because the ESD current is discharged through these diodes with the forward-diode path. The device dimension of Mp1 in scheme II can be adjusted with less impact on ESD performance. In addition, it's important to note that the location of power-rail ESD clamp circuit connected between VDD_ESD bus line and VSS power line is an important factor to implement the ESD protection scheme I. Because the ESD bus line is separated into input stage and output stage by the diode D3, the power-rail ESD clamp circuit must be placed in the input stage to provide the ESD current discharging path for input pad under ESD stress.

3. Experimental results

The testchip with traditional and new proposed ESD protection schemes had been fabricated in a 0.35-μm silicided CMOS process. Some inverters are connected from the input pad to the output pad, being served as the internal circuits for function verification of this testchip. The input ESD protection devices are realized by the gate-connected-to-source pMOS and gate-grounded nMOS with both the device dimensions (W/L) of 490/0.5 (μm/μm). The output ESD protection devices are realized by the output buffer of pMOS and nMOS with the same device dimensions. The layout parameters of ESD protection devices and output buffers are drawn according to the foundry's ESD rules with the silicide-blocking mask. In the proposed ESD protection scheme I, the junction perimeter of the diodes (D1, D2, and D3) is drawn as 50 μm. In the proposed ESD protection scheme II, the junction perimeter of the diode (D1) is drawn as 50 μm, and the device dimension (W/L) of Mp1 is drawn as 20/0.5 (μm/μm). The power-rail ESD clamp circuit is realized by the substrate-triggering field-oxide device (STFOD) [13,14] to have high enough ESD level in a limited layout area.

3.1. Leakage current

The leakage currents at the input pad of the traditional and new proposed ESD protection schemes under normal circuit operating condition are compared in Fig. 7(a). The leakage current is measured by applying a voltage ramp from 0 to 3.3 V to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In Fig. 7(a), the leakage currents at the input pad of traditional ESD protection scheme, new proposed ESD protection schemes I, and II are 109 pA, 132 pA, and 122 pA, respectively, with a 3.3-V signal applying to the input pad. From the measured results, the new proposed ESD protection schemes do not induce any extra leakage current under normal circuit operating condition.

The leakage currents at input pad and output pad of the traditional and new proposed ESD protection schemes under power-down-mode operating condition are measured and compared in Fig. 7(b) and (c), respectively. The leakage current is measured by applying a voltage ramp from 0 to 3.3 V to the input or output pad under the bias condition of 0-V VDD and 0-V VSS. From the measured results, the leakage currents at the input pads (output pads) of the new proposed ESD protection schemes are only ~130 pA in Fig. 7(b) (~300 pA in Fig. 7(c)), when a 3.3-V signal is applied to the input pad (output pad). On the contrary, the traditional ESD protection scheme has a very high leakage current of up to several milliamperes when the input or output voltage is only increased to 0.7 V. The leakage current in the new proposed ESD protection scheme has been successfully blocked by the diode of D1 or D2. The experimental results have verified that the new proposed ESD protection schemes can avoid the leakage current from the I/O pin to VDD power line under the power-down-mode operating condition.

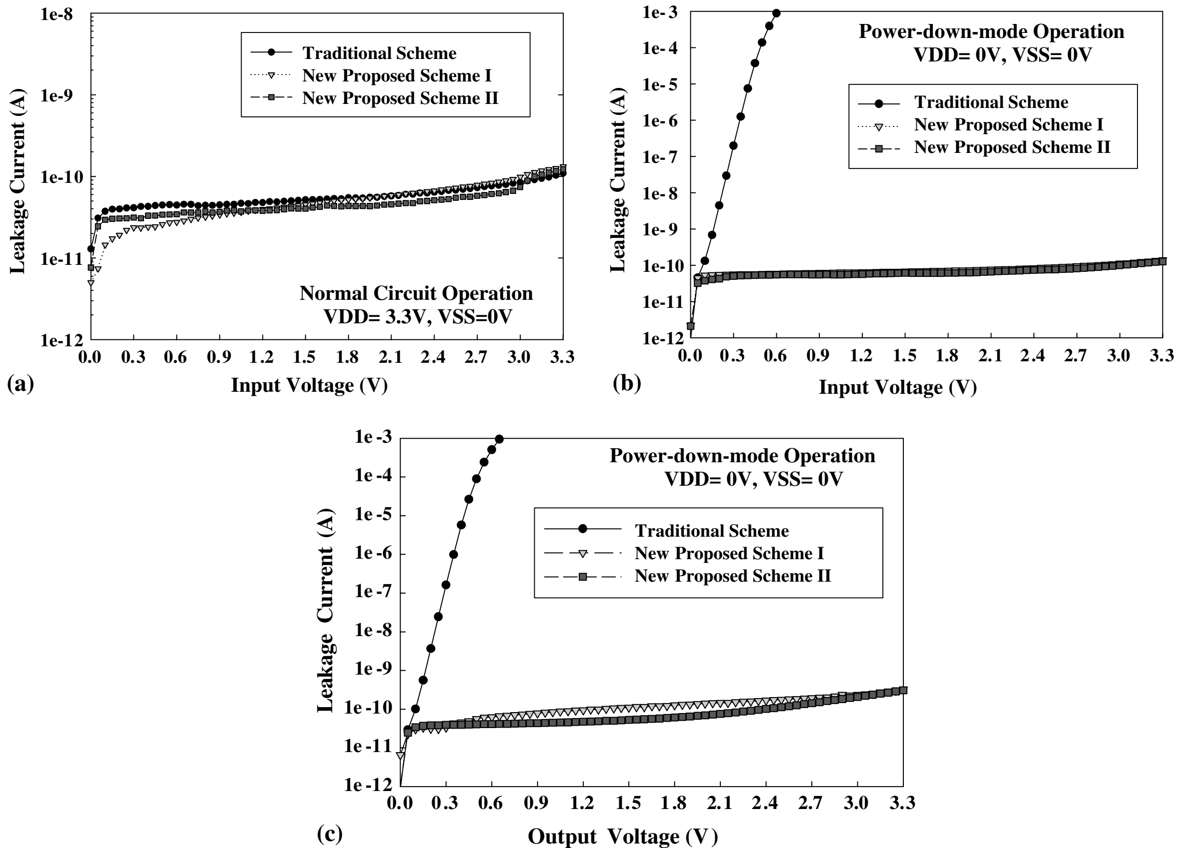


Fig. 7. Comparison of the measured leakage currents at (a) the input pad under normal circuit operating condition, (b) the input pad under power-down-mode operating condition, and (c) the output pad under power-down-mode operating condition, of the traditional and new proposed ESD protection schemes.

3.2. Function verification

The measurement setup to verify the function of I/O cells with the new proposed ESD protection schemes, or the traditional ESD protection scheme, under normal circuit operating condition and power-down-mode operating condition is shown in Fig. 8. To verify the function among the different designs under normal circuit operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In addition, to verify the function among the different designs under power-down-mode operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 0-V VSS but VDD is floating.

Fig. 9(a) and (b) show the voltage waveforms on the input/output pad of the I/O cells with the traditional ESD protection scheme under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 9(a), the I/O cells with

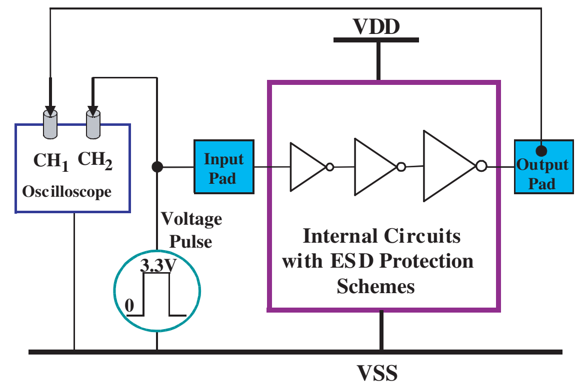
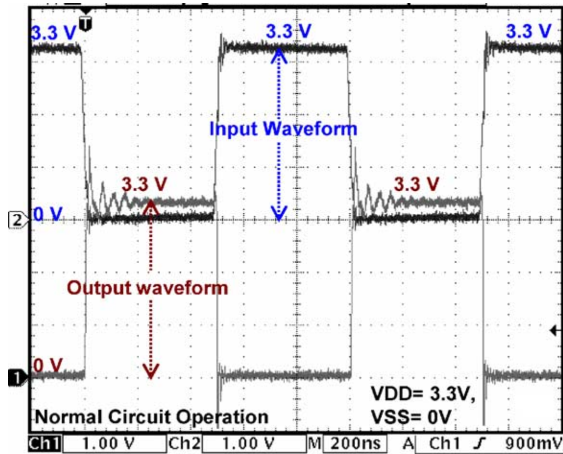
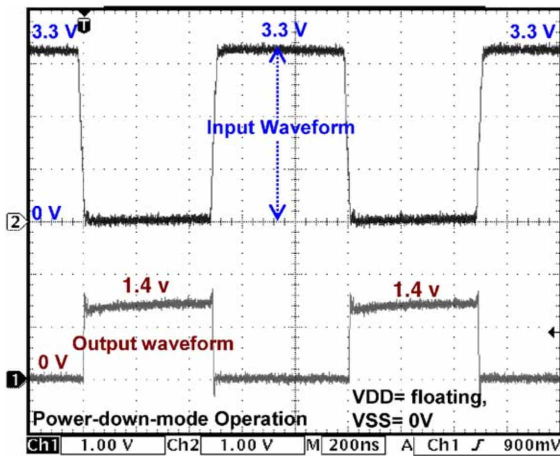


Fig. 8. The measurement setup to verify the function of I/O cells with the new proposed ESD protection schemes, or the traditional ESD protection scheme, under normal circuit operating condition and power-down-mode operating condition.

traditional ESD protection circuits can be operated normally under normal circuit operating condition.

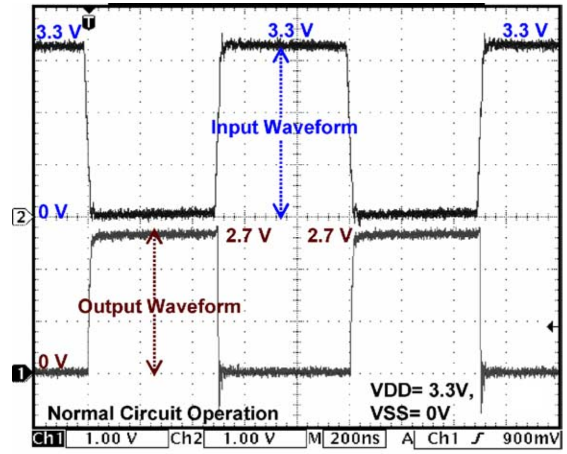


(a)

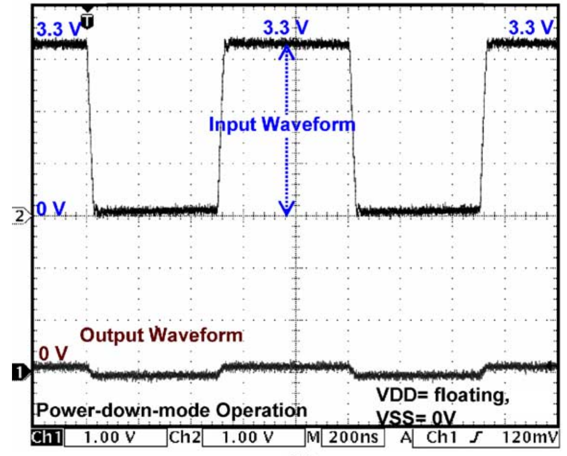


(b)

Fig. 9. The measured voltage waveforms on the input/output pad of IC with the traditional ESD protection scheme under (a) normal circuit operating condition with VDD = 3.3 V and VSS = 0 V, and (b) power-down-mode operating condition with VDD = floating and VSS = 0 V. (Y-axis = 1 V/Div., X-axis = 200 ns/Div.)



(a)



(b)

Fig. 10. The measured voltage waveforms on the input/output pad of IC with the proposed ESD protection scheme I under (a) normal circuit operating condition with VDD = 3.3 V and VSS = 0 V, and (b) power-down-mode operating condition with VDD = floating and VSS = 0 V. (Y-axis = 1 V/Div., X-axis = 200 ns/Div.)

However, under the power-down-mode condition, the voltage waveform on the output pad is dropped to a voltage level of ~1.4 V, when the input voltage level is 0 V, as that shown in Fig. 9(b). It implies that the internal circuits are triggered by the input voltage waveform under power-down-mode operating condition, although the circuits are expected to be off. With the wrong voltage waveform at the I/O pads, the system could be malfunction.

Fig. 10(a) and (b) show the voltage waveforms on the input/output pad of the I/O cells with the new proposed ESD protection scheme I under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 10(a), the I/O cells with the new proposed ESD protection scheme I can be operated normally under normal circuit operating condition. The high voltage level on the output pad is kept at ~2.7 V (VDD-V_d, where V_d is the cut-in voltage of the diode D2). In Fig. 10(b), the voltage level on the output pad is always kept at ~0 V under power-down-mode operating condition. This result has verified that the internal circuits can be really kept inactive by the new proposed ESD protection scheme I under power-down-mode operating condition. In addition, the measured voltage waveforms on the input/output pad of I/O cells with the proposed ESD protection scheme II have the same results as those shown in Fig. 10(a) and (b) under normal circuit operating condition and

Table 1
HBM ESD robustness of the traditional ESD protection scheme and the new proposed ESD protection schemes

ESD protection scheme	HBM ESD stress					
	PS-mode VSS(+), kV	NS-mode VSS(−), kV	PD-mode VSS(+), kV	ND-mode VSS(−), kV	VDD-to-VSS(+), kV	VDD-to-VSS(−), kV
Traditional scheme (input pin)	7.5	>8	>8	5	5	>8
Traditional scheme (output pin)	7.5	>8	>8	5		
New proposed scheme I (input Pin)	7.5	>8	7.5	>8	>8	>8
New proposed scheme I (output pin)	7.75	>8	7.75	>8		
New proposed scheme II (input pin)	7.75	>8	7.75	>8	>8	>8
New proposed scheme II (output pin)	7.5	>8	>8	>8		

power-down-mode operating condition, respectively. The experimental results have verified that the I/O cells with the proposed ESD protection scheme II can be normally operated under normal circuit operating condition, as well as the internal circuits can be really kept inactive under power-down-mode operating condition.

3.3. ESD robustness

The human-body-model (HBM) ESD robustness of I/O pads with the traditional or new proposed ESD protection schemes under different pin combinations is listed in Table 1. The failure criterion is defined as the leakage current of the circuits after ESD stress is greater than 1 μA under the normal operating voltage of 3.3 V. With the traditional ESD protection scheme, the ESD level of the I/O pads is 5 kV, which is dominated by the I/O pad under the ND-mode ESD stress or positive VDD-to-VSS ESD stress. However, with the new proposed ESD protection schemes I and II, the ESD level of the I/O pads is 7.5 kV, which is dominated by the I/O pad under the PS-mode or PD-mode ESD stress. The ESD level of I/O pad under the ND-mode ESD stress or VDD-to-VSS ESD stress is improved by the extra ESD current path in the new proposed ESD protection scheme, which is discharged through the diode D1 and power-rail ESD clamp circuit between the VDD_ESD bus line and VSS power line. As a result, ESD level of the whole chip can be efficiently improved by the new proposed ESD protection schemes for IC with power-down-mode operation.

3.4. Output-swing improvement circuit

Although the output signal of the new proposed ESD protection scheme was not pulled up to full-VDD voltage swing during normal circuit operating condition, it can be further improved with additional output-swing improvement circuit. This circuit block connecting between the VDD power line and VDD_ESD bus line in the ESD protection scheme I is shown in Fig. 11(a). The circuit diagram of output-swing improvement circuit is shown in Fig. 11(b). In this circuit, Mp1 is used as a pull-up device to achieve the full-VDD voltage swing of output signal. During normal circuit operating condition, Mp1 is always turned on. Thus, the output signal can be pulled up to VDD by the turn-on of Mp_out controlled by the pre-driver circuits. Therefore, the device size of Mp1 is determined by the driving current of the output cell in a CMOS IC. During power-down-mode operating condition, Mp1 is turned off to avoid the leakage current path from the output pad to VDD. The Mn1 and Mp2 in this circuit are used to control the gate of Mp1 during normal circuit operating

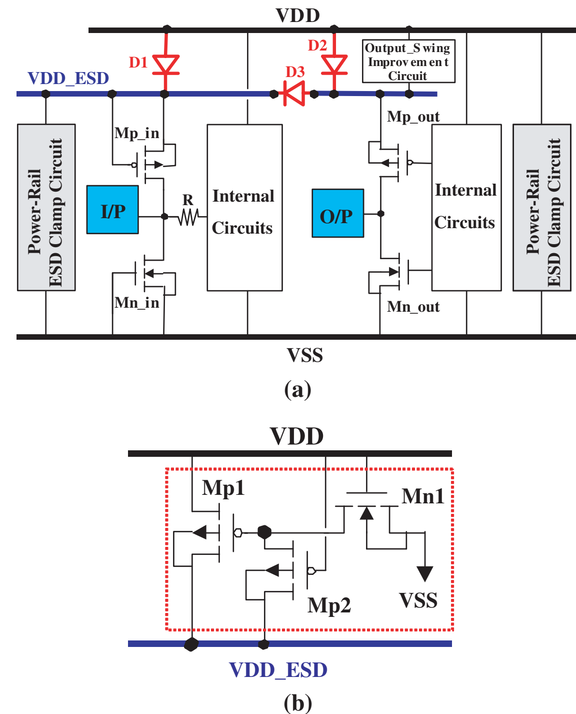


Fig. 11. (a) The output-swing improvement circuit connecting between the VDD power line and VDD_ESD bus line in the ESD protection scheme I. (b) The circuit diagram of output-swing improvement circuit.

condition and power-down-mode operating condition, respectively. The gates of Mn1 and Mp2 are connected to the VDD power line. Therefore, Mp2 is turned off, and Mn1 is turned on to keep the gate voltage of Mp1 at ~0 V under normal circuit operating condition. With the turn-on of Mp1, the output signal can be pulled up to full-VDD voltage swing under normal circuit operating condition. Under power-down-mode operating condition with the bias condition of 0-V VDD, Mn1 is turned off, and Mp2 is turned on to keep the Mp1 off. The bodies (n-well) of Mp1 and Mp2 are connected to the VDD_ESD bus line to avoid the leakage path of the parasitic diode under power-down-mode operating condition. Therefore, no extra leakage current will be induced under the power-down-mode operating condition. This output-swing improvement circuit has been fabrication with the new proposed ESD protection scheme in a 0.35-μm CMOS process to verify its effectiveness.

The leakage currents at I/O pads of new proposed ESD protection scheme I with output-swing improvement circuit under normal circuit operating condition and power-down-mode operating condition are measured in Fig. 12. From the measured results, no extra leakage current is induced by adding output-swing improvement circuit in the new proposed ESD protection scheme under both normal circuit operating condition and power-down-mode operating condition.

Fig. 13(a) and (b) show the voltage waveforms on the input/output pad of the new proposed ESD protection scheme with the output-swing improvement circuit under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 13(a), the output signal has been really pulled up to full-VDD voltage swing under normal circuit operating condition, when the input voltage level is 0 V. In Fig. 13(b), the internal circuits can be really kept off under power-down-mode operating condition. Therefore, the output signal of the proposed ESD protection scheme can be pulled up to VDD by the output-swing improvement circuit under normal circuit operating condition, without increasing any leakage current.

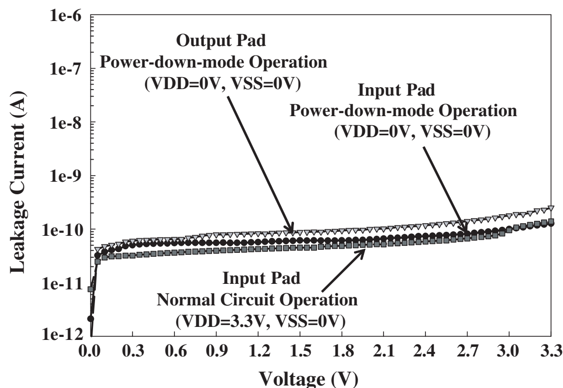
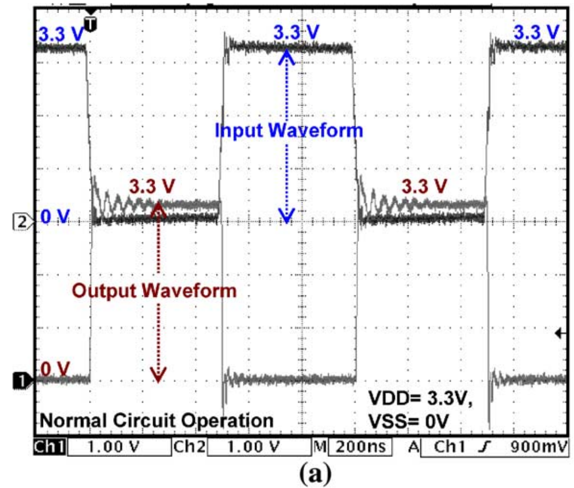


Fig. 12. The measured leakage currents at I/O pads of new proposed ESD protection scheme I with the output-swing improvement circuit under normal circuit operating condition and power-down-mode operating condition.



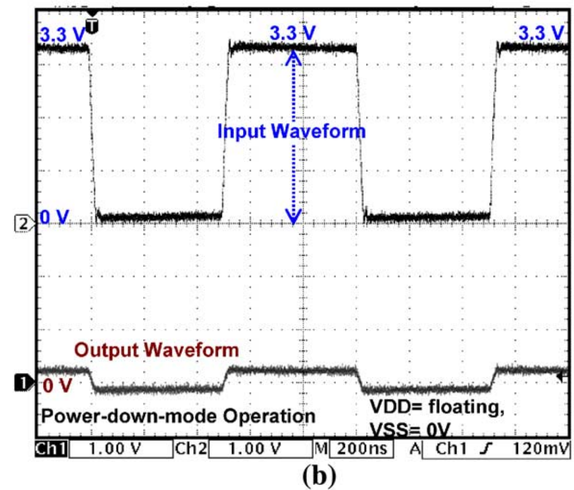


Fig. 13. The measured voltage waveforms on the input/output pad of the proposed ESD protection scheme I with output-swing improvement circuit under (a) normal circuit operating condition with VDD = 3.3 V and VSS = 0 V, and (b) power-down-mode operating condition with VDD = floating and VSS = 0 V. (*Y*-axis = 1 V/Div., *X*-axis = 200 ns/Div.)

4. Conclusion

Two modified ESD protection schemes without leakage current path for CMOS IC operating in power-down-mode condition has been successfully designed and verified in a 0.35-μm silicided CMOS process.

Under the normal circuit operating condition, the I/O cells with the new modified ESD protection schemes can be operated normally. Under the power-down-mode operating condition, the new modified ESD protection schemes can provide the I/O pad without leakage path, and avoid triggering the internal circuits those should be "off". High ESD robustness has been practically achieved in the testchip with these two new modified ESD protection schemes to sustain HBM ESD stress of up to 7.5 kV in a 0.35-μm silicided CMOS process. Furthermore, the output signal of the new modified ESD protection schemes can be successfully pulled up to VDD again by the output-swing improvement circuit under normal circuit operating condition.

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