# A Full Code-Patterns Coverage High-Speed Embedded ROM Using Dynamic Virtual Guardian Technique

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***Abstract*—Crosstalk between bitlines induces read failure and limits the coverage of applicable code-patterns for high-speed contact/via-programming read-only memories (ROMs) in SoC. Owing to the variation in bitline loading across code-patterns, the amount of coupled noise on an accessed bitline is code-pattern-dependent. This crosstalk effect worsens, with larger coupling capacitance and smaller intrinsic loading, as the technology node shrinks. This study proposes dynamic virtual guardian (DVG) techniques for contact/via-programming ROM macros and compilers to eliminate the crosstalk-induced read failure and increase the code-patterns coverage. Compared with conventional ROMs, DVG techniques achieve higher speed, lower power consumption and better design for manufacturing (DFM) capability with full code-patterns coverage. Experiments on fabricated designs, a conventional ROM and two 256 Kb DVG ROMs, using 0.18 $\mu$m 1P5M CMOS technology have demonstrated that DVG techniques achieve 100% code-pattern coverage under a small sensing margin.**

***Index Terms*—Code-patterns, crosstalk, ROM.**

## I. Introduction

READ-ONLY MEMORY (ROM) macros are commonly embedded in SoCs for storing codes and waveform tables. The current trends in SoCs are the demands for higher speed, lower power, larger capacity and shorter time-to-market in embedded ROMs. Compared to diffusion-programming ROMs, contact or via-programming ROM macros and compilers shorten the turn around time in manufacturing after ROM code modification [1].

Typically, the amount of coupling noise between bitlines in diffusion-programming ROMs and other memories (SRAM, DRAM, Flash) is independent of the content on a column for a given memory configuration. These nonvaried coupling noises in other memories can be overcome by twisted bitline scheme [2], [3], open/fold bitline scheme [4], multiplayer shielded bitline structure [5], or ground-shielded open-bitline sensing scheme [6]. Unfortunately, various ROM code-patterns produce large variation of coupling noise between bitlines in contact and via-programming ROMs. Thus, the crosstalk-induced read failure is code-pattern-dependent and limits the coverage rate of applicable code-patterns in contact/via-programming ROMs. Previous reports employed code inversion schemes [7], [8], precharge-discharge dynamic logics [9], charge recycling [10], limited bitline swing [11]–[14], and divided wordlines [15]–[17] to reduce the power consumption and improve the speed performance of ROMs. However, those studies do not address their solutions on the crosstalk-induced read failure across code-patterns for ROMs.

Dynamic virtual guardian (DVG) techniques are proposed to eliminate the crosstalk-induced read failure for contact/via-programming ROMs without additional ground wire routed [5] or changing bitline structure [2]–[6]. To our knowledge, this study is the first to investigate the code-pattern-dependent read failure induced by crosstalk between bitlines, and presents a solution on circuit with 100% code-pattern coverage for high-speed contact/via-programming ROMs.

The remainder of this paper is organized as follows. Section II discusses the behavior of crosstalk-induced read failure. Section III presents the proposed dynamic virtual guardian techniques. Section IV presents the experimental results. Section V draws conclusions based on the experimental results.

## II. Crosstalk-Induced Read Failure and Code-Patterns

Crosstalk-induced read failure (CIRF) and code-patterns coverage are interdependent in a contact/via-programming ROM. Various code-patterns introduce various capacitive loading and affect the generation of CIRF. CIRF, in turn, limits the coverage of applicable code-patterns in contact/via-programming ROMs.

### A. Code-Patterns

Various code-patterns cause different amounts of parasitic capacitance on bitlines and current consumption in contact/via-programming ROMs. In typical NOR-type contact/via-programming ROMs, the datum stored in a bit cell is identified by determining whether the electrical connection between the transistor of a bit cell and its bitline (BL) is on or off. A bit cell with a contact/via layer that connects its nMOS transistor to its bitline stored the datum 0 (0-cell), a cell without such a layer stored the datum 1 (1-cell). The architecture, circuit, and layout of a conventional ROM with $x$ rows and $y$ columns are illustrated in Fig. 1. When a row is activated by a wordline (WL), 0-cells sink current from their bitlines, while 1-cells do not sink any current. For a 0-cell, the parasitic

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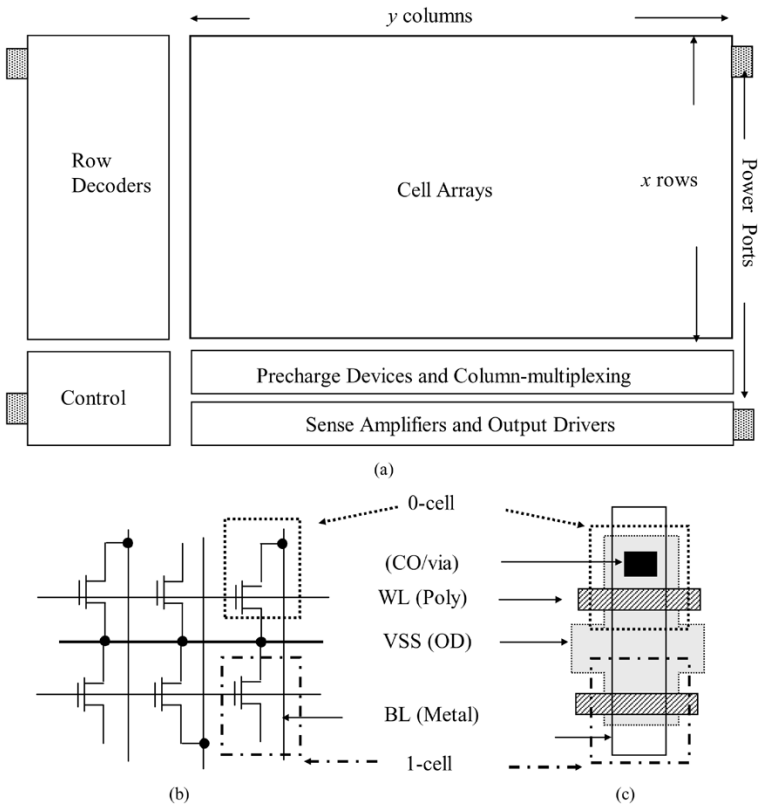


Fig. 1. (a) A conventional ROM architecture. (b) The circuit and layout of a cell array in via-programming ROMs. The wordline (WL), ground line (VSS), bitlines (BL) and bit cells are implemented by poly, diffusion (OD), contact (CO), via and metals.

capacitance on the drain side of the transistor is connected to its bitline. However, the parasitic capacitance on the drain side of the transistor in a 1-cell is isolated from its bitline.

Consequently, various code-patterns produce different capacitive loadings on a bitline. The bitline of a column whose bit cells are all 0-cells experiences the largest loading effect for contact/via-programming ROMs. The variation in parasitic capacitance on a bitline causes various amounts of voltage-swings on a bitline when a 0-cell is accessed.

### *B. Crosstalk-Induced Read Failure (CIRF)*

Failure to sense 1-cells is one of the major consequences when crosstalk between bitlines occurs. In conventional synchronous ROM design, all bitlines are precharged (in precharge phase) to a targeted voltage prior to the data-sensing phase of a cycle [14], [18]. In the data-sensing phase, a bitline is discharged to develop a voltage drop for reading a 0-cell or remains at the precharged voltage $(V_{\rm PRE})$ for reading a 1-cell. A reference voltage, $V_{\rm REF}$, is chosen between the $V_{\rm PRE}$ and the developed voltage drops (by 0-cells) on bitlines to differentiate between a 0-cell and a 1-cell for a sense amplifier in the data-sensing phase. The fixed-value (FV) and the half-rate bitline-tracking (HRBLT) schemes are the two most popular schemes for providing $V_{\rm REF}$ in ROMs. The FV scheme [18] provides a fixed voltage difference between $V_{\rm REF}$ and $V_{\rm PRE}$ during the entire data-sensing phase. The HRBLT scheme adopts the bitline tracking technique [11]–[14] to provide a dynamic voltage difference between $V_{\rm REF}$ and $V_{\rm PRE}$ during the data-sensing phase. The difference between $V_{\rm REF}$ and $V_{\rm PRE}$ provided by HRBLT is half of the voltage swing of a regular BL (with maximum loading) across various wordline pulse widths. Therefore, the HRBLT scheme can provide the same $V_{\rm REF}$ across various ROM configurations (rows and columns) and is widely adopted in ROM compilers/generators. Examples of bitline behavior in reading both 1-cell (BL-1) and 0-cell (BL-0) in 256 Kb ROMs using FV and HRBLT schemes for $V_{\rm REF}$ are illustrated in Fig. 2(a) and (b), respectively. The wordline to bitline coupling effect and the weak bitline pull-up transistor (for leakage compensation) are also included in this simulation. A significant coupled voltage drop, $V_X$, on a selected bitline reading a 1-cell causes sensing failure for ROMs. Fig. 2(c) and (d) depict the simulation waveform of bitlines (BL-1V) reading 1-cells with crosstalk effect using FV and HRBLT schemes for $V_{\rm REF}$, respectively. The simulations in this paper are based on 0.18 $\mu$m standard logic process with supply voltage (VDD) of 1.8 V. The $V_{\rm PRE}$ is equal to VDD in this work. The coupled (crosstalk) voltage noise on BL-1V results in the voltage of BL-1V being smaller than $V_{\rm REF}$. Then 0-cell is detected by a sense amplifier rather than the expected 1-cell for BL-1V. If a coupled voltage drop on a bitline is smaller than $(V_{\rm PRE}-V_{\rm REF})$, the sense amplifier (ideal one, with zero input offset) senses the correct data (datum 1 or 1-cell). On the other hand, the bitline without any crosstalk, BL-1, still retains the $V_{\rm PRE}$ during the data-sensing phase and always has the correct sensing result.

In conventional ROM designs, all bit cells on the same row are activated by a wordline while only those bit cells on the selected bitlines will be readout. The input address and multiplexing scheme in the column direction of a ROM determines

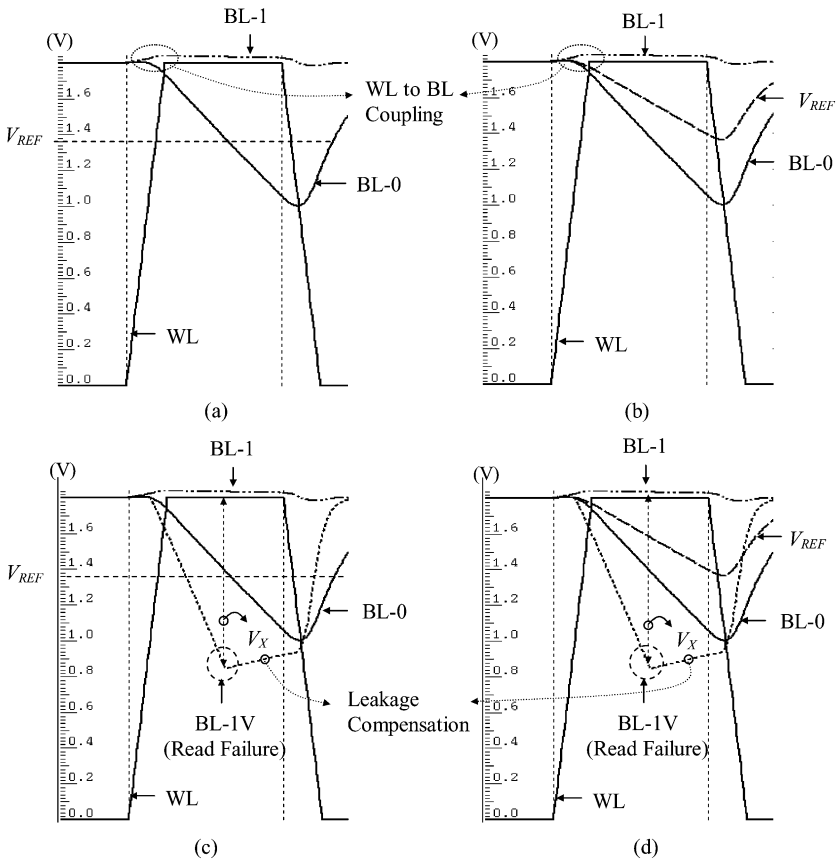


Fig. 2. Simulation waveforms of bitlines (512 cells) without crosstalk using (a) FV and (b) HRBLT schemes for $V_{\rm REF}$ (1.8 V). The waveforms of bitlines with crosstalk using (c) FV and (d) HRBLT schemes for $V_{\rm REF}$.

which bitlines are selected in an access cycle. Namely, there are voltage swings on both the selected (selected reading) and unselected bitlines (unselected reading) that access 0-cells during the data-sensing phase. Fig. 3 depicts a simplified bitline structure with coupling capacitances $(C_C)$, lumped bitline loading $(C_{\rm BL})$, and column-multiplexing circuit for one output-bit. The unselected bitlines ${\rm BL}[n-1]$ and ${\rm BL}[n+1]$, which are the neighboring bitlines of ${\rm BL}[n]$, have voltage drop developed by 0-cells when ${\rm WL}[m]$ is on. Voltage swings on ${\rm BL}[n-1]$ and ${\rm BL}[n+1]$ generate coupling noise through $C_C[n-1]$ and $C_C[n]$ onto the selected bitlines, ${\rm BL}[n]$. Accordingly, the neighboring bitlines are the aggressors and the selected bitlines are the victims under crosstalk effects.

Coupling capacitance between bitlines, intrinsic bitline loading and the amplitude of coupling voltage source are the key parameters affecting the amount of crosstalk among bitlines. Unfortunately, the coupling capacitance between minimum-spaced metal lines increases as manufacturing technology scales down. The trend of coupling capacitance limits the advantage of connecting more bit cells on a column (bitline) for advanced manufacturing technology.

Various code-patterns on a bitline lead to various voltage swings on bitlines while reading a 0-cell. For a given wordline pulsewidth $(T_{\rm WL})$ and cell current $(I_{\rm CELL})$ of an activated 0-cell, the variation of intrinsic bitline loading, a product of various code-patterns, causes various bitline discharge rates and voltage drops on bitlines. These voltage drops range from a full swing of the supply voltage for a bitline with minimum

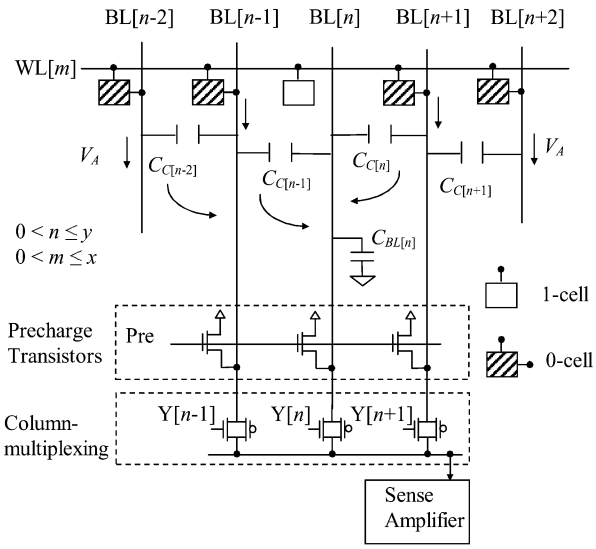


Fig. 3. A simplified structure of bitlines and column-multiplexing circuit in ROMs.

loading, to a few hundred millivolts for a bitline with maximum loading, as shown in Fig. 4. These various voltage drops on unselected bitlines, referred to as aggressor voltage $(V_A)$ and derived in (1), generate various amounts of coupled noise on their neighboring bitlines:

$$V_{A[n]} = \frac{I_{\rm CELL} \times T_{\rm WL}}{C_{{\rm BL}[n]} + C_{C[n-1]} + C_{C[n]}} + V_{X[n]}. \qquad (1)$$

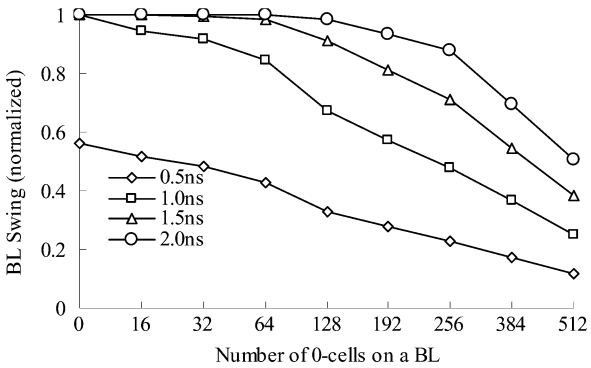


Fig. 4. Simulated bitline swing (normalized to VDD) versus number of 0-cells on a bitline (BL).

Moreover, the chain effect increases the coupled voltage noise on victim bitlines. The crosstalk between bitlines not only causes coupled voltage drop on a bitline which reads a 1-cell, but also enlarges the voltage drop on a bitline which reads a 0-cell. If the voltage drops on the $\mathrm{BL}[n-1]$ or $\mathrm{BL}[n+1]$ are enlarged by $\mathrm{BL}[n-2]$ or $\mathrm{BL}[n+2]$, the coupled voltage drop on the victim bitline $(\mathrm{BL}[n])$ is also increased, i.e., $\mathrm{BL}[n]$ is affected by the increased aggressor voltage. Hence, the chain effect amplifies the crosstalk.

Furthermore, the crosstalk between bitlines is also dependent on the intrinsic loading of the victim bitlines. The coupled voltage on a victim bitline is derived in (2). Unlike the signal lines with driver, the crosstalk effect in (2) does not include the ratio of driver strength as in [19] because the concerned victim bitline is floating (or tied to $V_{\mathrm{REF}}$ with high impedance) when reading a 1-cell. Fig. 5 depicts cases that do not yet include the chain effect. Under such straightforward situations, we can observe the crosstalk on victim bitlines with number of 0-cell on a bitline and aggressor voltage. For a given coupling capacitance and aggressor voltage, the crosstalk on victim bitlines with smaller intrinsic bitline loading (lesser number is larger than that with higher number of loading):

$$V_{X[n]} = V_{A[n-1]} \times \frac{C_{C[n-1]}}{C_{\mathrm{BL}[n]} + C_{C[n-1]} + C_{C[n]}} + V_{A[n+1]} \times \frac{C_{C[n]}}{C_{\mathrm{BL}[n]} + C_{C[n-1]} + C_{C[n]}}. \quad (2)$$

Therefore, a bitline suffers large coupled voltage noise when its intrinsic loading is small and its neighboring bitlines incur large voltage drop. From the point of view in code-patterns, an accessed 1-cell encounters large amount of coupled voltage noise under two conditions: 1) the bitline itself has few 0-cells and 2) both of its neighboring cells (on the same row) are 0-cells whose bitlines have small loading (few 0-cells). When considering the chain effect, increasing the number of consecutive 0-cells next to the accessed 1-cell on the same row, heightens the crosstalk effect.

## III. Dynamic Virtual Guardian Techniques

Since the coupling capacitance and the variation of intrinsic loading on bitlines across various code-patterns are inevitable in contact/via-programming ROMs, restricting the voltage swing of aggressors can reduce the coupled voltage on selected bitlines (victims). Three dynamic virtual guardian techniques (DVG1, DVG2, and DVG3) are proposed for high-speed ROMs to reduce the crosstalk between bitlines and prevent the CIRF.

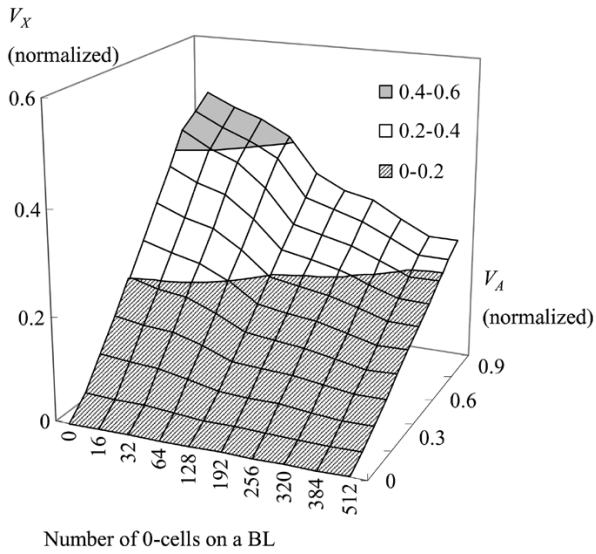


Fig. 5. Simulated coupled voltage $(V_X)$ versus number of 0-cells on a bitline and the aggressor voltage $(V_A)$. The $V_X$ and $V_A$ are normalized to VDD.

In both the DVG and conventional ROMs, bitlines are precharged to a target voltage before turning on a wordline. After the input address of each new cycle is decoded in the precharge phase, the selected bitlines are connected to sense amplifiers through the transistors controlled by column-selection signals, $\mathrm{Y}$. However, the behaviors of the data-sensing phase in DVG techniques are different from that of conventional ROMs.

### A. DVG1

In the first DVG technique (DVG1), the neighboring bitlines (both left and right sides) of selected bitlines are clamped to the precharged voltage $(V_{\mathrm{PRE}})$ during the data-sensing phase. These neighboring bitlines, clamped by the clamping transistors, act as the shielding or guardian for the selected bitlines and are dynamically specified according to the input address of each cycle. In conventional ROMs, the neighboring bitlines are not clamped and are in the unselected reading state. The clamping transistors in DVG1 are controlled by the column-select signals, $\mathrm{Y}$, as illustrated in Fig. 6(a). If $\mathrm{BL}[n]$ is selected, the column-select signal, $\mathrm{Y}[n]$, turns on the path for passing the signal value on $\mathrm{BL}[n]$ to a sense amplifier and enables the clamping mechanisms on $\mathrm{BL}[n-1]$ and $\mathrm{BL}[n+1]$. This clamping scheme results in a small voltage swing on those neighboring bitlines, $\mathrm{BL}[n-1]$ and $\mathrm{BL}[n+1]$, during the data-sensing phase, as shown in Fig. 6(b). However, the other unselected bitlines, such as $\mathrm{BL}[n-3]$ and $\mathrm{BL}[n+3]$, still have large voltage swings (unselected reading) as in conventional ROMs if 0-cells are activated during the data-sensing phase. This clamping behavior reduces the coupling noise source on the neighboring bitlines. Thus, DVG1 suppresses the coupled voltage drop on selected bitlines and prevents the CIRF. However, the inserted clamping

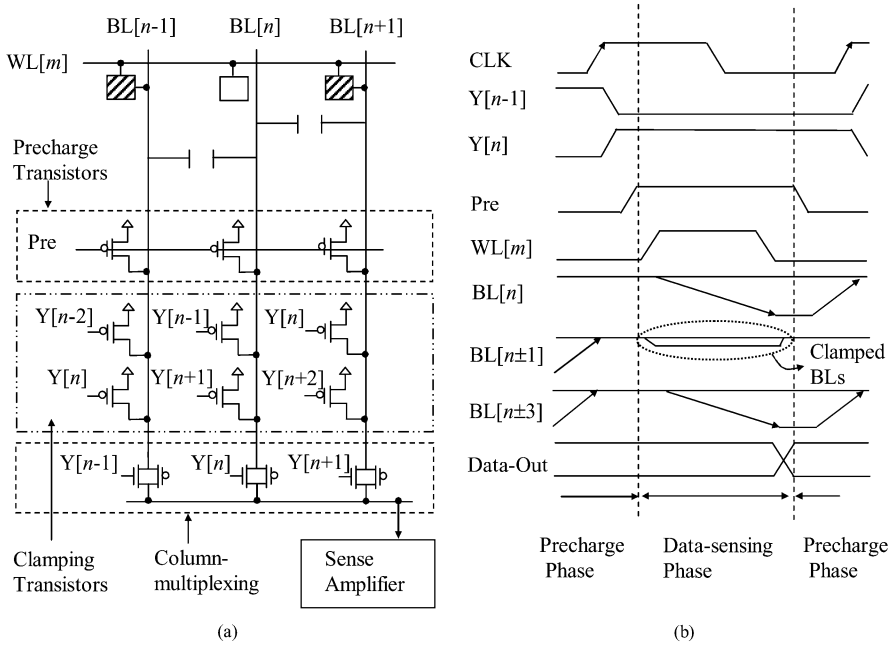


Fig. 6. (a) Circuit and (b) waveform of the DVG1.

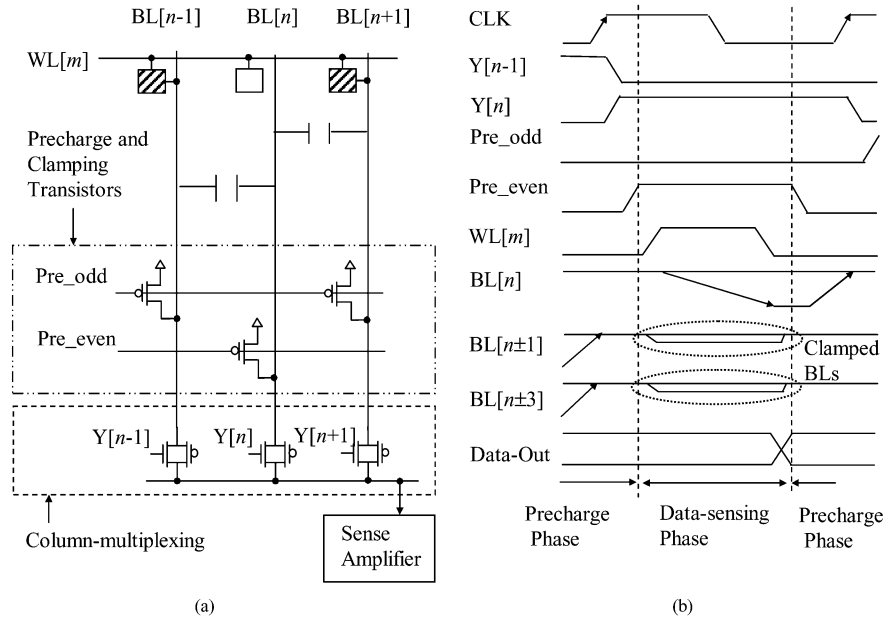


Fig. 7. (a) Circuit and (b) waveform of DVG2.

transistors in DVG1 take up more space than those in conventional ROMs.

### *B. DVG2*

Another DVG technique, DVG2, is proposed to reduce the area overhead while providing the same clamping capability as in DVG1. In DVG2, the clamping transistors are shared by the precharge transistors, as illustrated in Fig. 7(a). Half of the bitlines are clamped during the data-sensing phase rather than only two bitlines per output-bit as in DVG1. When one of the even bitlines is selected, the odd bitlines are clamped. Therefore, unlike in DVG1, in DVG2 the $\mathrm{BL}[n-3]$ and $\mathrm{BL}[n+3]$ are also clamped, as depicted in Fig. 7(b). The control signals for precharging and clamping are encoded with the least significant bit of the column addresses to control the odd and even bitlines separately. Consequently, the clamping circuit has no area overhead in column-multiplexing circuit, and the control block has only 2.3% area overhead for odd/even precharge signals (Pre_odd and Pre_even).

Fig. 8 shows the simulated voltage drops ($V_A$ and $V_X$) versus the transistor size of the clamping transistor with $T_{\mathrm{WL}} = 1$ ns and 512 bit cells on a bitline. The voltage drops are compared to $V_{\mathrm{PRE}}$. The wordline to bitline coupling effect and the bitline-leakage compensation transistor, which both help to pull-up the bitlines and result in suppressing the $V_A$ and $V_X$, are included in this simulation. As the width of a clamping transistor increases,

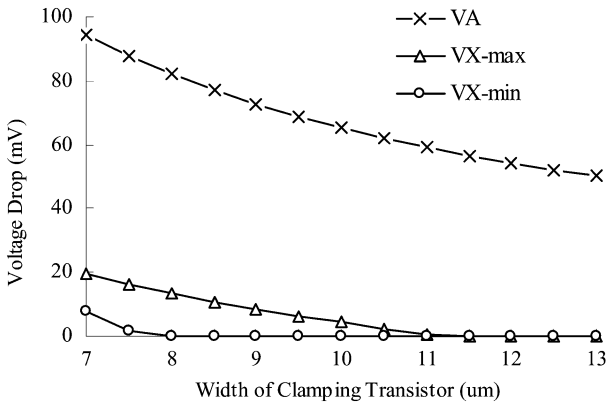


Fig. 8. Simulated voltage drops on an aggressor ($V_A$) and a victim ($V_X$) versus the transistor width of the clamping transistors in DVG1 and DVG2 ROMs.

the $V_A$ decreases and the $V_X$ is suppressed. Therefore, the $V_X$ can be reduced to zero if the width of clamping transistor is larger than 11 $\mu$m for a 256 Kb ROM in our designs.

### C. DVG3

The other DVG technique, DVG3, is proposed for asynchronous and low-power applications, in contrast to DVG1 and DVG2 which are designed for high-speed synchronous applications. Moreover, the DVG3 can reduce effects of residual voltage on bitlines better than some commonly adapted schemes for low-power ROMs.

In low-power ROMs, the selective precharge (SP) scheme [6]–[9], [20], which only precharges the selected bitlines, is a popular approach to reduce the consumption of current during the prechage phase at the expense of longer access time. However, any residual voltage from the previous cycle on the neighboring bitlines reading 0-cells generates a coupled voltage drop on the selected bitlines for the current cycle. The residual voltage can be as large as $V_{\rm PRE}$ if a neighboring bitline of current cycles is selected and reads a 1-cell at previous cycle. The residual voltage is small if the voltage swing is large (0-cells are read on a less-loaded BL) for the neighboring bitlines in the previous cycle. Hence, the ROMs using the conventional SP approach still suffer the CIRF. An additional timing phase, resetting all the bitlines to ground (GND) after data-sensing phase, can eliminate the residual voltage in the SP approach at the expense of a timing penalty in the cycle time [1], [6], [21].

The DVG3 can remove the residue voltage of SP ROMs without the timing penalty on resetting the bitlines. The neighboring bitlines in DVG3, as shown in Fig. 9, are discharged to the ground (the opposite state of the voltage for reading 1-cells) by the clamping transistors during the selective-precharge phase and are kept clamping at ground during the data-sensing phases. In the other words, the DVG3 cleans out the residual voltage on neighboring bitlines and precharge the selected bitlines at the same time (selected precharge phase). This precharge-discharge activity during selective precharge phase in DVG3 results in no requirement on additional timing phase for resetting the bitlines as in conventional SP scheme. Therefore, the neighboring bitlines in DVG3 have no voltage swing during the data-sensing phase. The DVG3 adopts the ground-shielding technique as in the shielded open bitline technique for NAND FLASH [6] but without additional bitline-resetting phase and changing the bitline structure of conventional one.

In summary, a bitline during the data-sensing phase in DVG techniques is in one of the three states: selected reading, unselected reading or clamped state (guardian). In the clamped state, the neighboring bitlines (or called guardian lines) of under-access bitlines are put into the crosstalk-suppression mode, i.e., virtually precharged/grounded. The guardian lines are dynamically assigned based on the input address and the multiplexing scheme in the column direction. To achieve fast access time, the neighboring bitlines in DVG1 and DVG2 are clamped at $V_{\rm PRE}$, same voltage for reading 1-cells, rather than clamped at ground as in DVG3.

## IV. Experimental Results

Two testchips with a 256 Kb conventional ROM macro and two 256 Kb DVG ROM macros (using DVG2 technique) were designed and fabricated using a 0.18 $\mu$m CMOS logic process, as shown in Fig. 10. The CIRF and design for manufacturing (DFM) capability of these fabricated ROM macros were measured and analyzed. Finally, the performance of DVG and conventional ROMs were compared.

Table I lists features of the experimental DVG and conventional (CNV) ROM macros. Two fabricated ROM macros (DVG2-FE and CNV-FE) employed the FV (noted with F) scheme to determine $V_{\rm REF}$, and had three adjustable $V_{\rm REF}$ values for crosstalk analysis, 1.45 V, 1.65 V, and 1.7 V. Since this work concentrates on the failure to read 1-cells, the $T_{\rm WL}$ values in DVG2-FE were set to experimental/relaxing (noted with E) timing, which was larger than typical timing, for ensuring sufficient sensing margin of reading 0-cells for three $V_{\rm REF}$ options. For fair comparison, the $T_{\rm WL}$ value and the key control signal timing in DVG2-FE and CNV-FE were the same. The DVG2-F ROM macro had typical timing in $T_{\rm WL}$ and higher $V_{\rm REF}$ options (1.7 V and 1.75 V) than DVG2-FE did to implement high-speed application. The number of fabricated samples of CNV-FE, DVG2-FE, and DVG2-F are 108, 216, and 108, respectively. Two conventional ROM macros with low $V_{\rm REF}$ value (0.82 V) in order to achieve full code-pattern coverage were included in this study with FV (CNV-F) and HRBLT (CNV-H) schemes. Parasitic resistance and capacitance were extracted from layout and were included in the simulations.

### A. Crosstalk Elimination

A realistic code-pattern, XT-pattern, was applied on the fabricated ROM macros to analyze the CIRF. The XT-pattern had ten sub-patterns: one for no-crosstalk (CP0) and nine for various degrees of crosstalk effect (CP1-9), including the worst case. For CP1-3, CP4-6, and CP7-9, three cases of bitline loading (number of 0-cells) on the neighboring bitlines (aggressors) were implemented to explore the minimum, typical and maximum $V_A$, respectively. The minimum, typical, and maximum values of $C_{\rm BL}$ on the victim bitlines (reading 1-cells) were implemented with three cases of number of 0-cells (i.e., 0, 256, and 511). In these nine code patterns, the victim bitlines

TABLE I
DESCRIPTIONS OF EXPERIMENTAL ROMS

| Structure | DVG2-F | DVG2-FE | CNV-FE | CNV-F | CNV-H |
|---|---|---|---|---|---|
| Full Code Coverage | Yes | Yes | No | Yes | Yes |
| Fabrication | Yes | Yes | Yes | No | No |
| $T_{WL}$[1] | T | E | E | T | T |
| $V_{REF}$ scheme | FV | FV | FV | FV | HRBLT |
| Standard $V_{REF}$ (V) | 1.7 | 1.65 | 1.65 | 0.82 | 0.82 |
| $V_{REF}$ (V) Options | 1.75 | 1.45 | 1.45 | No | No |
| | | 1.7 | 1.7 | | |

1. T stands for typical timing, E stands for experimental timing for all $V_{REF}$ options

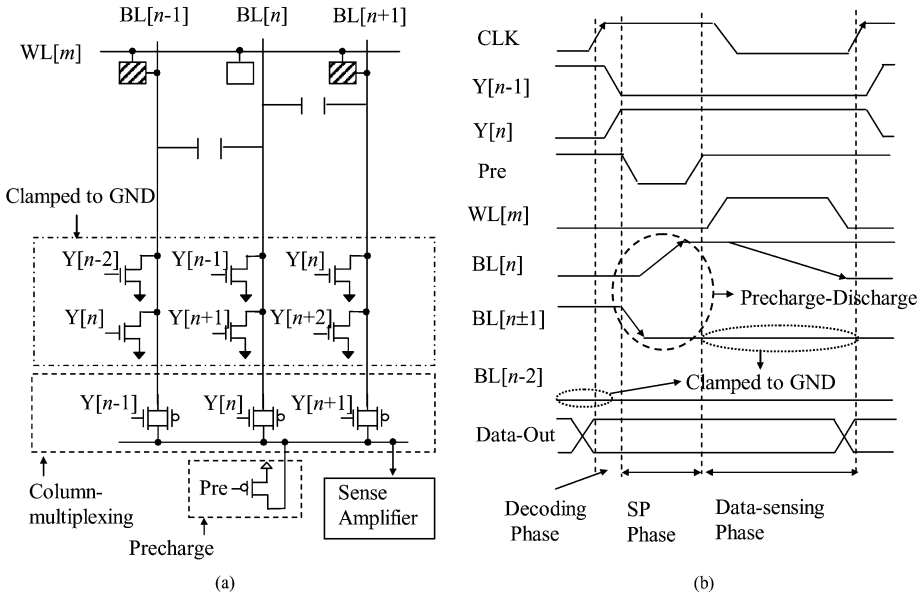


Fig. 9. (a) Circuit and (b) waveform of DVG3.

read 1-cells, and the aggressor bitlines read 0-cells. On the other hand, no crosstalk occurred at CP0 since all the cells on the aggressors are 1-cells; subsequently, no $V_A$ will be induced. Table II presents the measurement results of these ten sub-patterns for the fabricated 256 Kb conventional (CNV-FE) and DVG2-FE ROMs. The CNV-FE ROM with lowest voltage option of $V_{\rm REF}$ (1.45 V) failed the CP1, CP4, CP7, and CP8 patterns, while the CNV-FE with $V_{\rm REF} = 1.65$ V failed all the designed code-patterns except CP0 and CP3. The CNV-FE with $V_{\rm REF} = 1.7$ V only passed the CP0. Though the difference in terms of loading on the bitlines between CP0 and CP7 is negligible (one via/contact only), the CP0 did not have crosstalk effect but CP7 did. Thus, CNV-FE ROM passed the CP0 but failed the CP7. On the contrary, the DVG2-FE ROM, with three $V_{\rm REF}$ values, passed all the ten sub-patterns. These measurement results demonstrate that the DVG technique eliminated the CIRF successfully and provided room for a ROM to have a higher $V_{\rm REF}$ value or need smaller sensing margin of reading 1-cells compared with conventional ROMs.

The shmoo of the functional test with voltage sweep in operational voltage for I/O pads and the DVG2-F ROM macro is shown in Fig. 11. This DVG ROM operated down to a 0.95 V supply voltage correctly when the supply voltage for I/O pads of the testchip was also reduced. Since DVG2-F passed all the XT-pattern with both $V_{\rm REF}$ values, the DVG ROMs were func-

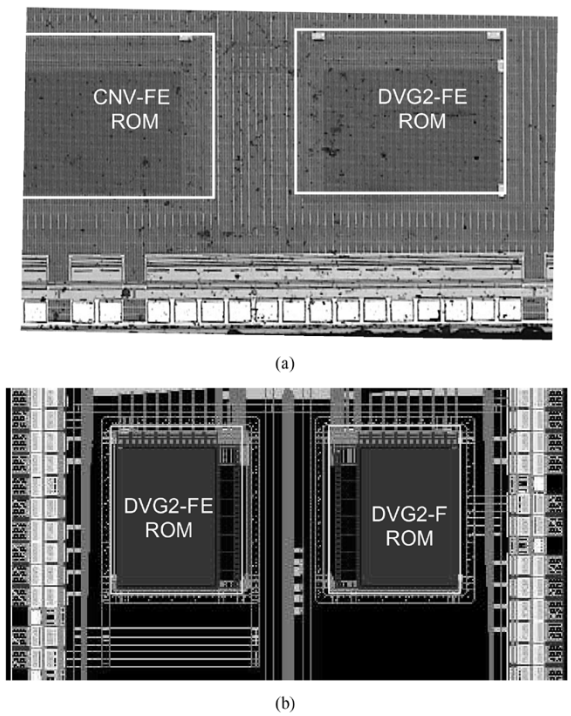


Fig. 10. (a) Die photo of a DVG2-FE and a conventional (CNV-FE) ROMs. (b) Layout photo of a DVG2-FE and a DVG2-F ROMs.

TABLE II
FUNCTIONAL TEST OF FABRICATED 256 Kb DVG AND CONVENTIONAL ROMS FOR CROSSTALK EFFECTS

| XT-Pattern | Number of 0-cells on a BL | | Conventional (CNV-FE) ROM | | | DVG2-FE ROM | | |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{REF}$ | | | $V_{REF}$ | | |
| | Aggressors | Victim | 1.45V | 1.65V | 1.7V | 1.45V | 1.65V | 1.7V |
| CP0 | 0 | 0 | Pass | Pass | Pass | Pass | Pass | Pass |
| CP1 | 512 | 0 | Fail | Fail | Fail | Pass | Pass | Pass |
| CP2 | 512 | 256 | Pass | Fail | Fail | Pass | Pass | Pass |
| CP3 | 512 | 511 | Pass | Pass | Fail | Pass | Pass | Pass |
| CP4 | 256 | 0 | Fail | Fail | Fail | Pass | Pass | Pass |
| CP5 | 256 | 256 | Pass | Fail | Fail | Pass | Pass | Pass |
| CP6 | 256 | 511 | Pass | Fail | Fail | Pass | Pass | Pass |
| CP7 | 1 | 0 | Fail | Fail | Fail | Pass | Pass | Pass |
| CP8 | 1 | 256 | Fail | Fail | Fail | Pass | Pass | Pass |
| CP9 | 1 | 511 | Pass | Fail | Fail | Pass | Pass | Pass |

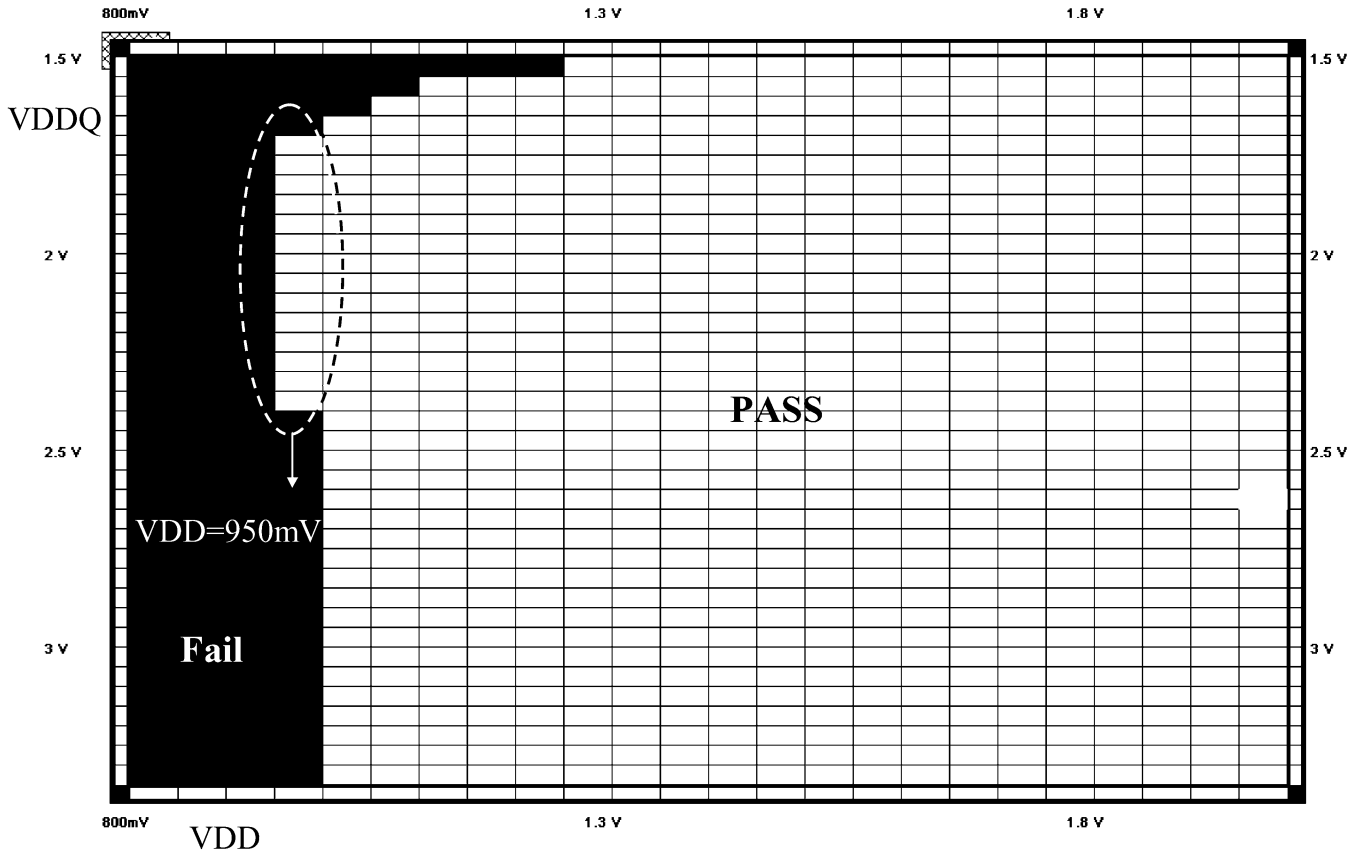


Fig. 11. Shmoo of functional test for various operational voltages of DVG2-F ROM (VDD) and I/O pads (VDDQ).

tional when the sensing margin of reading 1-cells is reduced to 50 mV ($V_{\rm REF} = 1.75$ V).

### *B. DFM Capability*

Process variations in the coupling capacitance between bitlines (metal lines) cause variation in crosstalk effect and functionality for conventional ROMs. This variation is commonly observed from lot-to-lot or fab-to-fab for the same process node of a foundry. Fig. 12 shows a simulated example of the sensing margin of reading 1-cells as a function of process variations in coupling capacitance. The variations (up to 30%) of coupling capacitance are normalized to the typical case specified by a foundry. The sensing margin of a bitline reading 1-cells without noise is 100 mV. This example adopts a bitline with 512 bit cells of which half are 0-cells. Three cases of aggressor voltage (normalized to VDD) are applied on conventional ROM. The employed $T_{\rm WL}$ is 1 ns. Large coupling capacitance between bitlines generates large $V_X$ values, and reduces the sensing margin of reading 1-cells in conventional ROMs. Accordingly, the sensing margin of reading 1-cells in conventional ROMs is sensitive to process variations in coupling capacitance. Since the implemented transistor size (transistor width is 12 $\mu$m) of clamping transistor in our designs is large enough to eliminate the $V_X$ regardless the variations of coupling capacitance, any variations in coupling capacitance due to manufacturing do not influence the sensing margin of reading 1-cells in DVG

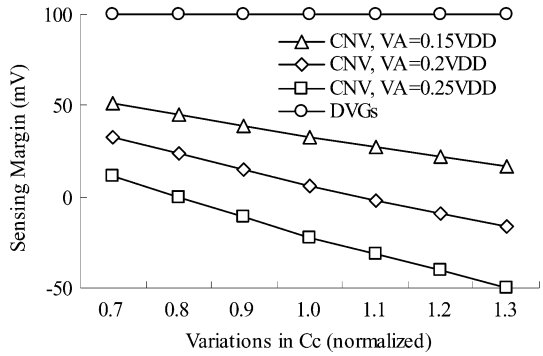


Fig. 12. Simulated sensing margin of reading 1-cells versus the process variations in coupling capacitance ($C_C$) for conventional (CNV) and DVG ROMs. The $C_C$ is normalized to typical process condition.

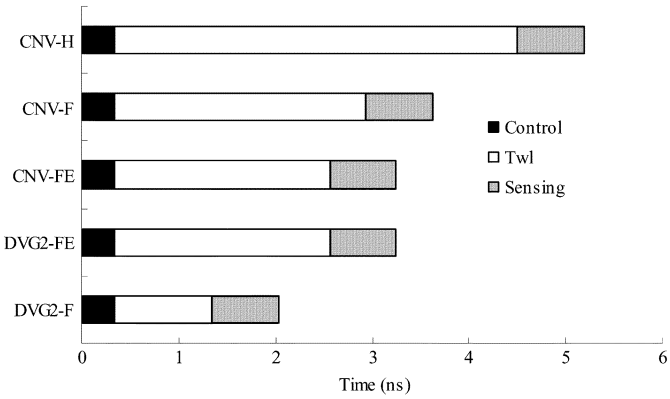


Fig. 13. Breakdown of access time for DVG ROMs (DVG2) and conventional (CNV) ROMs.

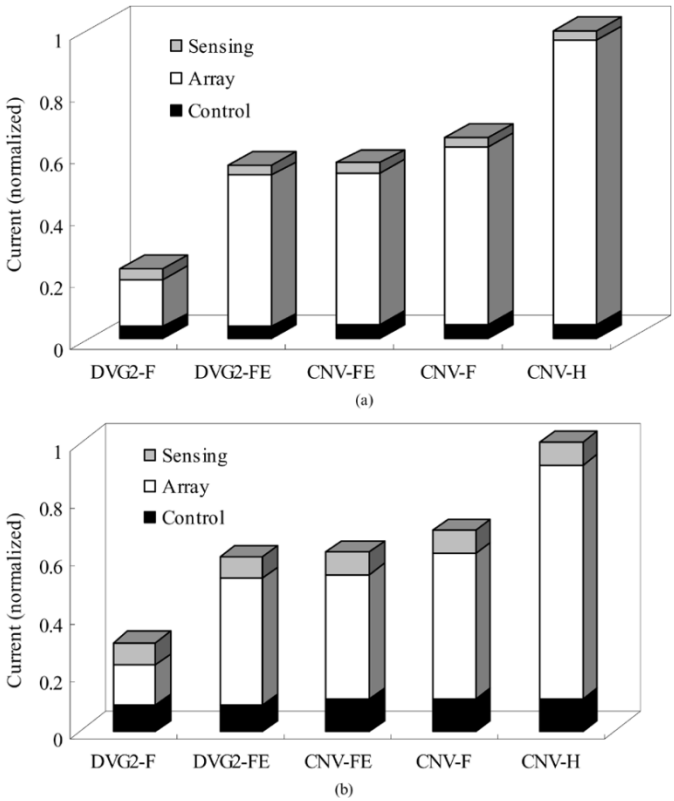


Fig. 14. Breakdown of current for 256 Kb DVG2 ROMs and conventional (CNV) ROMs with (a) W-pattern and (b) XT-pattern.

ROMs. Therefore, DVG techniques achieve larger tolerance for cross-fabs/cross-lots variations in manufacturing and have better DFM capability than conventional ROMs.

### C. Performance

In addition to full code-pattern coverage, the DVG ROMs achieved a smaller access time, higher operation frequency and lower power consumption than conventional ROMs.

For better coverage of applicable ROM code-patterns in conventional ROMs, small $V_{\rm REF}$ value can be employed to tolerate the crosstalk-induced voltage drop $(V_X)$ on victim bitlines. By applying a small reference voltage, say $(V_{\rm REF} - V_X)$, the minimum sensing margin for reading a 1-cell is maintained at $(V_{\rm PRE} - V_{\rm REF})$ for those victim bitlines, which had voltage values at $(V_{\rm PRE} - V_X)$ due to crosstalk effect. However, reducing the value of $V_{\rm REF}$ increases the required $T_{\rm WL}$ for a given sensing margin for reading 0-cells, particularly for large $V_X$ values. Hence, the coverage of applicable code-patterns for conventional ROMs can be increased by adjusting $V_{\rm REF}$ at the expense of longer access time and cycle time (e.g., CNV-F and CNV-H).

Since DVG techniques suppress the crosstalk-induced voltage drop on victim bitlines, the voltages on bitlines reading 1-cells during the data-sensing phase are retained close to $V_{\rm PRE}$ with high uniformity across code-patterns. The value of $V_{\rm REF}$ in DVG ROMs can be higher than those in conventional ROMs for a given minimum sensing margin value to read a 1-cell successfully. Hence, the $T_{\rm WL}$ in DVG ROMs can be smaller than that in conventional ROMs without degrading the sensing margin of reading 1-cells across code-patterns.

The timing breakdown of the simulated access time of two DVG ROMs (DVG2-FE and DVG2-F) and three conventional ROMs (CNV-FE, CNV-F, and CNV-H) is illustrated in Fig. 13. To obtain the same $V_{\rm REF}$ (0.82 V) for full coverage of code-patterns, CNV-F and CNV-H had different values for $T_{\rm WL}$. The $T_{\rm WL}$ and $V_{\rm REF}$ values of DVG2-F ROM were 1 ns and 1.7 V, respectively. The $T_{\rm WL}$ and $V_{\rm REF}$ values of DVG2-FE, CNV-FE were 2.2 ns and 1.45 V, respectively. The timing of decoding/control circuit (Control), data output circuit (Sensing) for DVG ROMs and referenced conventional ROMs were the same. Therefore, the speed improvement by DVG2-F compared to conventional ROMs derives solely from its smaller $T_{\rm WL}$. The access time of DVG2-F was only 55.9% and 39.1% of those of CNV-F and CNV-H, respectively. Further improvement in access time for DVG2-F can be achieved with smaller $T_{\rm WL}$ and sensing margin, which were verified by the functional test with $V_{\rm REF} = 1.75$ V.

Despite having faster access and cycle times, the DVG ROMs consumed less current than conventional ROMs did. Since the $T_{\rm WL}$ in the DVG ROM was smaller than that in the conventional ROMs, the voltage swings on bitlines for reading 0-cells in DVG ROMs are smaller, and the power consumptions of discharge-precharge activities on bitlines are significantly reduced in DVG

TABLE III
PERFORMANCE COMPARISON

| | DVG2-F | DVG2-FE | NHS-PD [9] | CRCS [10] | IBM [18] | HSCSS [21] |
|---|---|---|---|---|---|---|
| Tech Node (um) | 0.18 | 0.18 | 0.35 | 0.35 | 0.5[1] | 0.25[2] |
| Capacity (bits) | 256K | 256K | 16K | 128K | 144K | 32K |
| Aspect ratio (High/Width) | 1.21 | 1.21 | N.A. | 0.75 | 0.21 | 1.26 |
| Code Layer | Via | Via | Diffusion | Contact and Metal-1 | Diffusion | Via |
| VDD (V) | 1.8 | 1.8 | 3.3 | 3.3 | 2.5 | 1.0/1.7 |
| Access Time (ns) | 2.0 | 3.2 | 3.8 | 8.4 | 2.23 | 5.7/3[5] |
| Power[3] (mW) | 15.76[5] | 31.6[5] | 6.09[5] | 8.63 | 300 | 2.2/8[5] |
| PDP-bit[4] | 0.12 | 0.38 | 2.82 | 0.55 | 4.53 | 0.38/0.73 |

[1] Effective channel length is 0.2um
[2] Dual threshold voltages
[3] Measured at 100Mhz
[4] Power-Delay Product per bit (pico-Joule/bit)
[5] Silicon result
N.A. stands for not available

ROMs. Fig. 14 shows the simulated current breakdown of the five experimental ROM macros with the XT-pattern and the W-pattern. All bit cells are 0-cells in the W-pattern which has maximum power consumption across code-patterns. The current consumptions of DVG2-F with the W-pattern and XT-pattern are 22.5% and 30.6% of those of CNV-H, respectively. The simulated current consumptions of DVG2-F, DVG2-FE, and CNV-FE were confirmed within 3% of the mean value of the measurement result of fabricated samples.

The area overhead in DVG techniques is small. The DVG2 technique had negligible area penalty because no additional device was required in the precharge/clamping devices and column-multiplexing circuit of ROMs while only a few gates were required in the control circuit. However, DVG1 and DVG3 techniques have 3% area overhead for a 256 Kb ROM due to the clamping transistors for each bitline.

Table III compares the performance of DVG ROMs with previous reports. For a given memory configuration, the structure with large value in height (rows) had large power consumption and long access time. Thus, aspect ratios were also included in the comparison table. Since different works had various speed and power performance for various sizes of memory capacity, we adopt the power-delay product (PDP) per bit (PDP-bit) for fair comparison. The PDP-bit of DVG2-F, 0.12 pico-Joules per bit, was much smaller than those obtained in other reports. The DVG ROM clearly outperformed the others in terms of the power-delay product to memory capacity ratio.

## V. CONCLUSION

This work investigated the variation in crosstalk and read failure across various code-patterns of contact/via-programming ROMs. DVG techniques have been proposed to suppress the crosstalk between bitlines across code-patterns and manufacturing conditions. The fabricated samples using 0.18 $\mu$m CMOS technology demonstrated the effectiveness of the DVG technique for eradicating crosstalk-induced read failure with varied sensing margins. Moreover, evaluation of the 256 Kb DVG ROMs without additional sensing margin for tolerating coupling noise on victim bitlines showed significant reductions in access time and power consumption compared to 256 Kb conventional ROMs. Therefore, DVG ROMs achieved not only full coverage of applicable code-patterns but also high speed and low power capability.

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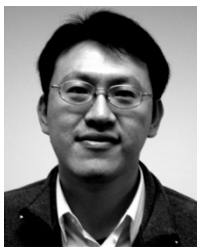

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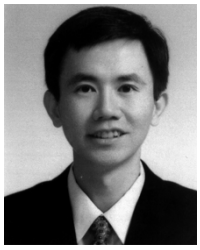

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