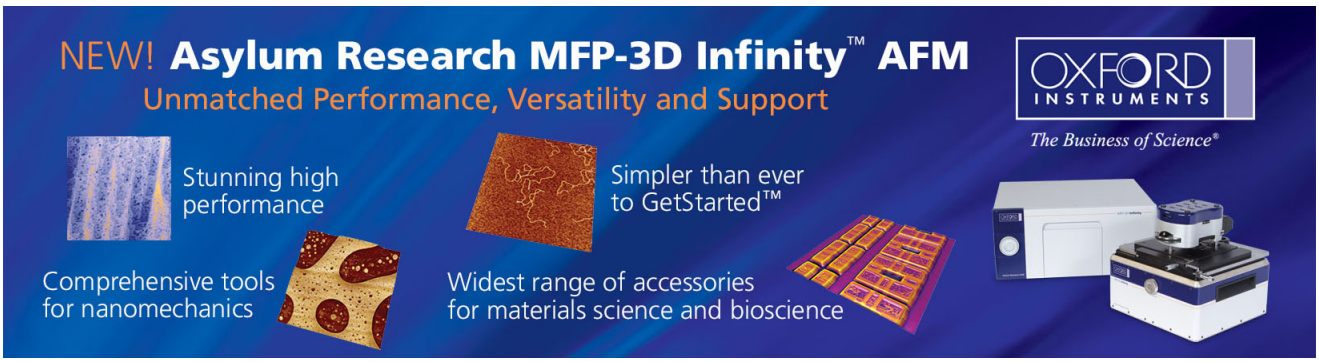
Infrared microscopy of hot spots induced by Joule heating in flip-chip SnAg solder joints under accelerated electromigration

S. H. Chiu, T. L. Shao, Chih Chen, D. J. Yao, and C. Y. Hsu

Citation: Applied Physics Letters **88**, 022110 (2006); doi: 10.1063/1.2151255
View online: http://dx.doi.org/10.1063/1.2151255
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/88/2?ver=pdfcov
Published by the AIP Publishing



Infrared microscopy of hot spots induced by Joule heating in flip-chip SnAg solder joints under accelerated electromigration

S. H. Chiu, T. L. Shao, and Chih Chen[a)]
National Chiao Tung University, Department of Material Science and Engineering, Hsin-chu 300, Taiwan, Republic of China

D. J. Yao
National Tsing Hua University, Institute of Microelectromechanical System, Hsin-chu 300, Taiwan, Republic of China

C. Y. Hsu
National Tsing Hua University, Department of Power Mechanical Engineering, Hsin-chu 300, Taiwan, Republic of China

(Received 23 May 2005; accepted 31 October 2005; published online 11 January 2006)

Joule heating effect in solder joints was investigated using thermal infrared microscopy and modeling in this study. With the increase of applied current, the temperature increased rapidly due to Joule heating. Furthermore, modeling results indicated that a hot spot existed in the solder near the entrance point of the Al trace, and it became more pronounced as the applied current increased. The temperature difference between the hot spot and the solder was as large as 9.4 °C when the solder joint was powered by 0.8 A. This hot spot may play an important role in the initial void formation during electromigration. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2151255]

Electromigration has emerged as another reliability issue for high-performance and high-density flip-chip solder joints,[1,2] and electromigration in solder joints has been studied in recent years.[3–7] The current crowding effect has been found to be responsible for the failure in the chip/anode side of the solder joint.[8,9] The current used for typical accelerated electromigration tests ranges from 0.5 A to 2.2 A. Although whether a hot spot exists at the current crowding region is of interest, only a few studies have addressed the Joule heating effect in solder joints.[10–12] However, there are still no experimental data to verify the temperature in the bump because the solder joints are completely surrounded by a chip, a substrate, and underfill; so no direct temperature measurement can be made to investigate the Joule heating effect inside the solder joints.

For this study, we used thermal infrared (IR) microscopy to measure the temperature distribution in the Al trace at various stressing conditions. Based on the experimental data, we constructed a finite element model to simulate the temperature distribution inside the solder bump during current stressing. Therefore, this study provides a deeper understanding of the Joule heating effect inside the flip-chip solder joints during current stressing.

The fabrication procedure for the SnAg bumps can be found in our previous publication.[8] The thickness of the Si chip was 300 μm. The under-bump metallization (UBM) consisted of 0.7 μm Cu, 0.3 μm Cr–Cu, and 0.1 μm Ti. It is assumed that a layer-type Cu_6Sn_5 intermetallic compound (IMC) of 1.4 μm thick grew in the interface of the UBM and the solder, whereas a layer-type Ni_3Sn_4 IMC of 1.0 μm thick formed in the interface of the pad metallization and the solder in the substrate side. The UBM and passivation openings were 120 μm and 85 μm in diameter, respectively. The Al trace on the chip side was 34 μm wide and 1.5 μm thick.

The temperature increase inside the bumps when powered by electric current was detected by thermal IR microscopy, that had resolution of 0.1 °C in temperature sensitivity and 2.8 μm in spatial resolution.

On the basis of the experimental results, a three-dimensional (3D) simulation was carried out by finite element analysis. Only two of the solder bumps had electrical current passing through. The electrical and thermal resistivities for the materials used in this modeling are listed in Table I. The effect of temperature coefficient of resistivity (TCR) was considered, and the TCR values for the metals are also listed in Table I. In addition, 3D coupled thermal-electric simulation was conducted to predict the steady-state temperature distribution using the ANSYS software package developed by ANSYS, Inc. The model used in this study was a SOLID69 eight-node hexahedral coupled field element. All the boundary conditions followed the experiment setup. The area

TABLE I. Thermal conductivities, electrical resistivities, and temperature coefficients of resistivity for the materials used in the simulation model.

Material	Thermal conductivity (W m °C)	Resistivity ($\mu\Omega$ cm) at 20 °C	TCR (10^{-3} K^{-1})
Silicon	147.00	···	···
Al trace	238.00	2.70	4.2
UBM(Ti+Cr/Cu+Cu)	147.61	5.83	4.9
SnAg3.5	33.00	12.3	4.6
Ni	76.00	6.8	6.8
Cu pad	403.00	1.7	4.3
BT (substrate)	0.70	···	···
Underfill	0.55	···	···
Passivation	0.34	···	···

Note: The materials not given in electric resistivity are assumed to be electrical insulators.

[a)]Author to whom correspondence should be addressed; electronic mail: chih@cc.nctu.edu.tw

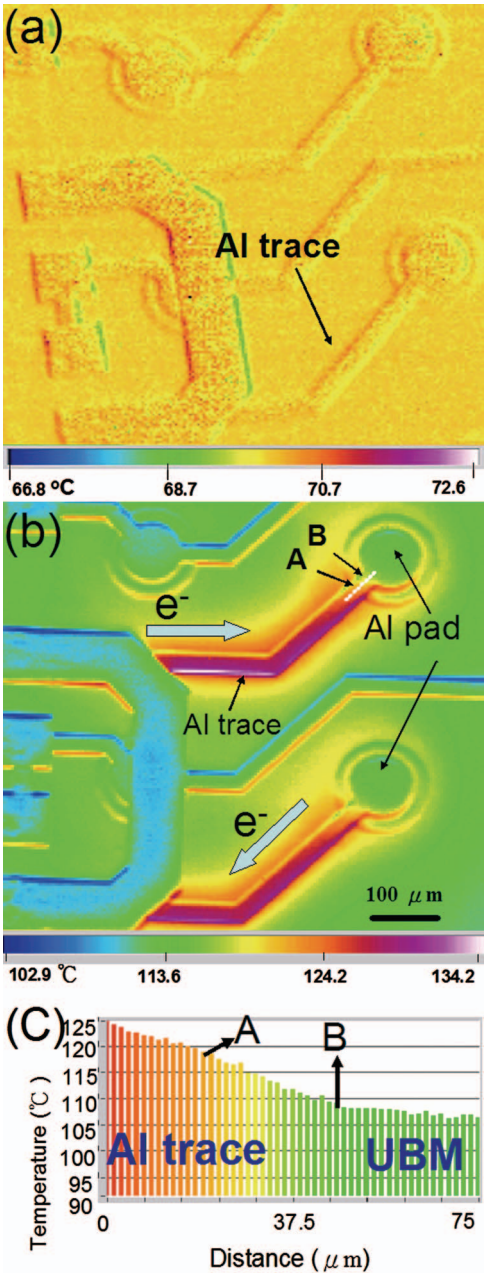


FIG. 1. (Color) (a) Temperature distribution in the package before current stressing, showing a uniform temperature in the package; (b) Temperature distribution in the Al trace measured by the IR microscope when powered by 0.59 A; (c) Temperature profile along the white line in (b).

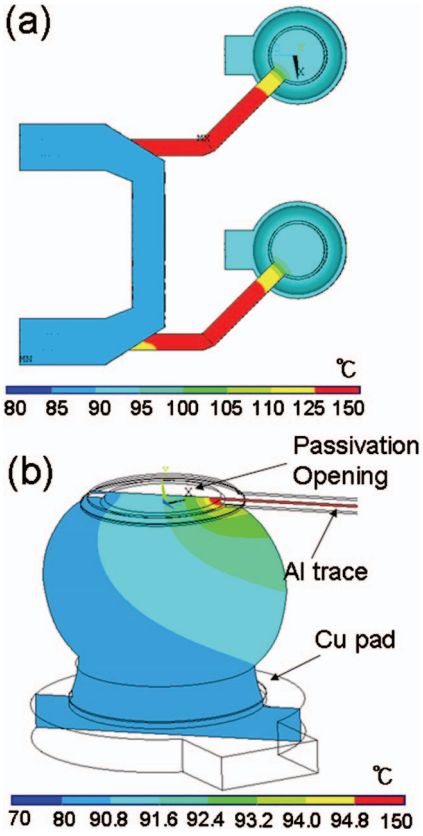


FIG. 2. (Color) (a) Simulated temperature distribution in the stressing circuit when powered by 0.59 A. (b) Temperature distribution inside the solder for one of the cross sections near the Al trace. A hot spot was found in the entrance point of the Al traces.

of the Si chip was 10.0 mm×6.0 mm and the thickness was 290 μm, whereas the bismaleimide triazine (BT) substrate was 4.75 mm wide, 7 mm long, and 350 μm thick.

Before the current stressing, calibration was performed on a hot plate maintained at 70 °C. The temperature distribution without current stressing is shown in Fig. 1(a). The circuit of the Al trace can barely be seen since the Si substrate is transparent to IR radiation. Figure 1(b) shows the temperature increase for the Al trace in the package when stressed by 0.59 A at the ambient temperature of 70 °C. The current path is indicated by two of the arrows in the figure. There were two solder bumps located directly below the two circular Al pads/UBMs, as labeled in the figure. It is noteworthy that the Al trace has much higher temperature than the circular Al pads, which were directly connected to the UBM and the solder bumps. The maximum temperature was as high as 134 °C, which occurred approximately at the middle of the Al trace, whereas the temperature was only about 105 °C for the Al pads above the solder bumps. The inner circle of the Al pad in Fig. 1(b) represents the passivation opening, whereas the outer circle corresponds to the UBM opening of the solder joint.

Furthermore, whether a hot spot exists inside the solder is of interest for electromigration study. Figure 1(c) illustrates the temperature profile along the 75 μm long dashed line in Fig. 1(b). The points A and B in Fig. 1(b) represent the edges of the UBM and the passivation openings, respectively. The temperatures at points A and B were approximately 118.2 °C and 109.7 °C, respectively, which are much higher than the average temperature of 105.2 °C in the Al pad. The average temperature was calculated by averaging the temperatures in a 10 μm×10 μm square in the center of the passivation opening. In addition, there is a thermal gradient since the temperature at the Al pad near the entrance of the Al trace was higher than that at the opposite end. The gradient in this junction was as high as 1700 °C/cm.

Figure 2(a) shows the simulated temperature distribution in the Al trace and in the solder joints when stressed by 0.59 A. The simulation results fit the experimental results very well. The temperature distribution inside the solder in one of the cross sections near the entrance of the Al trace is shown in Fig. 2(b). A hot spot existed in the solder adjacent to the entrance points of the Al trace into the solder at the passivation opening. The temperature at the spot was 95.6 °C, which was 4.5 °C higher than the average value in the solder. The temperature on the chip side was higher than

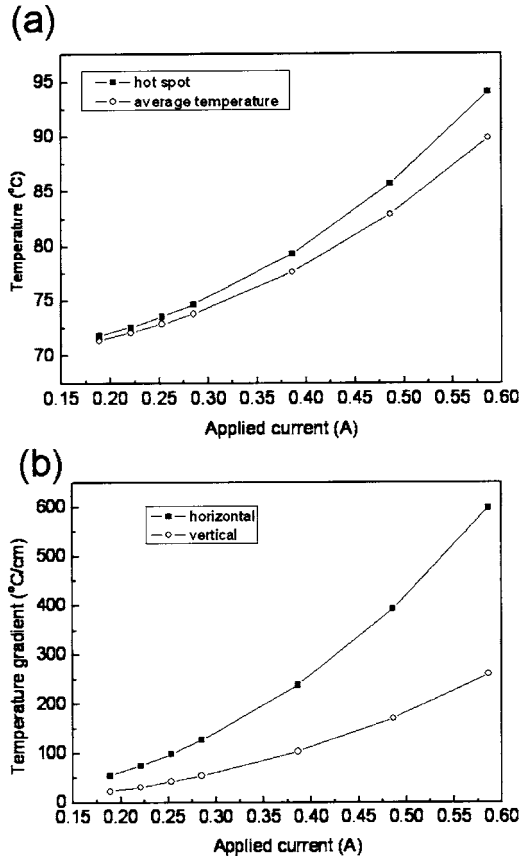


FIG. 3. (a) Simulated temperature in the solder joint and in the hot spot as a function of applied current up to 0.8 A. (b) Vertical and horizontal thermal gradients in the solder bumps as a function of applied current up to 0.8 A.

that on the substrate side. In addition, the vertical thermal gradient was measured to be 276 °C/cm, whereas the horizontal thermal gradient was calculated to be 634 °C/cm at this stressing condition. The thermal gradient is denoted in this letter as the subtraction of the temperature in the hot spot by the temperature at the opposite end of the solder, then divided by the distance between the two locations. Under this stressing condition, the current density in the Al trace was 1.1×10^6 A/cm^2. The average current density in the joint was 5.2×10^3 A/cm^2 based on the UBM opening. In the hot spot, the maximum current density was 1.7×10^5 A/cm^2, whereas the average current density involved in a volume of 5 μm$\times$5 μm$\times$5 μm was estimated to be 1.4×10^5 A/cm^2.

The Joule heating effect was also inspected at various applied currents. Figure 3(a) depicts the temperature in the hot spot and the average temperature in the solder as a function of applied current up to 0.8 A. Both of them increased rapidly with the increase of applied current. The difference in these two temperatures increases as the applied current increases, and it may be as high as 9.4 °C when stressed by 0.8 A. Figure 3(b) shows the vertical and horizontal thermal gradients as functions of the applied current. They also increase with the increase in stressing current. Moreover, the horizontal thermal gradient rose more quickly than the vertical one, reaching 1320 °C/cm under the stressing of 0.8 A.

The existence of the hot spot may be attributed to two reasons. First, it may be due to the local Joule heating inside the solder itself. The heating power can be expressed as

$$P = I^2R = j^2\rho V,$$

where P is Joule heating power, I is the current, R is the resistance, j is the local current density, V is the volume of the material, and ρ is the resistivity. The product of I^2R is the total heating power, whereas $j^2\rho$ is the heating power per unit volume. In our simulation model, the total resistance of the Al trace was about 900 mΩ, and the resistance of the solder bump was about 10 mΩ. Therefore, the Al trace generated most of the heat. Due to the serious current crowding in the solder joint, the current density in the vicinity of the Al entrance into the solder joint is typically one to two orders higher than the average value,[7,8] causing local Joule heating there. Second, the Al trace has higher Joule heating effect, and the hot spot was close to the Al trace. At lower stressing current, the hot spot is not obvious because there is less heat generation. However, it became more pronounced as the applied current increased due to large heat generation and difficulty in heat dissipation. The solder in the hot spot was the most vulnerable part in the solder joint during electromigration testing, since it may experience much larger electron wind force due to the higher current density and the higher diffusivity owing to the higher temperature as well as its low melting point. Hence, voids start to form at this spot.[8]

In summary, the Joule heating effect in the solder joints has been experimentally investigated using an IR microscope and a 3D coupled thermal-electrical simulation. The temperature distribution in joints can be determined thoroughly. A hot spot was found in the vicinity of the entrance point of the Al trace, which is detrimental to the electromigration lifetime of the solder joints.

The authors would like to thank Dr. Everett C. C. Yeh for helpful discussions and the National Science Council of R. O. C. for financial support through Grant No. 92-2216-E-009-008. In addition, assistance with the simulation facility from the National Center for High-Performance Computing (NCHC) in Taiwan is highly appreciated.

[1] K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[2] *International Technology Roadmap for Semiconductors*, Assembly and Packaging Section, Semiconductor Industry Association, San Jose, CA (2003), pp 4–9.
[3] S. Brandenburg and S. Yeh, in *Proceedings of Surface Mount International Conference and Exhibition*, San Jose, CA, 23–27 August 1998 (SMTA, Edina, MN, 1998), p. 337.
[4] C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
[5] W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. **94**, 5665 (2003).
[6] T. Y. Lee, K. N. Tu, and D. R. Frear, J. Appl. Phys. **90**, 4502 (2001).
[7] Everett C. C. Yeh, W. J. Choi, and K. N. Tu, Appl. Phys. Lett. **80**, 4 (2002).
[8] T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen, J. Appl. Phys. **96**, 4518 (2004).
[9] J. W. Nah, K. W. Paik, J. O. Suh, and K. N. Tu, J. Appl. Phys. **94**, 7560 (2003).
[10] T. Y. T. Lee, T. Y. Lee, and K. N. Tu, in *Proceedings of the 51st Electronic Components and Technology Conference* (IEEE Components, Packaging, and Manufacturing Technology Society, Orlando, FL, 2001), p. 558.
[11] H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. **82**, 7 (2003).
[12] T. L. Shao, S. H. Chiu, C. Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. **33**, 1350 (2004).