Characterization of Programmed Charge Lateral Distribution in a Two-Bit Storage Nitride Flash Memory Cell by Using a Charge-Pumping Technique

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***Abstract*—In this paper, we use a modified charge pumping technique to characterize the programmed charge lateral distribution in a hot electron program/hot hole erase, two-bit storage nitride Flash memory cell. The stored charge distribution of each bit over the source/drain junctions can be profiled separately. Our result shows that the second programmed bit has a broader stored charge distribution than the first programmed bit. The reason is that a large channel field exists under the first programmed bit during the second bit programming. Such a large field accelerates channel electrons and causes earlier electron injection into the nitride. In addition, we find that programmed charges spread further into the channel as program/erase cycle number increases.**

***Index Terms*—Charge pumping (CP), cycling stress, programmed charge distribution, two-bit storage nitride Flash cell.**

I. Introduction

NITRIDE-BASED trapping storage Flash memory has received much interest recently for its smaller bit size, simpler manufacturing process, and no drain-induced turnon [1], [2]. In a conventional SONOS cell, programmed charges are stored uniformly in a nitride layer. This SONOS concept has recently evolved into a localized trapping and two-bit storage cell, such as NROM [3] and Nbit [4] technologies. These special-type nitride Flash cells resemble a standard MOS transistor except that the gate oxide is replaced by an oxide-nitride-oxide gate dielectric stack. Two bits operation can be achieved by placing programmed charges in the nitride layer locally above the source or the drain junction by channel hot electron program and band-to-band hot hole erase. A reverse read scheme is employed to maximize the effect of the stored charge on the threshold voltage window [3]. Because of a symmetrical cell structure and a nonconductive storage element, the Nbit technology has been engineered to take advantage of a higher packing density memory array without compromising device endurance, performance and reliability.

In two-bit operation, the control of programmed charge lateral distribution of each bit is a major concern for the scalability of this memory cell. The stored electrons at the first bit will affect the threshold voltage of the second bit in reverse read and vice versa. This phenomenon is referred to as the second bit effect [5] and is closely related to programmed charge lateral spread. Furthermore, the lateral spread of stored charges in nitride will result in the degradation of erase capability or erase speed due to a spatial mismatch between stored electrons and injected holes during erase [6]. For these reasons, comprehensive understanding of programmed charge spatial distribution is

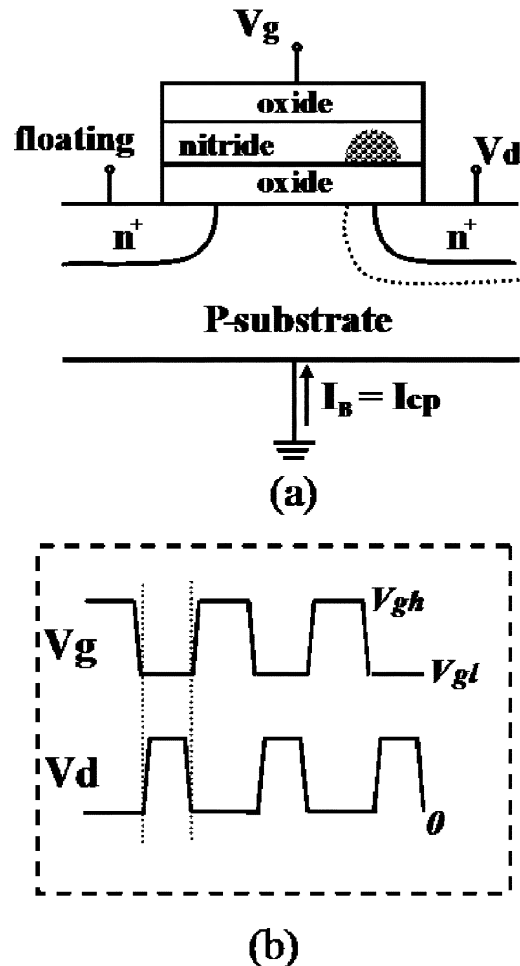

Fig. 1. (a) Schematic diagram of a two-bit storage nitride Flash cell and (b) CP measurement waveform. The dashed line in the substrate represents the depletion region caused by V_d. The thickness of the ONO gate stack is 9 (top oxide), 6, and 6 nm, respectively.

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of vital importance in the optimization of the cell structure and operation bias.

Attempts have been made in the past to characterize the trapped charge distribution in a NROM cell [7], [8]. Larcher *et al.* used an inverse modeling approach to extract programmed charge distribution from measured current–voltage (I–V) characteristics [7]. This method, however, suffers from some drawbacks, such as lack of precise information on device doping profile and extensive numerical calculation to reach a consistent solution between stored charge distribution and measurement result.

In this paper, we will use a modified charge-pumping (CP) technique [9] to probe the lateral distribution of programmed charges at the source and drain junctions separately without using computer simulation. The devices and measurement setup throughout this study will be described in Section II. The CP current for single bit storage and two-bit storage will be shown in Section III. Program/erase cycling stress effect on stored charge distribution will be also examined.

II. Experimental

The nitride Flash cells used in this paper have a gate length of 0.5 μm and a gate width of 1.0 μm. The thickness of each ONO layer is 9 nm (top oxide), 6 nm (nitride) and 6 nm (bottom oxide). The cell intrinsic threshold voltage (V_t) is about 1.6 V where V_t is defined as the gate voltage when the drain current is 1 μA at a reverse read voltage of 1.6 V. Channel hot electron program and band-to-band hot hole erase accompanied by a reverse read scheme are adopted to achieve two-bit per cell operation.

In CP measurement, the voltage waveforms at gate and drain terminals supplied by a two-channel pulse generator are illustrated in Fig. 1. The employment of a dual-channel pulse generator can circumvent the misalignment of gate and drain signal. The gate pulse has a fixed high level ($V_{\rm gh}$) and a variable low level ($V_{\rm gl}$). The $V_{\rm gh}$ is sufficiently high ($V_{\rm gh} = 6$ V here) to ensure that the entire channel at program state is inverted.

The CP current, named hereafter $I_{\rm cp}$, is measured at the substrate. To probe the lateral extent of programmed charge in the drain side (or the source side), V_d (or V_s) is adjusted to modulate the drain (or source) depletion width while V_s (or V_d) is left floating. In this way, there is no channel current and thus no impact ionization induced substrate current in CP measurement. Besides, the V_d is 180° phase-shifted with respect to V_g so that the drain signal is applied only during the interface-trap ($N_{\rm it}$) electron emptying period. Because the length of the channel hot electron injection region (i.e., programmed region) is only about a few nanometers [9], $I_{\rm cp}$ contributed by interface traps in the programmed region is very low and close to the measurement limit of the current setup. Therefore, a higher frequency of 2.5 MHz with 50% duty cycle and rise/fall times of 15 ns each is selected in CP measurement. To make sure the measured $I_{\rm cp}$ is still reliable at this frequency, the frequency dependence of normalized CP current at program state is shown in Fig. 2. The constant $I_{\rm cp}/f$ confirms the validity of the CP measurement.

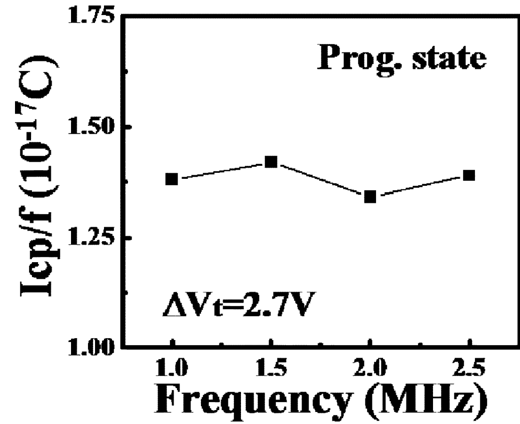

Fig. 2. Dependence of normalized CP current ($I_{\rm cp}/f$) on measurement frequency. In CP measurement, the V_t window (ΔV_t) is 2.7 V and $I_{\rm cp}$ is measured at $V_{\rm gl} = 2.5$ V.

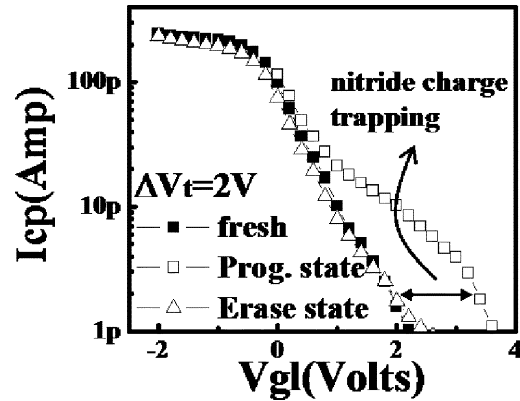

Fig. 3. $I_{\rm cp}$ versus $V_{\rm gl}$ in a fresh cell, in program state and in erase state, respectively. The V_t window (ΔV_t) is 2 V. V_d in CP measurement is 0 V.

III. Measurement Result and Discussion

A. Single-Bit Storage

Fig. 3 shows the $I_{\rm cp}$ versus $V_{\rm gl}$ curves in a virgin cell, after programming only, and after one P/E cycle, respectively. Only the first bit (drain side) is P/E cycled and the V_d in CP measurement is 0 V. The threshold voltage window (ΔV_t) is 2 V. The $I_{\rm cp}$ in a virgin cell and in erase state are almost identical, whereas a noticeable $I_{\rm cp}$ bump at program state is noticed. This $I_{\rm cp}$ bump is attributed to a local increase of channel threshold voltage due to negative nitride charge trapping. To verify the nitride charge storage effect, the $I_{\rm cp}$ characteristics for two different threshold voltage windows, $\Delta V_t = 2$ V and 2.7 V, are compared in Fig. 4. As expected, the larger threshold voltage window exhibits a larger $I_{\rm cp}$ bump due to more stored electrons. The dependence of the program-state $I_{\rm cp}$ bump on V_d in charge pumping measurement is shown in Fig. 5. The $I_{\rm cp}$ bump is suppressed as V_d increases. The reason is that the drain depletion region increases with V_d. At a sufficiently large V_d (in this Fig. 1.8 V), interface traps underneath the program charges are completely "masked" by the drain depletion region. Thus, these interface traps can no longer go through inversion-accumulation cycles in CP measurement and do not contribute to $I_{\rm cp}$. As a result, the program-state $I_{\rm cp}$ bump is totally suppressed. Our

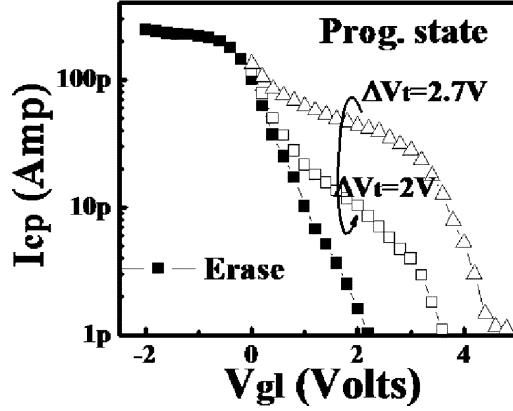

Fig. 4. $I_{\rm cp}$ versus $V_{\rm gl}$ for different V_t window. The program state $I_{\rm cp}$ bump increases with V_t window due to more injected charges.

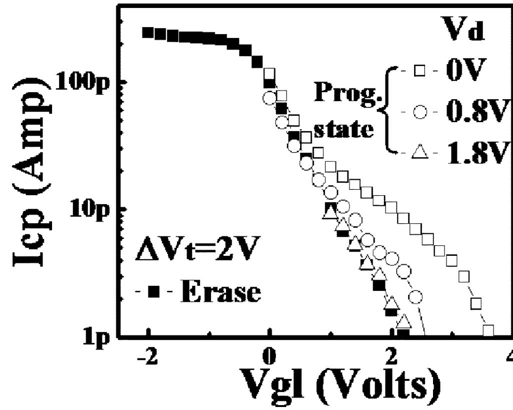

Fig. 5. $I_{\rm cp}$ versus $V_{\rm gl}$ with different V_d in CP measurement. The program-state $I_{\rm cp}$ bump decreases with V_d. The V_t window is 2 V.

result here implies that a V_d about 1.8 V is necessary in reverse read to avoid completely the second bit effect.

B. Two-Bit Storage

The Nbit cell stores two bits at different locations (drain-side and source-side). Each bit within a cell serves as binary unit of data that is totally mapped to four states in a memory cell. The $I_{\rm cp}$ of the four states corresponding to "11," "10," "01" and "00" are shown in Fig. 6. "00" denotes both bits in program state. "10" (or "01") denotes the drain-side bit in erase state (or in program state) and the source-side bit in program state (or in erase state). To explore the influence of the programming sequence on trapped charge spatial profile, the CP measurement is performed after each bit is programmed. Fig. 7 shows the $I_{\rm cp}$ of the first programmed bit and the second programmed bit, respectively. Here, the $I_{\rm cp}$ of the second programmed bit is obtained in two ways. One is to measure $I_{\rm cp}$ after the first bit is erased. The second approach is to subtract the fist bit $I_{\rm cp}$ from the "00" state $I_{\rm cp}$. Fig. 8 compares the second bit $I_{\rm cp}$ from the above two approaches and the result is almost the same. It should be emphasized that a crossover of the first bit and the second bit $I_{\rm cp}$ in Fig. 7 is observed. This suggests that the second programmed bit has a wider charge distribution but a smaller peak density. The reason will be discussed later. To profile the nitride stored charge lateral distribution, a technique similar to [9] is performed. In

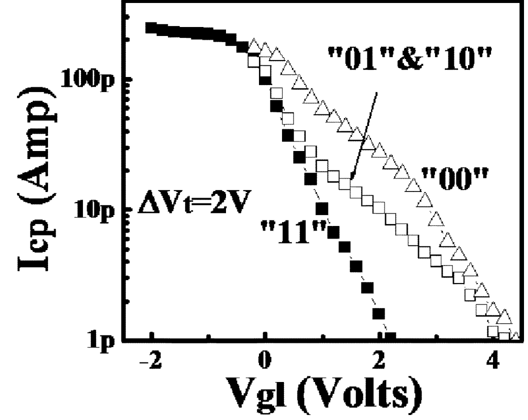

Fig. 6. $I_{\rm cp}$ versus $V_{\rm gl}$ of the four states of two-bit storage. "11" represents both bits in erase-state and "10" represents one bit in erase-state and one bit in program-state.

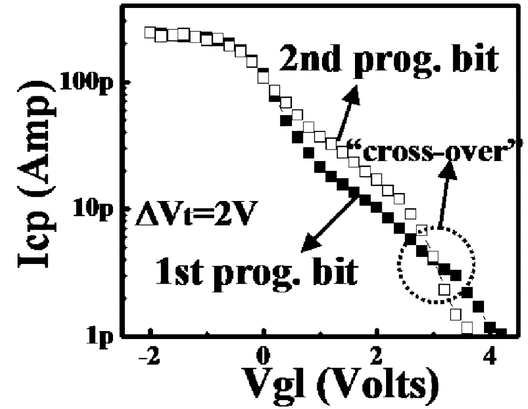

Fig. 7. Comparison of the $I_{\rm cp}$ versus $V_{\rm gl}$ of the first programmed bit and the secondly programmed bit. The second bit $I_{\rm cp}$ is measured with the first bit erased.

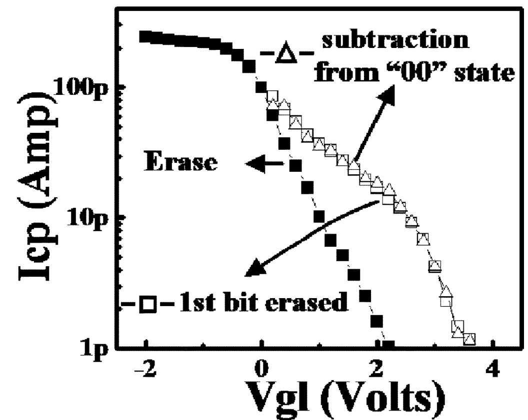

Fig. 8. Comparison of the second bit $I_{\rm cp}$-$V_{\rm gl}$ from two approaches. One is to measure $I_{\rm cp}$ after the first bit is erased. The second approach is to subtract the fist bit $I_{\rm cp}$ from the "00" state $I_{\rm cp}$.

profiling, we make the following assumptions. First, we assume that a fresh cell has uniform interface trap density ($N_{\rm it}$) along the channel [9]. The CP current thus should have a linear dependence on channel position x

$$x = \frac{I_{\rm cp}(V_{\rm gl})}{I_{\rm cp,max}} L_{\rm ch} \tag{1}$$

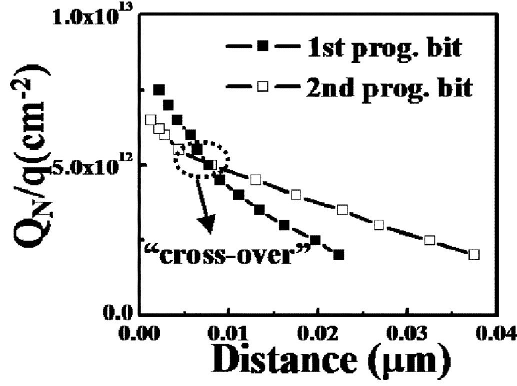

Fig. 9. Lateral profiling of the programmed charge distribution of the first programmed bit and the secondly programmed bit. A uniform interface trap distribution along the channel is assumed. $I_{\mathrm{cp,max}}$ in (1) is 195 pA.

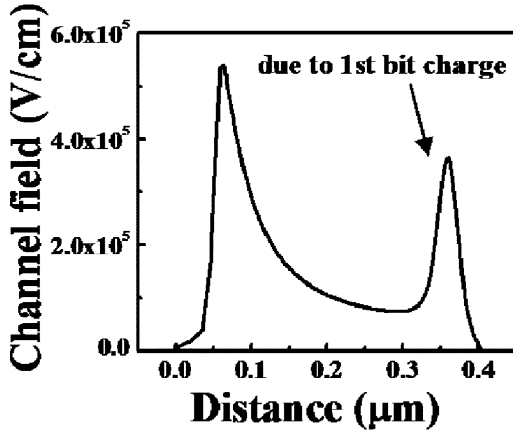

Fig. 10. Simulated channel field distribution in second bit programming from 2-D device simulation. $x = 0$ is at the n$^+$ source edge and $x = 0.4$ is at the n$^+$ drain edge. $V_s = 6.5$ V and $V_g = 11$ in second bit programming.

where $x = 0$ is defined at the edge of the source or drain junction. L_{ch} is the channel length and $I_{\mathrm{cp,max}}$ denotes the saturated CP current. The second assumption is that N_{it} generation after one program/erase (P/E) cycle is negligible. Based on these assumptions, the nitride charge distribution is deduced as follows:

$$Q_N(x) = \frac{C_{\mathrm{ONO}}}{q}(V_{\mathrm{gl}} - V_{\mathrm{ti}}) \tag{2}$$

where $Q_N(x)$ is the nitride charge density at the position x, and V_{ti} stands for the threshold voltage of a fresh device. Fig. 9 depicts the extracted stored charge distribution of the first programmed bit and the second programmed bit versus a distance from the source/drain junction. The stored charges extend into the channel about tens of nanometers. This result is in agreement with the simulation in [7]. In addition, the CP measurement result shows that the second programmed bit exhibits a broader distribution but a smaller peak density. To explain this result, a two-dimensional device simulation is performed. A rectangular charge distribution with a width of 30 nm and a charge density of 1.6×10^{19} cm^{-3} is used. Fig. 10 shows the lateral channel electric field distribution in the second bit programming. A large channel field exists not only in the programmed region but also in the first bit region (drain side). Such a large field in the first bit region will accelerate channel electrons from the drain and cause

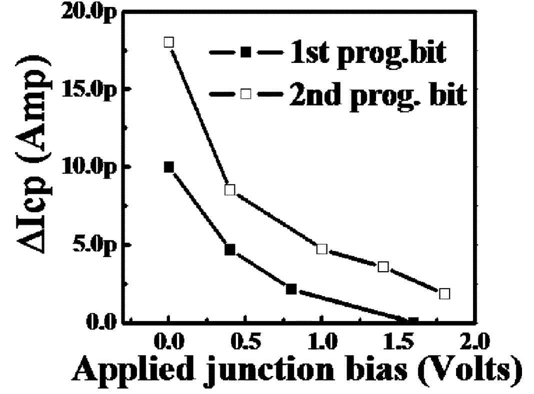

Fig. 11. Difference in I_{cp} between program-state and erase-state as a function of drain bias for the first bit and source bias for the second bit. The ΔI_{cp} is obtained from Figs. 6 and 7 at $V_{\mathrm{gl}} = 1.6$ V.

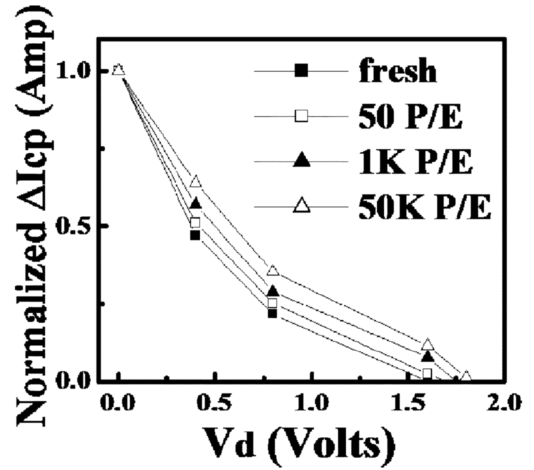

Fig. 12. Difference in I_{cp} between program state and erase state as a function of V_d in CP measurement at various P/E cycle numbers. ΔI_{cp} is measured at $V_{\mathrm{gl}} = 1.6$ V and is normalized to its value at $V_d = 0$ V to take into account interface trap creation in cycling.

earlier hot electron injection into the nitride, thus resulting in a broader second bit distribution. Finally, we would like to remark that (2) and consequently Fig. 9 are derived from a simplified one-dimensional model. For a narrow charge distribution by hot electron programming, (2) only serves as a first-order approximation. Accurate profiling of programmed charge distribution requires a more complicated 2-D model.

The programmed charge lateral extent can be also probed by varying V_d (or V_s) in CP measurement. Fig. 11 shows the difference in I_{cp} between program state and erase state versus V_d (or V_s). ΔI_{cp} is measured at $V_{\mathrm{gl}} = 1.6$ V. The second programmed bit needs a larger junction bias to "mask" the programmed charge. The same conclusion that the second bit has a broader charge distribution is obtained.

C. P/E Cycling Stress Effect

The P/E cycling stress effect on programmed charge distribution is examined in Fig. 12 by using the variable V_d method. The V_t window keeps the same during cycling. Again, the ΔI_{cp} is measured at $V_{\mathrm{gl}} = 1.6$ V and is normalized to its value at $V_d = 0$ V to compensate for interface trap creation effect for different cycling stress. It has been reported that hot-carrier stress

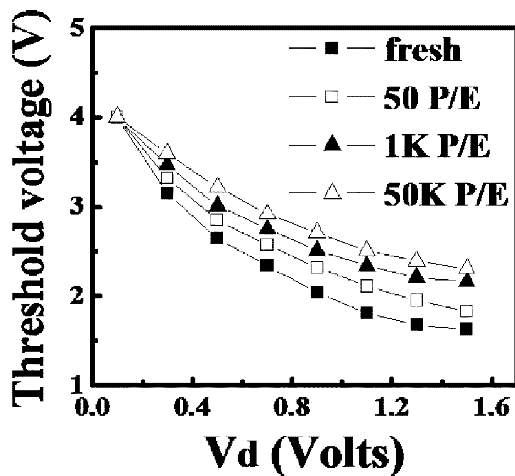

Fig. 13. Threshold voltage versus reverse read V_d for different cycle numbers.

created oxide traps spread toward the channel with stress time [10], [11]. Such traps, especially positively charged traps, can effectively lower the Si/SiO_2 injection barrier [12], [13] and enhance the electron injection probability. Therefore, as cycle number (stress time) increases, the hot electron injection region expands toward the channel due to the spread of the bottom oxide damaged region. A larger V_d in CP measurement is necessary to screen programmed charge at a larger cycle number. The consequence of the broadening of programmed charge distribution is the degradation of the second bit effect. Fig. 13 shows the threshold voltage versus V_d in reverse read for different cycle numbers. The second bit effect is apparently worsened with increasing cycle number.

IV. Conclusion

We have characterized the programmed charge lateral distribution in a two-bit storage nitride Flash cell by a channel hot electron program. The CP measurement reveals that the charge distribution of each bit extends into the channel for tens of nanometers. This suggests the possibility of further scaling down the nitride Flash cell with respect to the overlap of two bit charges. Our paper also shows that the charge distribution of the second programmed bit is influenced by the stored charge of the first bit. A broader second bit charge distribution is obtained.

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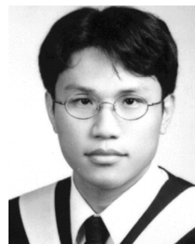

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Dr. Lu was the Executive Secretary and Managing Director of the Board and Board Director since 1998 for the Physical Society of Taiwan. from 1981 to 1984. He has been Vice-Chairman and then Chairman of IEEE Electron Devices Society, Taipei Chapter, from 1991 to 1996, and Board Director and Supervisor of IEEE Section since 1996. He is a member of many honor societies, including Sigma Pi Sigma, Phi Tau Phi, and Phi Lambda. He is a life member of the American Physical Society, the Physical Society of ROC, the Chinese Institute of Engineers, and CIE-USA. He received the National Science and Technology Achievement Award from the Prime Minister of Taiwan in 1994. In 1995, he was awarded the National Invention Award, and in 2002, he was awarded the most prestigious semiconductor award in Taiwan—the Pan Wen Yuan Award.