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Simulation study of 14-nm-gate III-V trigate field effect transistor devices with $In_{1-x}Ga_xAs$ channel capping layer

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In this work, we study characteristics of 14-nm-gate InGaAs-based trigate MOSFET (metal-oxide-semiconductor field effect transistor) devices with a channel capping layer. The impacts of thickness and gallium (Ga) concentration of the channel capping layer on the device characteristic are firstly simulated and optimized by using three-dimensional quantum-mechanically corrected device simulation. Devices with $In_{1-x}Ga_xAs/In_{0.53}Ga_{0.47}As$ channels have the large driving current owing to small energy band gap and low alloy scattering at the channel surface. By simultaneously considering various physical and switching properties, a 4-nm-thick $In_{0.68}Ga_{0.32}As$ channel capping layer can be adopted for advanced applications. Under the optimized channel parameters, we further examine the effects of channel fin angle and the work-function fluctuation (WKF) resulting from nano-sized metal grains of NiSi gate on the characteristic degradation and variability. To maintain the device characteristics and achieve the minimal variation induced by WKF, the physical findings of this study indicate a critical channel fin angle of 85° is needed for the device with an averaged grain size of NiSi below 4x4 nm^2. [http://dx.doi.org/10.1063/1.4922190]

I. INTRODUCTION

Silicon-based metal-oxide-semiconductor field effect transistor (MOSFET) devices face various challenges on materials, structural innovation, and process improvement. High-speed MOSFET devices could be realized by using InGaAs related materials owing to their high electron mobility.[1] Recent studies on III-V FETs have shown fascinating characteristics from thin-channel planner MOSFETs.[2,3] III-V junctionless FET devices have also been reported for even superior on-/off-state current ratio.[4,5] InGaAs/InAlAs is one of highly attractive III-V materials due to little lattice mismatch[6] and outstanding heterojunction transport property.[7] III-V materials have the higher electron mobility than silicon one which can increase the driving current. However, the leakage current will be increased at the same time. Consequently, proper channel capping or barrier layers[8–11] will be beneficial for device applications. However, the effect of channel capping layers on electircal and physical characteristics of the aforementioned devices has not been clearly investigated.

In this work, we study the impact of the thickness (T_{cap}) and the mole fraction (x) of gallium (Ga) of channel capping layer on physical and electrical characteristics of 14-nm $In_{1-x}Ga_xAs$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ / InP trigate MOSFET on silicon substrate. Notably, devices with high-κ/metal gate (HKMG) have attracted great attention.[12–19] Owing to similarity in materials

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of capping layer $In_{1-x}Ga_xAs$ and channel layer $In_{0.53}Ga_{0.47}As$, the explored new device could be fabricated. By considering physically noticeable parameters of short-channel effect (SCE): on-/off-state current (I_{on}/I_{off}) > $1.7x10^6$, subthreshold swing (SS) < 72 mV/dec, and drain-induced barrier lowering (DIBL) < 55 mV/V simultaneously, we will find the feasible range of T_{cap} and x for high-performance device applications, where the threshold voltage (V_{th}) is targeted at 160 mV. After that, metal gates may introduce a random fluctuation source, so-called the work-function fluctuation (WKF)[20–23] owing to the dependency of work function (WK) on the random orientation of nano-sized metal grain.[24] Such uncontrollable grain orientations result in random WK of metal during fabrication period.[23,25] Many studies concerning WKF on silicon-based planar devices have been reported,[20,21,24] but researches about the WKF on III-V MOSFETs[26] have not been well explored. Theoretically, ideally rectangular shape of the trigate may not always guarantee because of limitations of the fabrication process in III-V MOSFET devices. The process distortion comes from lithography processes and etching steps causes significant SCEs and degrades the device performance.[27,28] Therefore, we further discuss characteristic variation resultin from different channel fin angle and WKF of gate metal.

This paper is organized as follows. Section II introduces the device structure and simulation settings. Section III reports the impact of the thickness of $In_{1-x}Ga_xAs$ capping layer and the mole fraction of Ga on III-V trigate MOSFET and discusses the WKF-induced and channel-fin-angle-variability for the achieved optimal devices including the fluctuation suppression and the proper channel fin angle to be adopted. Finally, we draw conclusions and suggest future work.

II. DEVICE CONFIGURATION AND SIMULATION METHODOLOGY

Figure 1(a) shows a 3D-plot of the InGaAs-based trigate MOSFET. Above the silicon substrate is the 1-μm-thick InP then the 1.5-μm-thick p-type doped by beryllium $1x10^{15}$ cm^{-3} $In_{0.52}Al_{0.48}As$ buffer layer follows, and undoped $In_{0.53}Ga_{0.47}As$ channel layer is applied. The channel capping layer of $In_{1-x}Ga_xAs$ with different x and T_{cap} is covered with $TaSiO_x$. Source/drain is doped by silicon as n-type dopant. Figure 1(b) is a cross-sectional view along the cutting line AA', where the intrinsic channel is $In_{0.53}Ga_{0.47}As$ with a capping layer of $In_{1-x}Ga_xAs$. The adopted parameters, such as effective oxide thickness, work function, and doping concentrations, are listed in Table I, where T_{cap} varies from 0 to 5 nm and x is from 0.27 to 0.42.

To minimize the random dopant fluctuation,[29] undoped $In_{1-x}Ga_xAs$ capping layer above channel is studied. Optimal channel capping layer of $In_{1-x}Ga_xAs$ will be discussed subject to the aforementioned SCE parameters. The 3D drift-diffusion model and density-gradient equations are solved numerically at the same time for including quantum mechanical effects. The band gaps of the relevant binary compounds are functions of temperature T:

$$E_g(\text{InAs}) = 0.36 - \frac{2.760\times10^{-4}T^2}{T+93}, \tag{1}$$

$$E_g(\text{GaAs}) = 1.42 - \frac{5.405\times10^{-4}T^2}{T+204}, \tag{2}$$

and the band gap of ternary compound depending on composition fraction x is given by:[30]

$$E_g(In_{1-x}Ga_xAs) = 0.36 + 0.629x + 0.436x^2. \tag{3}$$

The scattering which causes the mobility degradation is dominated by phonon scattering and the high normal field inside capping layers. The acoustic mobility due to acoustic phonon scattering is

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C(N_i/N_0)^\lambda}{F_\perp^{1/3}(T/300K)^k}, \tag{4}$$

where B and C are the fitting parameters.[31] Notably, the acoustic mobility is inversely proportional to the effective masses which are incorporated into the fitting parameters.[31] The contribution

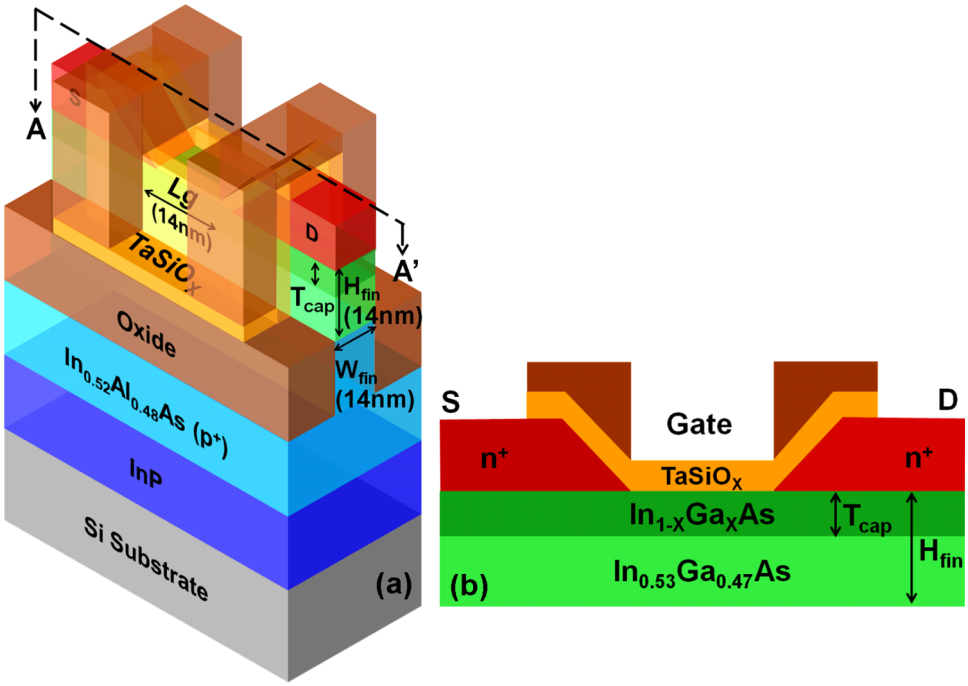

FIG. 1. (a) 3D structure of the explored III-V trigate MOSFET. (b) Zoom-in cross-sectional view of the device, along the cutting line AA' in (a).

TABLE I. Parameters used for the simulated devices.

Effective oxide thickness (nm)	0.52
Gate work function (eV)	4.9
$In_{1-x}Ga_xAs$ (S/D layer) (cm^{-3})	$1x10^{19}$ (Si)
$In_{1-x}Ga_xAs$ (capping layer) (cm^{-3})	Undoped
$In_{0.53}Ga_{0.47}As$ (channel) (cm^{-3})	Undoped
$In_{0.52}Al_{0.48}As$ (buffer layer) (cm^{-3})	$1x10^{15}$ (Be)
InP (cm^{-3})	$1x10^{16}$ (Be)

attributed to surface roughness scattering is given by:

$$\mu_{sr} = \left(\frac{(F_\perp/F_{ref})^2}{\delta} + \frac{{F_\perp}^3}{\eta}\right)^{-1}. \tag{5}$$

These surface contributions to the mobility are then combined with the bulk mobility μ_b:

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}}. \tag{6}$$

The reference field $F_{ref} = 1$ V/cm ensures a unitless numerator in Eq. (5). $F_\perp$ is the transverse electric field normal to the semiconductor-insulator interface. $D = \exp(-y/l_{\text{crit}})$ (where y is the distance from the interface and l_{crit} is a fit parameter) is used to describe the damping that switches off the inversion layer from the interface. The other parameters are listed in Table II.

Devices will be operated under high electric fields; the drift velocity of carrier is no longer proportional to the electric field and will be saturated. To describe this, the high-field mobility model[32] is further considered:

$$\mu_F = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} \cdot F}{v_{sat}}\right)^{\beta_F}\right]^{1/\beta_F}}, \tag{7}$$

TABLE II. List of the adopted parameters.

Coefficients	Electrons	Holes	Unit
B	9.5x10^8	9.925 x10^6	cm/s
C	1.16 x10^4	2.947 x10^3	cm$^{5/3}$/(V$^{2/3}$s)
N_0	1	1	cm^{-3}
λ	0	0.0317	1
k	1	1	1
δ	1 x10^{14}	2.0546 x10^{14}	V/s
η	2 x10^{20}	2.0546 x10^{30}	V^2/(cmxs)
l_{crit}	1 x10^{-6}	1 x10^{-6}	cm

where the low-field mobility μ_{low} is calculated from Eq. (6), the exponent β_F, ν_{sat}, and the driving force F are given by

$$\beta_F = \beta_0(\frac{T}{T_0})^{\beta_{\text{exp}}}, \tag{8}$$

$$v_{sat} = A_{vsat} - B_{vsat}(\frac{T}{T_0}), \tag{9}$$

and

$$F_c = \vec{E} \cdot (\frac{\vec{j_c}}{|j_c|}), \tag{10}$$

where T denotes the lattice temperature, and the $\vec{j_c}$ is the electron or hole current vector. Detail parameters are listed in Table III.

The traps placed at the high-κ gate oxide-InGaAs interface are distributed within a narrow gap near the conduction band edge. They are acceptor type and negatively charged when occupied, where the density of interface traps is 4x10^{11} eV^{-1}cm^{-2}.[33] By solving a set of 3D quantum-mechanically corrected device transport equations,[34–38] the current density, the carrier's density, the electric field, and related physical quantities are calculated for the entire device structure. The drain voltage of 0.8 V and the gate voltage varying from -0.2 to 0.8 V are supplied. The constant current method that the drain current sets at 100 nA/μm is used to extract the threshold voltage (V_{th}).

Devices will suffer work-function fluctuation because the dependency of work function on the random orientation of nano-sized metal grain. Nickel has very high work function, and its compounds are usually used for metal gate. It has three orientations and each orientation has its corresponding work function with certain probability. It has been reported that the nickel silicide (NiSi) work function can be adjusted to 4.9 eV,[39] and the compounds usually have a strong correlation with the original materials. Therefore, we assume that nickel silicide has three kinds of work function with the corresponding probabilities. The work functions are 4.75, 4.85, and 5.05 eV with the probabilities: 30%, 30%, and 40%, respectively. First, under the optimal case of thickness and composition of the capping layer, we partition the gate metal into many sub-regions. Second, randomly generate work function in the sub-region according to the probability distribution of

TABLE III. List of the adopted parameters.

Coefficients	Electrons	Holes	Unit
β_0	2	2	1
β_{exp}	0	0	1
A_{vsat}	4.5x10^7	1 x10^7	cm/s
B_{vsat}	5x10^6	3.6x10^6	cm/s

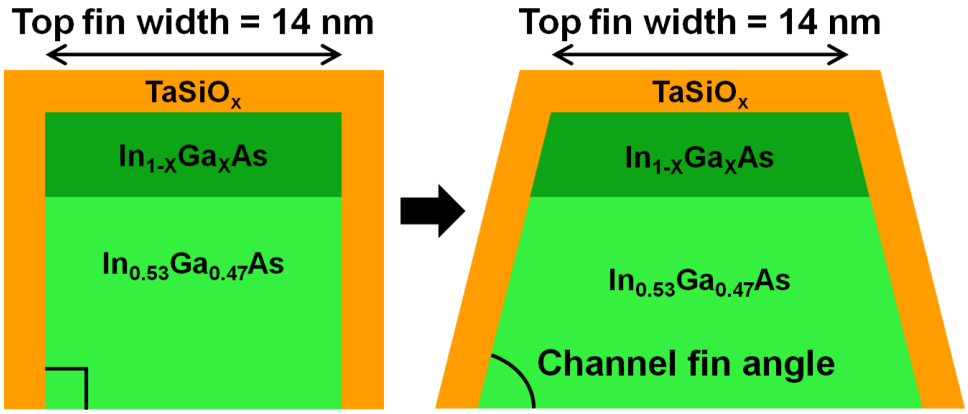

FIG. 2. The cross-sectional views of the rectangular and trapezoidal channel with 14-nm top-fin width. The channel fin angle is defined on it.

orientation. Finally, generate samples and solve a set of 3D quantum transport equations, where details of WKF simulation follow one of our recent works.[40] Theoretically, ideally right-angle shape (channel fin angle = 90°) of the trigate may not always guarantee because of limitations of the fabrication process in trigate III-V MOSFET devices. Therefore, according to the optimized case of thickness and composition of the channel capping layer above, we do further analyze the effect of process variation on the characteristic variability for the device with non-ideal cross-sectional channel shapes (i.e., devices with different channel fin angles). The device with trapezoidal-shaped channels is shown in Fig. 2, where the top-fin width is fixed at 14 nm and the channel fin angle varies from 70° to 90°. We calibrate all simulation cases having the same threshold voltage to explore the characteristic degradations owing to SCEs on trapezoidal-shape devices and WKF with different channel fin angles.

III. RESULTS AND DISCUSSION

The energy band diagram, as shown in Fig. 3, is first simulated for both the on- and off-state from the channel surface to the substrate. Zoom-in plots of Figs. 3(a) and 3(b) clearly show that the conduction band energies of T_{cap} = 4 nm are lower than that of T_{cap} = 0 nm owing to the small energy band gap. All energies of the off-state are above Fermi level, so the III-V device is normally off. For the on-state, as shown in Fig. 3(b), the conduction bands and Femi levels of electrons become negative. The electron's Fermi levels are above conduction bands, so the regions between electron's Fermi levels and conduction bands are filled with electrons. We can estimate the total electron concentration per unit volume in the conduction band by integrating the density of quantum states times the probability that a state is occupied by an electron over the conduction band energy. The conduction band energy is low, so the device with T_{cap} = 4 nm has the large electron concentration and on-state current.

Figure 4 shows the I_D-V_G and transconductance (g_m-V_G) curves with T_{cap} = 4 nm and different Ga concentrations. Devices with low Ga concentration show high on-state current, resulting from improved carrier mobility. The lattice constant of $In_{1-x}Ga_xAs$ with Ga mole fraction of 0.47 is about 0.586 nm, which matches with that of $In_{0.52}Al_{0.48}As$. For $x < 0.47$, the lattice constant of the capping layer is larger than 0.586 nm and the capping layer is subjected to a compressive strain. As the compressive strain increases, the alloy scattering decreases, resulting in improved electron mobility.[41] Furthermore, the mobility's reduction of the alloy scattering has its maximum effect at $x = 0.7$.[42] The reduction of the effective electron mass with the increasing indium concentration is also an important reason of mobility increasing, where the mobility is inversely proportional to the effective mass. As shown in Figs. 5(a) and 5(b), we plot the I_D-V_D characteristics. The energy band gap of capping layer is smaller than that of channel layer. Because we fix the fin height, the fin channel will have the higher percentage of small energy band gap with increasing capping layer.

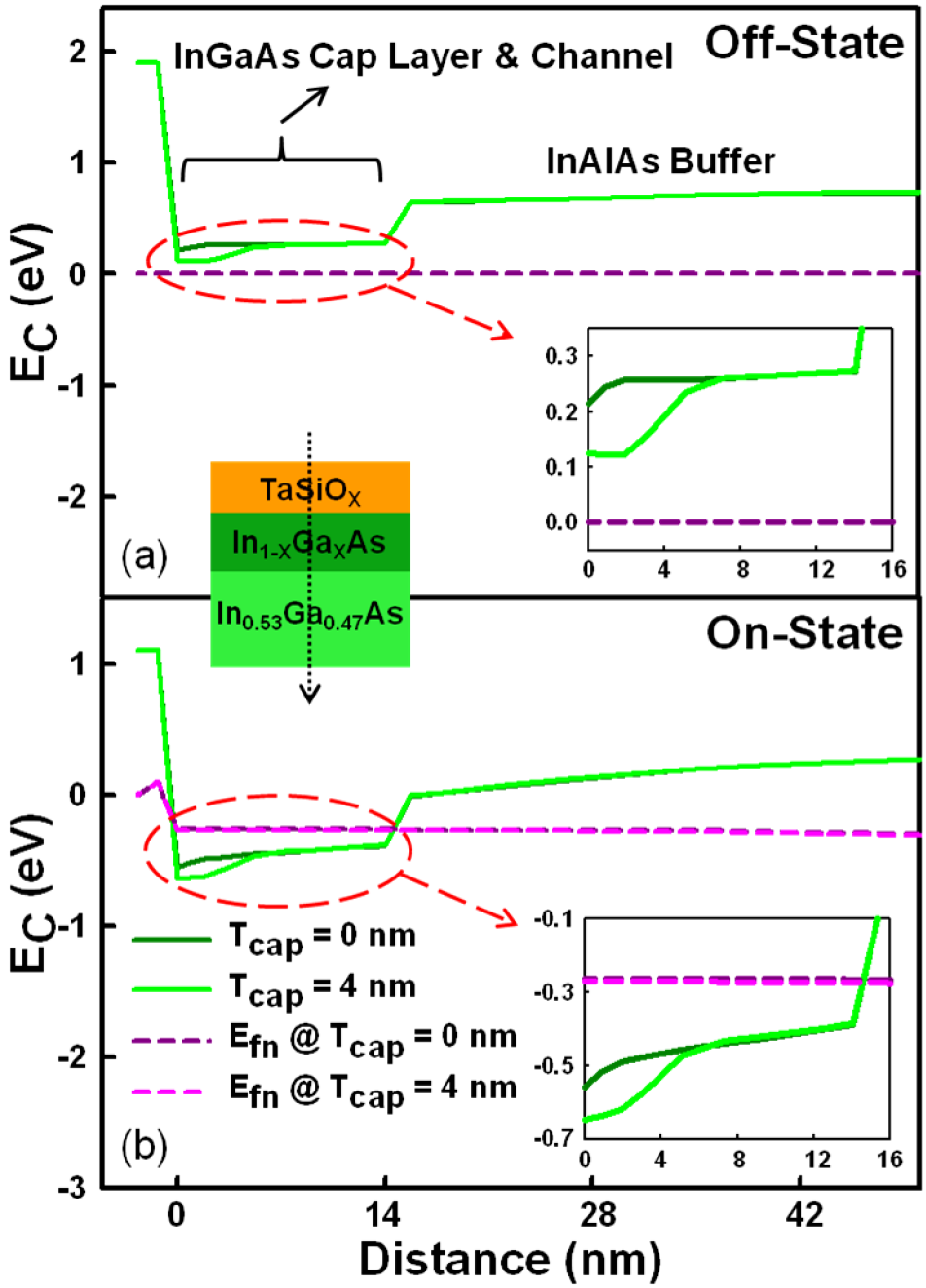

FIG. 3. (a) Off-state and (b) on-state energy band diagrams for the devices with $x = 0.32$ and different T_{cap} of 0 and 4 nm. The energy near the channel surface for device with 4-nm-thick capping layer is smaller than that of device without capping layer.

The mobility varies with capping layer composition that is similar for aforementioned reasons of Fig. 4. Hence, as the thickness of capping layer increases and the Ga mole fraction decreases, the device will possess large driving current due to relatively larger region of small band gap and high mobility. On the other hand, devices with a thick channel capping layer and a low Ga concentration have the large gate capacitance (C_G), as shown in Figs. 6(a)-6(b). Large C_G will induce large inversion charge thereby enhancing the current density which can also be explained by using the results in Fig. 8. Therefore, devices with thick T_{cap} and low x possess the enhanced gate controllability

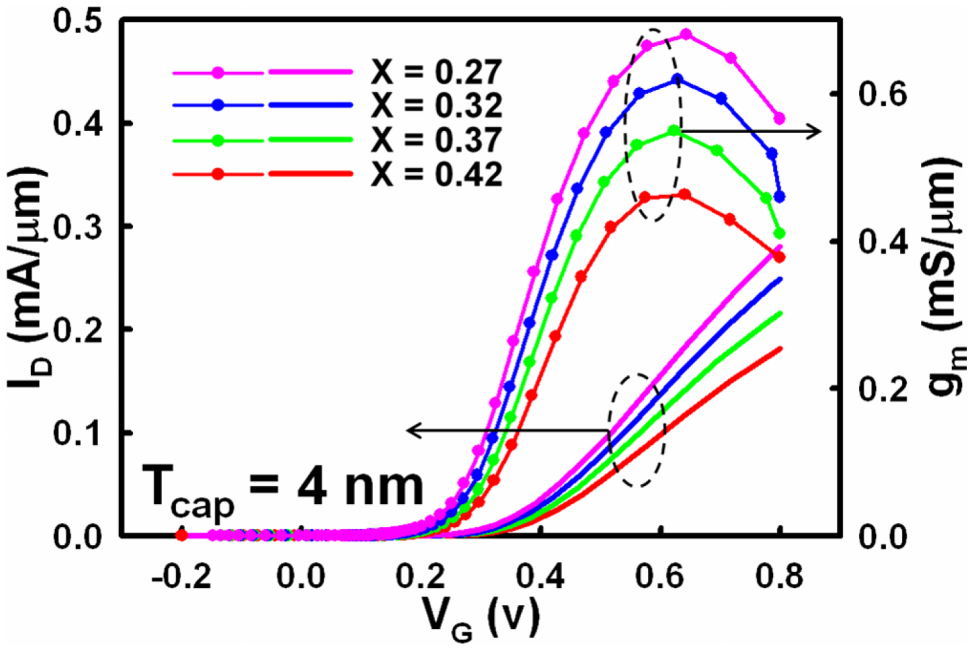

FIG. 4. Plots of I_D-V_G and g_m-V_G with different x and $T_{cap} = 4$ nm. A small x implies a low Ga concentration which may reduce the alloy scattering and effective mass and then increase the channel mobility. Thus, it has higher drive current.

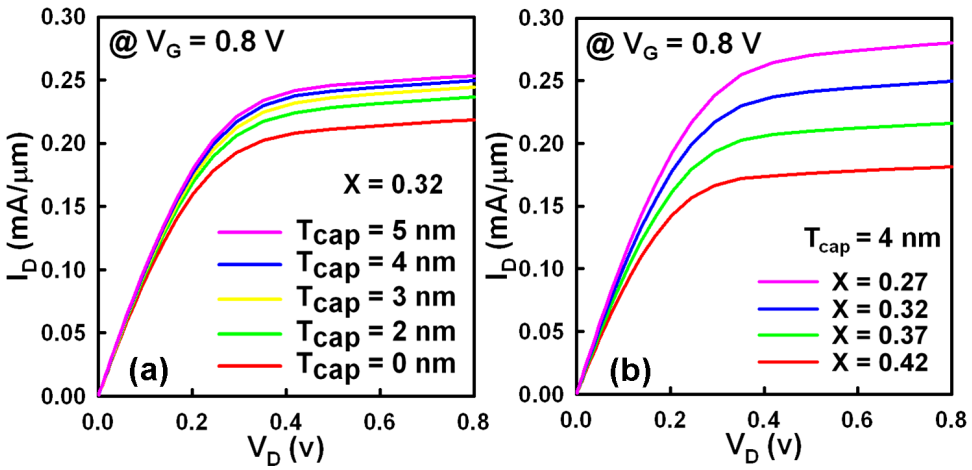

FIG. 5. (a) The I_D-V_D curves of the device with $x = 0.32$ and different T_{cap}. (b) The I_D-V_D curves of the device with $T_{cap} = 4$ nm and different x.

due to more carriers being sensitive to electrodes. Figures 7(a) and 7(b) even show the circuit gain versus operation frequency for different thickness and Ga mole fraction, respectively. We can obtain the wide unity-gain bandwidth by T_{cap} increasing and x decreasing. The unity-gain bandwidth is proportional to g_m/C_G,[43] and the variations of g_m are relatively larger than C_G under the conditions of different T_{cap} and x. Therefore, g_m dominates the influence of unity-gain bandwidth, and the result is corresponding to Fig. 4.

Figure 8 shows the electron density profiles at the on-state for different x and T_{cap}. No matter increasing the thickness of capping layer or decreasing the gallium concentration, the centroid of the inversion charge density in the channel is pulled toward the gate oxide interface; consequently, they will induce high electron density and increase the on-state current. It also explains the tendency of transport current in Fig. 5. Notably, this phenomenon increases the gate control over the channel

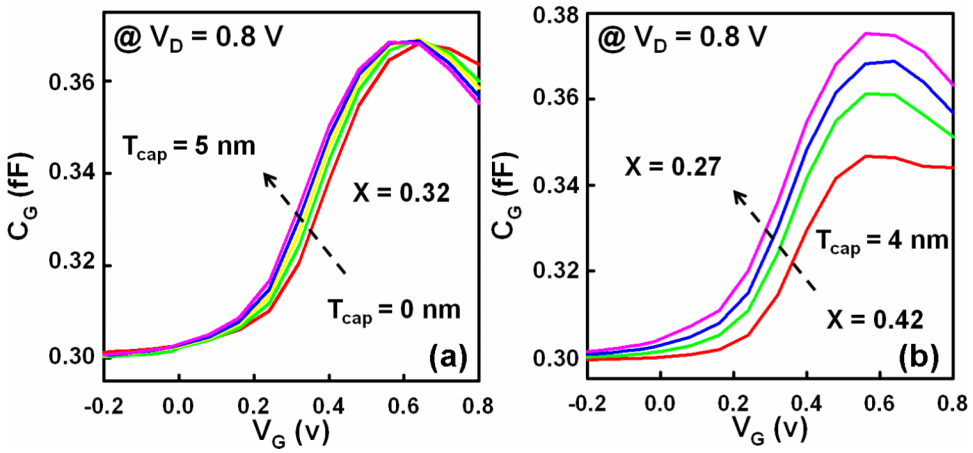

FIG. 6. (a) The C_G-V_G curves of the device with $x = 0.32$ and different T_{cap}. (b) The C_G-V_G curves of the device with $T_{cap} = 4$ nm and different x.

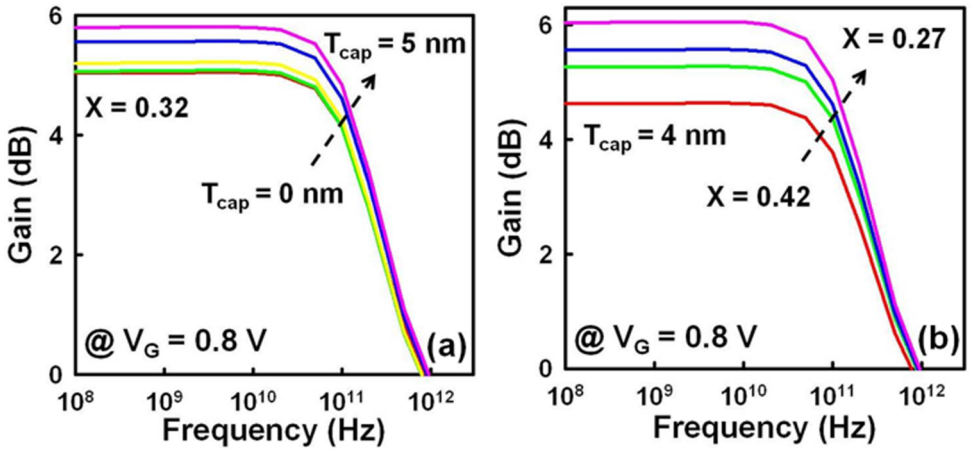

FIG. 7. The curves of gain versus operation frequency for (a) $x = 0.32$ and different T_{cap} and (b) $T_{cap} = 4$ nm and different x.

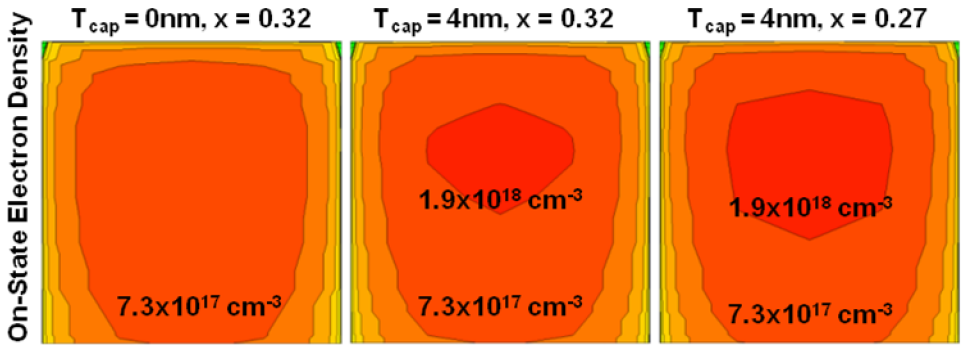

FIG. 8. The on-state electron density. T_{cap} increasing and x decreasing not only induce high electron density but also pull the centroid of inversion charge density in the channel toward the gate oxide interface.

thereby reducing the impact of SCEs. Thus, to suggest the optimal design of channel capping layer, we plot the SS, DIBL, I_{on}/I_{off} and V_{th} versus the x and T_{cap} to observe the trends, as shown in Fig. 9. Both SS and DIBL decrease with T_{cap} increasing and x decreasing, as plotted in Figs. 9(a)-9(b). However, although the on-state current increases due to small band gap and high mobility, the off-state current also increases; thereby, a trade-off exists for the on-/off-state current ratio, as shown

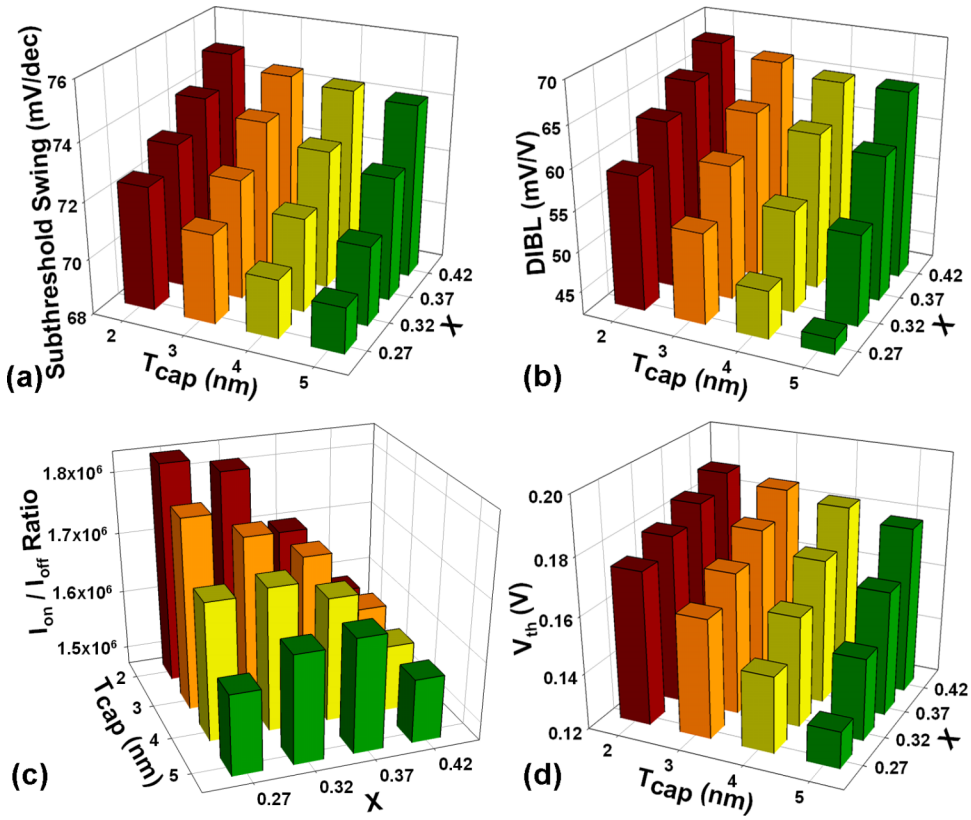

FIG. 9. Plots of (a) SS, (b) DIBL, (c) I_{on}/I_{off} ratio, and (d) V_{th} versus the x and T_{cap}, respectively. Increasing T_{cap} and decreasing x of $In_{1-x}Ga_xAs$ will reduce the V_{th} and improve the SS and DIBL; however, there is a trade-off for the variation of I_{on}/I_{off} ratio.

in Fig. 9(c). Finally, if a V_{th} of 160 mV is considered for high-performance device applications, a 4-nm thickness of $In_{1-x}Ga_xAs$ channel capping layer with $x = 0.32$ could be used accordingly.

Under the optimized parameters above, as shown in Fig. 2, the devices with trapezoidal-shaped channels where the channel fin angle varying from 70° to 90° are simulated. We calibrate all simulation cases having the same threshold voltage to explore the characteristic degradations. Table IV lists the extracted values of I_{on}, I_{off}, I_{on}/I_{off}, SS, and DIBL with different channel fin angles and the same V_{th} which equals to 160 mV. As channel fin angle decreases, the on-state current density decreases owing to fewer electrons to be inversed in the bottom channel. The on-/off-state current ratio also decreases with angle decreasing due to decreasing of on-state current and increasing of off-state current. Because we fix the top-fin width at 14 nm, when we decrease the channel fin angle, the bottom-fin width will increase. The region of bottom fin increasing causes the worse gate control over the channel. Therefore, the smaller the channel fin angle is, the less the SCEs can be suppressed. Notably, the critical angle for the case of SS < 75 mV/dec and DIBL < 75 mV/V is around 80°, as summarized in Tab. IV.

TABLE IV. Characteristics with respect to different channel fin angles.

Channel fin angle	I_{on} (A/μm)	I_{off} (A/μm)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)
70°	$1.58\text{x}10^{-4}$	$3.32\text{x}10^{-10}$	$4.74\text{x}10^{5}$	79.58	92
75°	$1.94\text{x}10^{-4}$	$2.85\text{x}10^{-10}$	$6.83\text{x}10^{5}$	77.60	82.67
80°	$2.11\text{x}10^{-4}$	$2.45\text{x}10^{-10}$	$8.59\text{x}10^{5}$	75.78	74.67
85°	$2.45\text{x}10^{-4}$	$2.43\text{x}10^{-10}$	$1.01\text{x}10^{6}$	73.72	65.33
90°	$2.49\text{x}10^{-4}$	$1.46\text{x}10^{-10}$	$1.71\text{x}10^{6}$	71.33	54.67

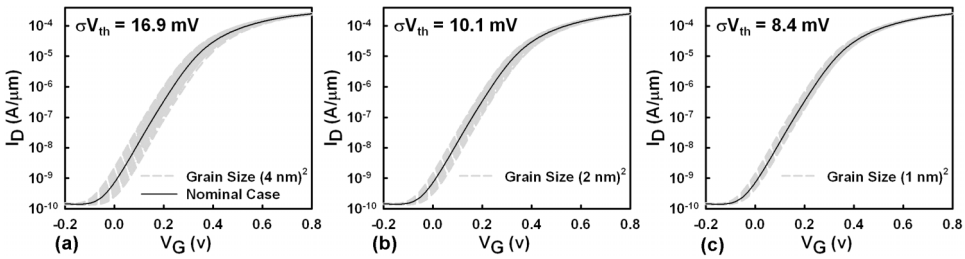

FIG. 10. (a)-(c) The fluctuation of drain currents with respect to different grain sizes. In the subthreshold region, the fluctuation is the largest due to being greatly affected with potential barrier.

Figures 10(a)–10(c) show the fluctuation of drain currents with respect to different sizes of metal grain for the device with an ideal channel fin (i.e., fin angle = 90°). When we apply negative bias voltage to the device (V_G = −0.2 V), holes will accumulate at the channel thereby reducing the effect of external electric field on the inside (so-called the screening effect); hence, the fluctuation of I_{off} is small (its magnitude of normalized fluctuations < 2%) for all cases of different grain sizes. In the subthreshold region, the gate voltage is small below the threshold voltage, so electrons are difficult to go through the channel and will be greatly affected with potential barrier. For the case of 4x4 nm^2 grain size, the magnitude of surface potential fluctuation is large and is governed by local work function which results in significant fluctuation of subthreshold region; for example, the normalized σI_{off} is about 50%. As we applying large gate voltage above the threshold voltage, inversion charges will fill the interface state of the channel and enhance the electron's screening effect. As shown in Fig. 10 and Fig. 12, the value of normalized σV_{th} is reduced from 10.56% to 5.25% when the grain size is reduced from 4x4 to 1x1 nm^2. Thus, when V_G = 0.8 V, the fluctuation of I_{on} is suppressed and

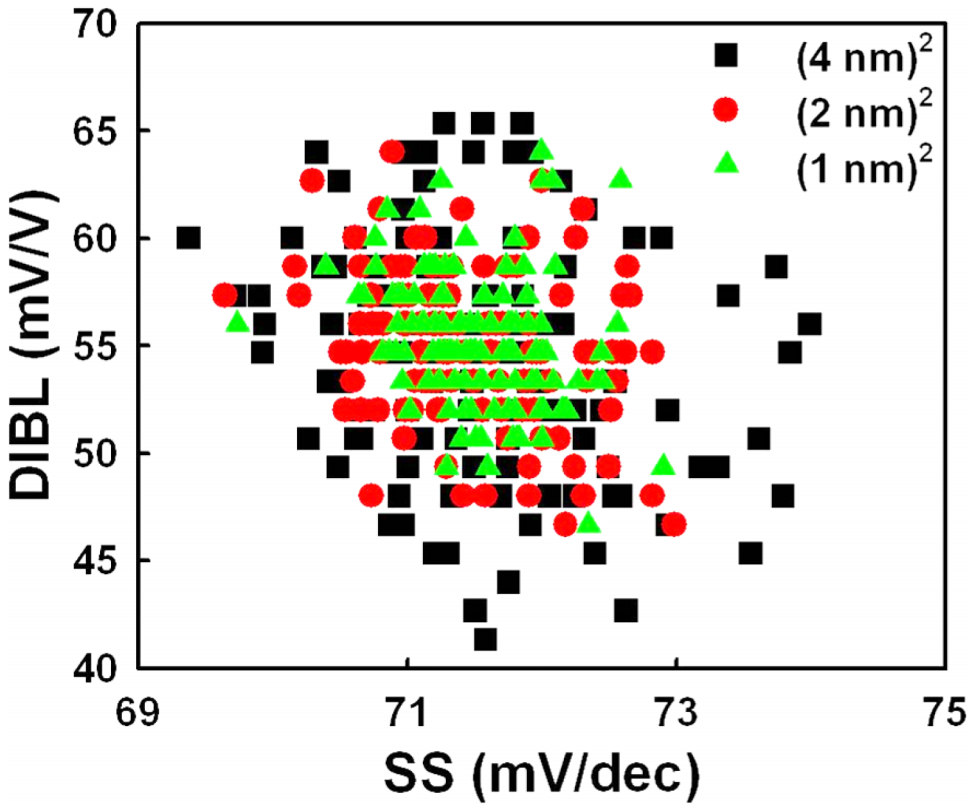

FIG. 11. The scatter plot of DIBL versus SS. The distribution region of 4x4 nm^2 grain size is the largest.

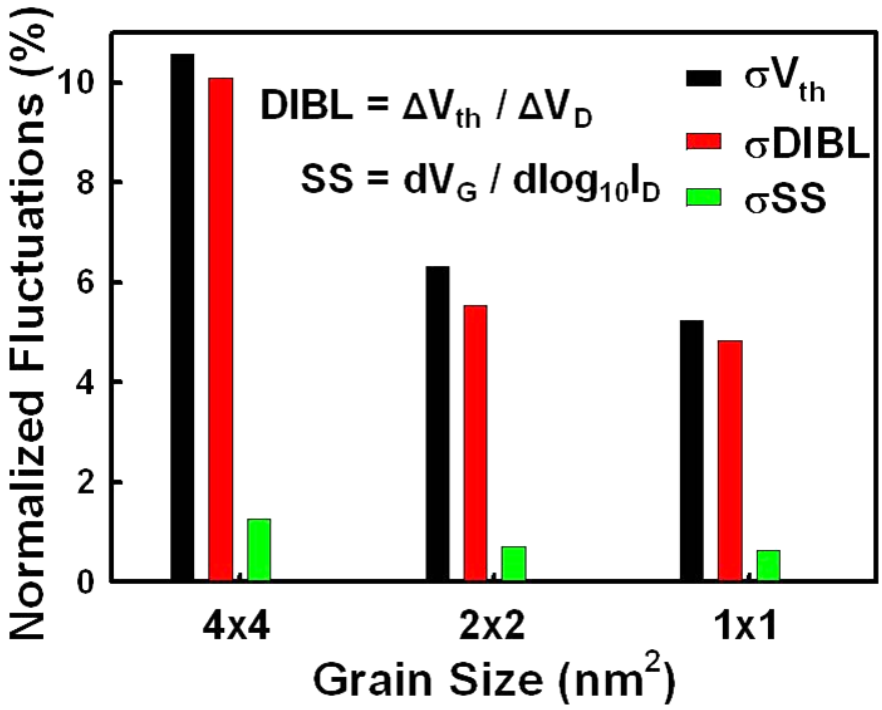

FIG. 12. The bar charts for standard deviations of V_{th}, DIBL and SS. All are normalized by the values of nominal case. As the grain size decreases, the fluctuation decreases.

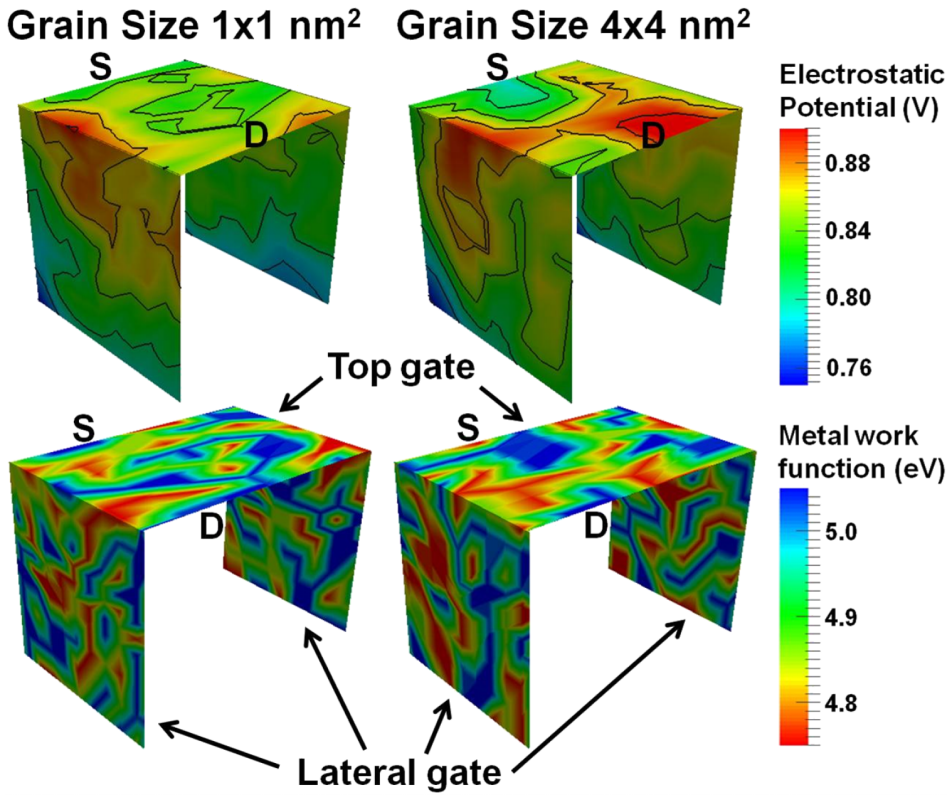

FIG. 13. The electrostatic potential with different grain sizes and the corresponding metal work function distribution under the same bias condition ($V_G = V_D = 0.8$ V). 1x1 nm^2 grain size has the smaller difference drop of the surface potentials.

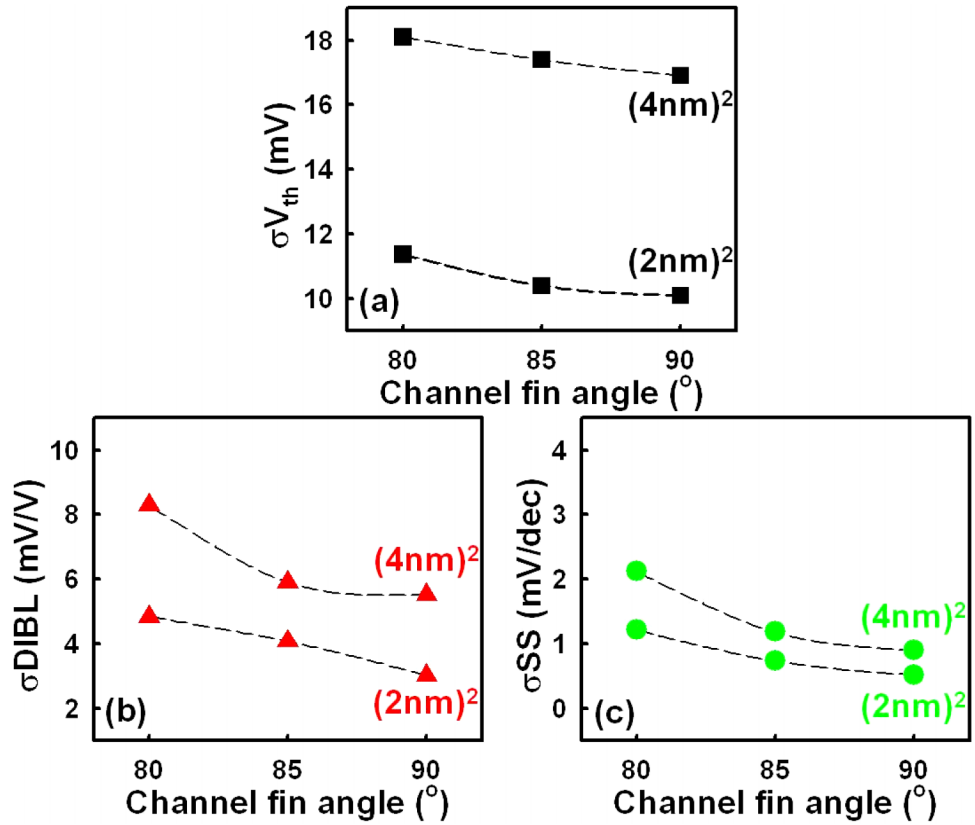

FIG. 14. Plots of the standard deviations of (a) V_{th}, (b) DIBL and (c) SS. The upper lines are for 4x4 nm^2 grain size, and the lower lines are for 2x2 nm^2 grain size. To maintain small fluctuation of V_{th}, DIBL and SS (for example, the normalized σV_{th}, σSS and σDIBL are within 7%), the channel fin angle should be between 85° and 90°.

the normalized fluctuation is within 3% owing to strongest screening effect. The σV_{th} of 4x4 nm^2 grain size is greater than twice the σV_{th} of 1x1 nm^2 grain size. Because the I_{off} (V_G = 0 V) has an exponentially increasing relation with V_{th}, the increment of σI_{off} is more significant with grain size increasing. Figure 11 shows the distribution of DIBL versus SS with respect to different grain sizes. The random distribution region of 4x4 nm^2 grain size is the largest among three different grain sizes, so the large size of metal grain will cause serious characteristic fluctuation. Furthermore, from Fig. 11, we can see that DIBL is more sensitive to the variation of metal grain size. The distribution of metal work function will strongly affect the electrostatic potential of the channel, and the variation of potential in the channel even directly decides the magnitude of threshold voltage. Therefore, DIBL's variation can significantly reflect the degree of WKF. Then, the bar charts for the normalized standard deviation of V_{th}, DIBL, and SS (σV_{th}, σDIBL, and σSS) are shown in Fig. 12. They are all normalized by their values of nominal case. The σSS is quite small that shows a stable switching characteristic. There is a significant reduction on the σDIBL when the size of metal grain is reduced from 4x4 to 2x2 nm^2. However, the difference of standard deviation between the cases of 2x2 and 1x1 nm^2 is small. To clarify it, as the grain size decreases, as shown in Fig. 13, the variation of surface potential of 1x1 nm^2 grain becomes smoother and relatively has the smaller potential difference (the maximum potential difference on the top fin is about 80 mV), compared with the case of 4x4 nm^2 grain (its maximum difference is 130 mV) thereby reducing the impact of fluctuation. From a device fabrication point of view, metal deposition at a low temperature or adding composite materials could be considered to obtain small size of metal grains.

We further explore the magnitude of WKF with respect to channel fin angles varying from 80° to 90°, according to the discussion above. As shown in Fig. 14, the magnitudes of σV_{th}, σDIBL, and σSS increase with decreasing the channel fin angle, and the fluctuations are more obvious from 85°

TABLE V. Comparison of recent works about InGaAs channel.

	Ref. 44	Ref. 41	Ref. 41	Ref. 26	In this work
Structure	QWFET	MOSFET	MOSFET	FinFET	Trigate MOSFET
Channel	InGaAs with InP layer above it	InGaAs with Barrier above it	InGaAs	InGaAs	InGaAs with capping layer
Lg (nm)	75	40	40	14	14
V_{DD} (V)	0.5	1.0	1.0	0.6	0.8
V_{th} (V)	0.2[a]	-0.3	-0.01	0.2	0.16
I_{on} (mA/μm)	0.49	0.11[a]	0.045[a]	0.35[a]	0.249
I_{off} (nA/μm)	30[a]	[b]	[b]	0.4[a]	0.146
g_m (mS/μm)	1.75	0.3[a]	0.15[a]	[b]	0.6248
f_T (GHz)	[b]	24[a]	11[a]	[b]	282.67
SS (mV/dec)	90[a]	[b]	[b]	70	71
DIBL (mV/V)	[b]	[b]	[b]	37	54
σV_{th} (mV)	[b]	[b]	[b]	68[a]	12.2
σSS (mV/dec)	[b]	[b]	[b]	1.0	0.95
σDIBL (mV/V)	[b]	[b]	[b]	[b]	5.5

[a]Estimated from the figures.
[b]Not available in the work.

to 80°. By normalizing these fluctuations to the value of nominal case with channel fin angle of 90°, we find that the change of σV_{th} of 4x4 nm^2 metal grain is larger than 10% for all the channel fin angles, as shown in Fig. 14(a), so it will not be suitable for device application if the averaged grain size is about 4x4 nm^2. For the case of the grain size below 4x4 nm^2, such as the 2x2 nm^2 grain size, the change of σDIBL is still large for the channel fin angle near 80°. Hence, as shown in Figs. 14(b) and 14(c), to suppress the fluctuation of SCEs (both the normalized σSS and σDIBL are with 7%) induced by the WKF, the device with vertical channel of channel fin angle between 85° and 90° could be adopted.

IV. CONCLUSIONS

In summary, we have studied the impact of T_{cap} and x of $In_{1-x}Ga_xAs$ capping layer on 14-nm $In_{1-x}Ga_xAs$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ / InP trigate MOSFET. For the given specifications of SS < 72 mV/dec, DIBL < 55 mV/V, and $I_{on}/I_{off} > 1.7x10^6$ with V_{th} = 160 mV, the device with a 4-nm-thick $In_{0.68}Ga_{0.32}As$ channel capping layer can provide optimal characteristic for high-performance device applications. For the optimized device configuration, the simulation results suggest that the smaller the grain size is, the more the WKF can be suppressed. As a result, to effectively suppress the WKF-induced DC characteristic fluctuation, the averaged grain size should be smaller than 4x4 nm^2 and the channel fin angle could be between 85° and 90°.

In Table V, we do compare the recent works about the III-V transistors with various InGaAs channels with our results. We have achieved the larger on-/off-state current ratio, the higher cut-off frequency, and the lower standard deviations of SCE parameters. We are currently studying the III-V MOSFET device with high aspect ratio (fin height / fin width) to obtain the better device characteristics including fluctuation suppression.

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