Co Si x thermal stability on narrow-width polysilicon resistors

Yen-Ming Chen, George C. Tu, Ying-Lang Wang, Gwo-Jen Hwang, and Cheng-Yao Lo

Citation: Journal of Vacuum Science & Technology B **24**, 83 (2006); doi: 10.1116/1.2141626
View online: http://dx.doi.org/10.1116/1.2141626
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/24/1?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

$CoSi_x$ thermal stability on narrow-width polysilicon resistors

Yen-Ming Chen and George C. Tu
Department of Materials Science and Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China

Ying-Lang Wang[a] and Gwo-Jen Hwang
College of Science and Engineering, National University of Tainan, Tainan, Taiwan

Cheng-Yao Lo
Department of Materials Science and Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China

(Received 15 March 2005; accepted 31 October 2005; published 12 January 2006)

In this study, the thermal stability of polysilicon lines with various widths and different dopant types in 90-nm processes is investigated. The thermal behavior of silicides formed on N+ polyresistors and P+ polyresistors is very different. The worst thermal stability is found on the narrower N+ polyresistors, while an abnormal thermal behavior is observed on P+ polyresistors. This anomalous thermal-stability change with different drawn linewidths of P+ polyresistors is related to the grain-size distribution and the actual polyresistor linewidth. Also, it is interesting to find that the voids formed in P+ polyresistors lead to a stepped increase in sheet resistance. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2141626]

I. INTRODUCTION

Cobalt silicide is widely used on polycrystalline Si (poly-Si) as low-resistance gate electrodes and local interconnects because 0.18-μm node cobalt silicide has low bulk resistivity ($\sim$18 $\mu\Omega$ cm), excellent chemical stability, and less linewidth dependence compared to titanium silicide.[1,2] However, thermal stability is a concern for the application of cobalt silicide in actual devices. The thermal stability of silicide on poly-Si and its effect on device performance have been studied extensively.[3] In previous studies, the thermal stability of silicide via long-time or high-temperature thermal testing has been investigated[4–6] and some groups have used a force balance model to explain silicide agglomeration.[7–9] This study focuses on the effect of different linewidths and dopant types on the thermal stability of poly-Si lines in 90-nm processes. It is found that the narrow poly-Si lines defined in 90-nm processes induce poor thermal stability and high sheet resistance. Both the linewidth and the doping type determine the thermal stability of narrow poly-Si lines.

II. EXPERIMENT

Boron-doped, *p*-type Si wafers with resistivity of 10 Ω cm and with a (001) orientation were used as substrates and the 90-nm process was applied for this study. 100-μm-long poly-Si lines with linewidths ranging from 2000 to 90 nm were fabricated to evaluate the thermal stability of silicided polysilicon. The N+ source/drain and P+ source/drain were formed by As/P and BF_2/B implant, respectively. Then rapid thermal annealing (RTA) was used to activate the implant dose. After hydrofluoric acid (HF) treatment, Ti capping (Co/Ti) materials were sputtered on silicon wafers, followed by the first RTA treatment. Selective etching was performed after the first RTA to remove unreacted Ti and Co. Next, the second RTA was performed at 850 °C/30 s to form low-resistivity silicide. After the interlayer dielectric layer was deposited by chemical-vapor deposition, lithography and dry etching were performed for contact-layer definition. Finally, copper metallization was performed. The sheet resistance of silicided N+ and P+ polyresistors with various linewidths (see Fig. 1) was measured by HP4071 semiconductor electrical parameter analyzer. The emission microscope (EMMI) was used for positioning failure sites and transmission electron microscope (TEM) was used to examine silicide thickness, poly-Si physical linewidth, and the agglomeration phenomenon.

III. RESULTS AND DISCUSSION

In previous studies, the thermal stability of silicide has usually been examined by long-term thermal stress and analyzed by resistance variation.[5,10–12] These researches concluded that narrow line and large silicide grain degraded the thermal stability. Figure 2 shows our measured sheet-resistance variation of N+ and P+ poly-Si lines with different widths. These lines were fabricated by the Ti capping process. The larger sheet-resistance variation indicates poor thermal stability. It is usually thought that the narrower the

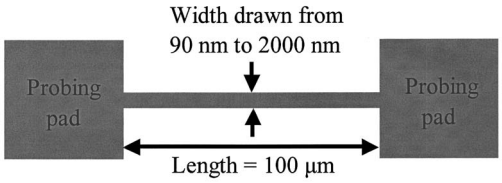

FIG. 1. Polyresistor test structure studied in this research.

[a]Author to whom correspondence should be addressed; electronic mail: ylwang@tsmc.com

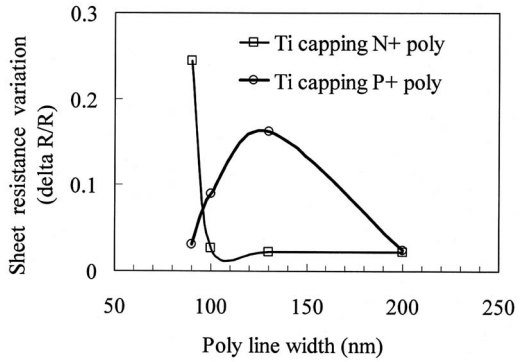

FIG. 2. Sheet-resistance variation of polyresistors with different widths.

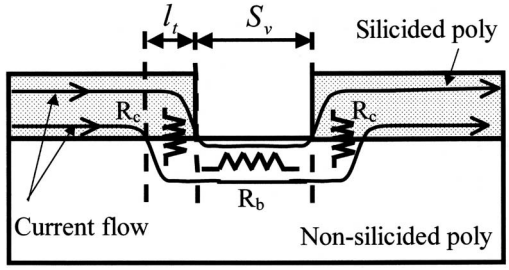

FIG. 4. Illustration for the current flow through the polyresistor.

poly-Si line, the worse the thermal stability. In this study, the thermal behavior of all N+ polyresistors is consistent with the common result, as shown in Fig. 1. However, the P+ polyresistors have anomalous behavior that contradicts common belief. P+ poly-Si lines fabricated by the Ti capping process and polyresistors with a linewidth of 130 nm have the largest variation in the sheet resistance, rather than the narrowest line. In order to verify the thermal behavior of P+ polyresistors, the second RTA with various temperatures and process times was investigated. Figure 3 displays the cumulative plots for the sheet resistance of P+ poly-Si lines. The spread of the sheet resistance increases as the RTA temperature and process time increase. In particular, the sheet resistance increases by 5 Ω/sq for each jump for the P+ polyresistor processed by 850 °C/120 s. EMMI images in the inset of Fig. 3 show that one hot spot is found on the 5-Ω/sq-increased sample and two hot spots are found on the 10-Ω/sq-increased sample, indicating that the increase in the sheet resistance is determined by the number of disconnections that occurred on the narrow polyresistors. Figure 4 plots a schematic to explain the increase in the sheet resistance. The total sheet resistance of silicide (R) is the sum of R_a, R_b, and R_a', where R_a and R_a' are the resistances of a transitional region where current will flow from the silicide region to the nonsilicide region. R_b is the resistance of nonsilicided polyresistor where the length is equivalent with the void. It is assumed that R_a is equal to R_a' due to the same resistor length in these two transitional regions, so $R=2R_a+R_b$. R_a can be further divided into silicide resistor R_1, silicide to poly-Si contact resistance R_c, and poly-Si resistor R_2. It was found by assuming $R_1+R_c=R_2$ or

$$R_{S_1}\left(\frac{L}{w}\right)+\left(\frac{\rho_c}{wL}\right)=R_{S_2}\left(\frac{L}{w}\right), \tag{1}$$

where ρ_c is the specific contact resistance of silicide to poly-Si interface, R_{s_1} is the sheet resistance of silicide, and R_{s_2} is the sheet resistance of nonsilicided portion of P+ polysilicon. With the measured $\rho_c=50\ \Omega\ \mu m^2$, $R_{s_1}=9.6\ \Omega$/sq, and $R_{s_2}=800\ \Omega$/sq $L=0.25\ \mu$m and $R_c=1525\ \Omega$ are obtained and the increase in the total resistance is 4.8 Ω/sq, which is consistent with the observation in Fig. 2. The TEM top view of 130-nm P+ polyresistors is shown in Fig. 5. It is found that the voids on 130-nm P+ polyresistors are almost as large as the linewidth and these voids have a similar size. These voids may lead to the stepped increase in the sheet resistance. The result is very different from that of the narrow N+ polyresistors. Figure 6 shows the cumulative plot for the sheet resistance of N+ polyresistors with different drawn widths. When the poly-Si linewidth shrinks to 90 nm, the spread of the sheet-resistance distribution for N+ polyresistors becomes worse. The TEM plane view of the 90-nm sample with high sheet resistance is shown in Fig. 7. Unlike the case in 130-nm P+ polylines, the voids randomly distributed on the 90-nm N+ polyline are much smaller than the linewidth, resulting in a gradual increase in the sheet resistance, rather than a stepped increase as in the P+ polylines.

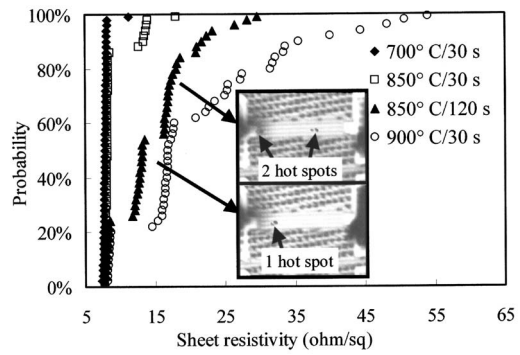

FIG. 3. Sheet-resistance distribution for P+ polyresistor (drawn width =130 nm). The insets are the EMMI images of high-resistance sites.

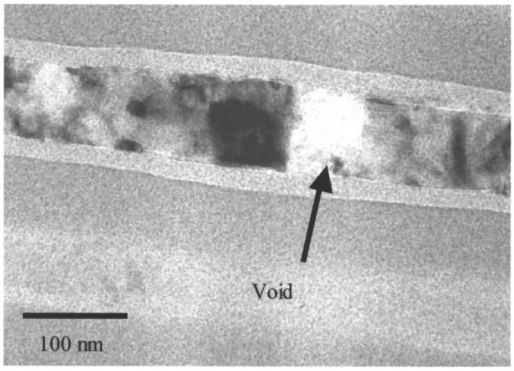

FIG. 5. TEM plan view for the high-resistance site on P+ polyresistor (drawn width=130 nm).

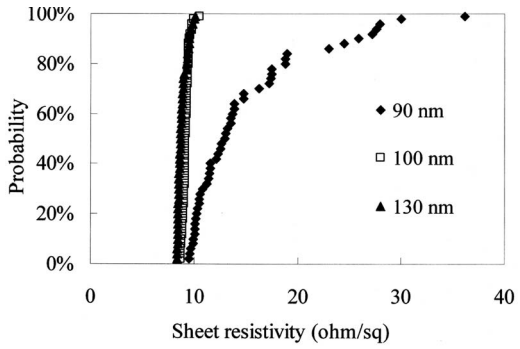

FIG. 6. Sheet-resistance distribution for different drawn widths of N+ polyresistors.

The different void size that occurred on N+ and P+ polyresistors results in the different thermal behaviors that are related to the grain size on poly-Si lines. The TEM plane views of Figs. 8(a)–8(c) show the grain-size distribution on N+ polyresistors with different widths. As shown in Fig. 8(a), a large spread in the grain-size distribution is clearly observed on the 2000-nm drawn poly-Si line. The grain dimension ranges from 30 to 170 nm, with an average value of 100 nm. For the 130-nm drawn poly-Si line, the actual linewidth is about 83 nm. The grain distribution on this line is not a normal distribution like that on the 2000-nm-width polyline. The maximum grain size is constrained by the actual linewidth. The TEM plane view also shows that the grain size is as large as the linewidth and also shows the quasibamboo-like microstructure, as can be seen in Fig. 9. As the linewidth shrinks, the maximum grain size on narrow polylines is limited by the linewidth and forms the quasibamboo microstructure where either a single grain or two grains coexist in the linewidth.[13] For the 90-nm drawn polyline, the maximum grain size is only about 50 nm, which is consistent with the actual linewidth. Figures 8(b) and 8(c) show that there are still small portions of grains that are smaller than the actual linewidth distributed around the line edge. The disappearance of these grains results in an increase in the sheet resistance, as can be seen in Fig. 7. The grain size of *p*-type polyresistors is shown in Figs. 10(a)–10(c). The

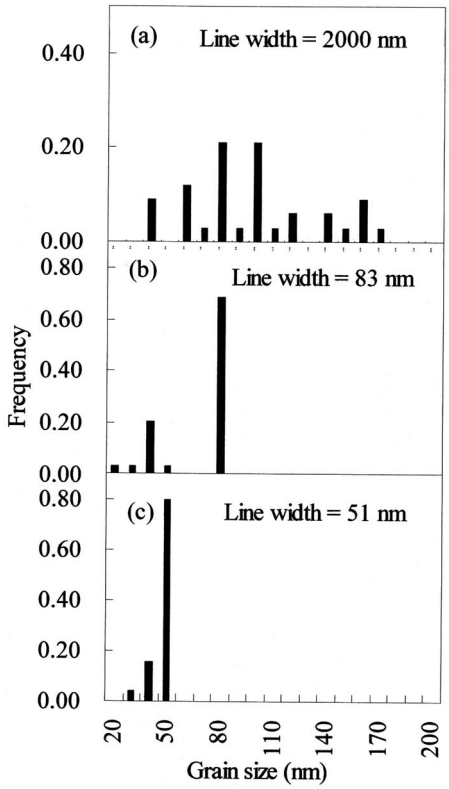

FIG. 8. Grain-size distribution for N+ polyresistors.

grain-size distribution in 2000-nm drawn polylines is similar to that in *n*-type polylines. Broadening grain-size distribution is found and it ranges from 40 to 130 nm, with an average value of 80 nm. For the 130-nm drawn polyline, the actual width is about 88 nm. This is close to the mean grain size in the 2000-nm drawn polyline, where grain growth has no constraint. The grain-size distribution in the 130-nm drawn polyline ranges from 40 to about 80 nm. The majority are around 60 nm. As shown in Fig. 5, the grain size similar to

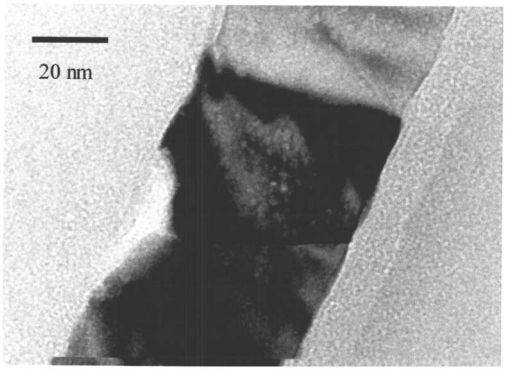

FIG. 7. TEM plan view for the high-resistance site on N+ polyresistor (drawn width=90 nm).

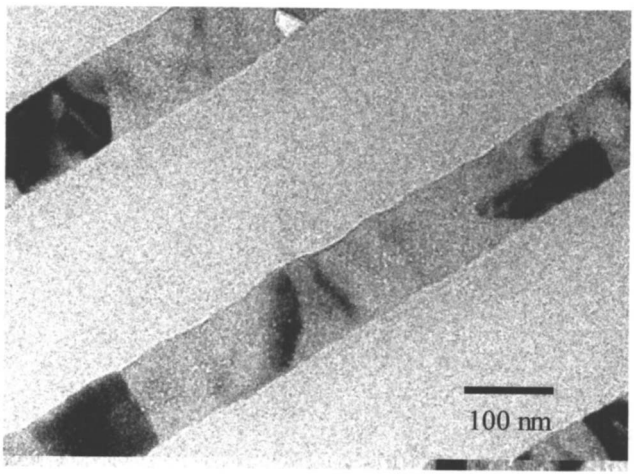

FIG. 9. TEM plan view for the high-resistance site on P+ polyresistor (drawn width=130 nm).

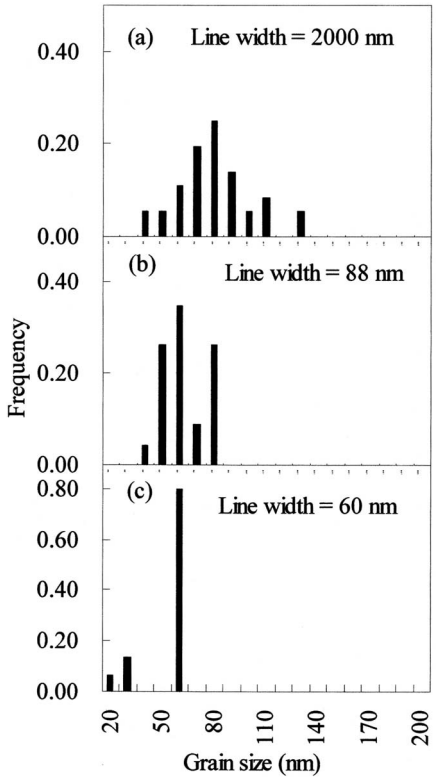

FIG. 10. Grain-size distribution for P+ polyresistors.

the linewidth is believed to leave a void behind while grains merge with each other during the thermal cycle. The grain size in the narrower polyline is further constrained when the linewidth is narrower than the unconstrained grain size. The 90-nm drawn P+ polyresistor thus results in similar thermal stability to the *n*-type polyline and does not show the similar thermal stability to the 130-nm drawn *p*-type polyline because the less the grain boundary exists, the less the probability for Co/Si diffusion. The degradation of silicide is strongly affected by the silicide thickness and, for the same thickness, the microstructure of the silicide impacts thermal stability significantly. The underlying silicon substrate has the greatest influence on the microstructure of the silicide. Consequently, it influences the thermal stability of the silicide. The polyresistor grain size for nonsilicide N+ and P+ polyresistors were measured on blanket wafers. The grain sizes for N+ and P+ polyresistors were about 120 and 78 nm, respectively. These sizes are similar to those of the formed silicide. A similar observation for the underlayer morphology was also made in a previous research.[14] The dopants implanted in the poly-Si layer have a great influence on thermal stability property.[15,16]

IV. CONCLUSIONS

The thermal stability of polysilicide formed on poly-Si lines with different widths and dopant types was investigated in this study. As was concluded in previous studies,[5,10–12] large silicide grain size and narrow poly linewidth degrade the resistance to agglomeration and lead to poor thermal stability. In this study, the thermal behavior of silicide formed on N+ polyresistor agrees with that previous observation. However, a special digitalized sheet-resistance increase is observed on P+ polyresistors. The voids on the specific linewidth of P+ polyresistors result in this digitalized sheet-resistance increase. This anomalous thermal-stability change in the P+ polyresistors with different linewidths is related to the grain-size distribution and the actual polyresistor linewidth. The substrate plays a significant role in the silicide grain size, which then impacts the thermal stability in the cobalt-silicide process.

ACKNOWLEDGMENT

This study is supported in part by the National Science Council of the Republic of China under Contract Nos. NSC-93-2524-S-260-001 and NSC-93-2524-S-009-004-EC3.

[1]T. P. Chow and A. J. Steckl, IEEE Trans. Electron Devices **45**, 1480 (1983).
[2]M. A. Nicolet and S. S. Lau, *VLSI Electronics Microstructure Science* (Academic, New York, 1993), Vol. 6, p. 329.
[3]E. G. Colgan, J. P. Gambino, and Q. Z. Hong, Mater. Sci. Eng., R. **16**, 43 (1996).
[4]T. Ohguro, M. Saito, E. Morifuji, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, IEEE Trans. Electron Devices **47**, 2208 (2000).
[5]A. Alberti, F. La Via, V. Raineri, and E. Rimini, J. Appl. Phys. **86**, 3089 (1999).
[6]J. P. Gambino, E. G. Colgan, A. G. Domenicucci, and B. Cunningham, J. Electrochem. Soc. **145**, 1384 (1998).
[7]A. Alberti, F. La Via, S. Ravesi, and E. Rimini, Appl. Phys. Lett. **79**, 3419 (2001).
[8]T. P. Nolan, R. Sinclair, and R. Beyers, J. Appl. Phys. **71**, 720 (1999).
[9]Z. G. Xiao, G. A. Rozgonyi, C. A. Canovai, and C. M. Osburn, Materials Research Society Symposium Proceedings 202 (Materials Research Society, Pittsburgh, 1991), p. 101.
[10]Q. F. Wang, K. Maex, S. Kubicek, R. Jonckheere, B. Kerkwijk, R. Verbeeck, S. Biesemans, and K. De Meyer, Proceedings of Symposium on VLSI Technology, Kyoto, 1995 (unpublished), p. 17.
[11]M. C. Poon, F. Deng, H. Wong, M. Chen, J. K. O. Sin, S. S. Lau, C. H. Ho, and P. G. Han, Proceedings of Symposium on Electron Device Meeting, Hong Kong, 1997 (unpublished), p. 54.
[12]N. S. Kim, H. S. Cha, N. K. Sung, H. H. Ryu, K. S. Youn, and W. G. Lee, J. Vac. Sci. Technol. A **20**, 1171 (2002).
[13]L. Arnaud, G. Tartavel, T. Berger, D. Mariolle, Y. Gobil, and I. Touet, Proceedings of Symposium on Reliability Physics, 1999 (unpublished), p. 263.
[14]W. M. Chen, S. K. Banerjee, and J. C. Lee, Appl. Phys. Lett. **64**, 1505 (1994).
[15]Q. F. Wang, J. Y. Tsai, C. M. Osburn, R. Chapman, and G. E. McGuire, Appl. Phys. Lett. **61**, 2920 (1992).
[16]B. S. Chen and M. C. Chen, J. Appl. Phys. **74**, 1035 (1993).