1.3-μm InAs–InGaAs Quantum-Dot Vertical-Cavity Surface-Emitting Laser With Fully Doped DBRs Grown by MBE

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***Abstract*—We report InAs–InGaAs quantum-dot vertical-cavity surface-emitting lasers (VCSELs) grown by molecular beam epitaxy with fully doped n- and p-doped AlGaAs distributed Bragg reflectors and including an AlAs layer to form a current and waveguiding aperture. The metal contacts are deposited on a topmost p^+-GaAs contact layer and on the bottom surface of the n^+-GaAs substrate. This conventional selectively oxidized top-emitting device configuration avoids the added complexity of fabricating intracavity or coplanar ohmic contacts. The VCSELs operate continuous-wave at room temperature with peak output powers of 0.33 mW and differential slope efficiencies up to 0.23 W/A. The peak lasing wavelengths are near 1.275 μm, with a sidemode suppression ratio of 28 dB.**

***Index Terms*—Fully doped distributed Bragg reflector (DBR), InAs quantum dot (QD), molecular beam epitaxy (MBE), vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

THE development of GaAs-based vertical-cavity surface-emitting lasers (VCSELs) emitting in the 1.3-μm range remains a fruitful area of laser diode research, offering significant growth and fabrication challenges but also a large variety of possible epitaxial material combinations to investigate. Recently reported results revealed the self-assembled InAs–InGaAs quantum dots (QDs) can be used to fabricate 1.3-μm GaAs-based LDs and VCSELs [1], [2]. Oxide-confined (OC-) VCSELs, wherein lateral oxidation is used to form current and optical confinement apertures, need to be etched to expose the high Al composition AlGaAs layer close to the active region. The most common physical geometries for OC-VCSEL fabrication are the intracavity metal contacted structure [2] and the mesa structure planarized by a spin-on glass or polyimide [3]. Typically the intracavity contacting method is used for molecular beam epitaxy (MBE)-grown VCSEL fabrication [2], because the distributed Bragg reflectors (DBRs) are commonly undoped to avoid free-carrier absorption and the need to compositionally grade the DBR heterointerfaces. However, the etching process required to form mesas for the placement of intracavity contacts is extremely critical. During each of two mesa fabrication steps, the etching depth must be controlled to stop exactly on the thin heavily doped contact layers adjacent to the microcavity. The etching process tolerance is typically too small to obtain a high yield, even if the etch is performed with *in situ* reflectance monitoring. The resultant nonplanar configuration also complicates the subsequent metallization process. As a result, the device yields of intracavity contacted OC-VCSELs are lower.

In this letter, we report a near-planar processing method for InAs QD OC-VCSELs that is expected to be readily adaptable to a high volume production line with high device yields and state-of-the-art QD VCSEL performance. With this fabrication technique, we herein demonstrate GaAs-based QD VCSELs that operate continuous wave (CW) at room temperature (RT) with peak output powers exceeding 1/3 mW and up to 23% peak differential slope efficiencies.

II. Device Structure and Fabrication

The InAs QD OC-VCSEL wafer used in this experiment was prepared by solid-source MBE and grown on an (001)-oriented n-GaAs substrate. The active region consists nine sheets of InAs pyramidal islands formed by a two monolayer-thick InAs deposition, and embedded in an 8-nm-thick $In_{0.15}Ga_{0.85}As$ QW overgrowth layer separated by 30-nm-thick GaAs barrier layers. The nine sheets of InAs–InGaAs QDs are divided into three groups and each group consists of three closely spaced sheets of dots. For the purpose of placing all the three groups of QD layers exactly at antinode positions of the resonant standing wave field to obtain higher optical gain, the microcavity optical length is elongated to 2λ to sustain at least three normalized squared electric-field antinode positions inside the microcavity. The n- and p-doped DBRs are composed of $\lambda/4$-thick GaAs–$Al_{0.9}Ga_{0.1}As$ layers with digital interface grading to help reduce each VCSELs series resistance. The n- and p-doped DBRs consisted of 33.5 and 27 periods, respectively, and the calculated reflectance R for each mirror greater than 0.99. The DBR material layers are δ-doped with Si at

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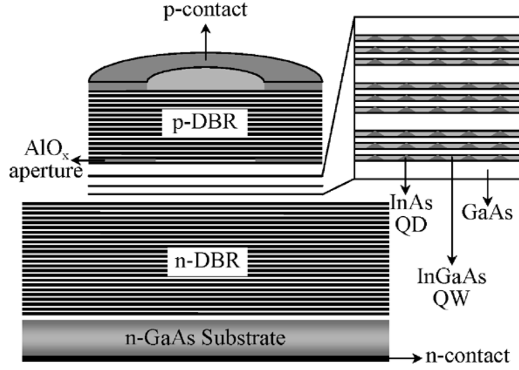

Fig. 1. Schematic illustration of the OC QD VCSEL with fully doped DBRs grown by MBE. The 2λ-thick active region consists of nine sheets of InAs QDs embedded in 8-nm-thick InGaAs QWs.

$N_D \sim 5 \times 10^{18}$ cm^{-3} and with C at $N_A \sim 5 \times 10^{18}$ cm^{-3} adjacent to the digitally graded interfaces, respectively. The doping level of each DBR periods was reduced to about 2×10^{17} cm^{-3} for the purpose of reducing free-carrier absorption. A 20-nm-thick AlAs layer was placed at the interface between the first p-DBR quarter-wave layer and the microcavity active region. This AlAs layer is later selectively oxidized in water vapor to serve as both a current and waveguiding aperture. A schematic illustration of a fabricated QD VCSEL is given in Fig. 1.

After MBE growth, a 1.7-μm-thick SiN_x layer was deposited onto the wafer sample surface by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. This SiN_x layer was used as a hard mask for a subsequent dry etching step. Conventional photolithography and reactive ion etching (RIE) with *in situ* reflectance monitoring were then performed to define a mesa pattern on the SiN_x. Trenched mesa etching was then performed using RIE to transfer the pattern of the SiN_x hard mask onto the wafer sample. The shape of the trench is not a thick-line letter "O" (i.e., an annulus) but rather a thick-line letter "C" that is almost a closed circle. The etched depth of the trench was carefully controlled to expose the 20-nm-thick AlAs layer. The total etching depth was 6.5 μm. Selective wet oxidation was then preformed at 400 °C in steam. The mesa diameter of the oxidized VCSELs was 22 μm with a 12-μm oxide aperture. After the removal of the residual SiN_x, we used PECVD to deposit a 150-nm-thick SiO_2 layer onto the wafer samples for device passivation. This passivation layer was then partially etched for contact window formation. Subsequently Ti(30 nm)/Pt(50 nm)/Au(200 nm) was deposited onto the topmost heavily doped $(N_A \sim 2 \times 10^{19}$ cm$^{-3})$ p^+-GaAs to serve as p-contact metal. After substrate lapping down to 200 μm, AuGe(50 nm)/Ni(20 nm)/Au(350 nm) was deposited onto the backside of the samples to serve as the n-contact metal. The processing technique and resultant device appearance is almost identical to the metal–organic vapor phase epitaxy (MOVPE) grown 850-nm OC-VCSEL we previously reported [4], except the trenched mesa etching for our QD VCSELs is deeper. Note that our process includes neither the intracavity contacts nor the polyimide planarization.

Initially the measured light output power (L) from the QD VCSEL was lower than expected because the power reflectance (R) of the top DBR was quite high. Therefore, we removed the top three periods of the p-DBR (including the p^+-GaAs contact layer) to slightly reduce the reflectivity and fabricated a new set of devices. As a result, the top and bottom DBRs then consisted of 24 and 33.5 periods, respectively. To compensate for the reduce doping in the topmost p-DBR layer after the etching of the DBR, we first performed a Zn diffusion at 570 °C for 8 min across the entire wafer sample surface in an As_4 overpressure prior to device fabrication. The shallow Zn diffusion serves to reconstruct the p^+-GaAs topmost ohmic contact layer.

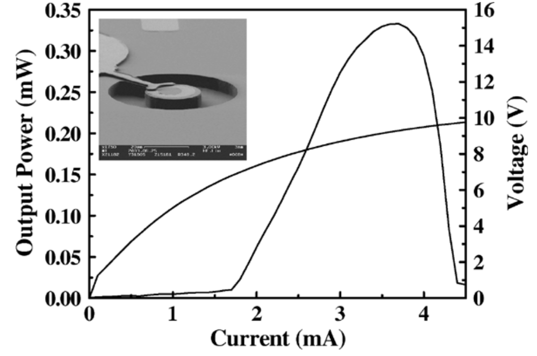

Fig. 2. L–I–V characteristics of the InAs QD VCSEL. The turn-on voltage is 1.26 V and I_{th} is 1.7 mA with 0.33-mW maximum output power. The inset shows the SEM photograph of the fabricated device.

III. Results and Discussion

The measured CW, RT light output power (L) and applied voltage (V) versus current (I) characteristic of one of our typical QD VCSELs is given in Fig. 2. The inset in Fig. 2 is a tilted micrograph of a fabricated device as taken by a scanning electron microscope (SEM). The mesa diameter is 22 μm and the trench width is 15 μm. The internal diameter of the VCSELs top metal ring contact is 10 μm and the bonding pad diameter is 85 μm, respectively. The large bonding pad connects directly to the VCSELs top metal ring contact by lying flush on the wafer surface and across the section of the trench that is not etched. Thus, our process does not require the formation of an air-bridge.

As extracted from the data in Fig. 2, the turn-on voltage of the fabricated device is 1.26 V, the threshold voltage $(V_{\rm th})$ is 6.9 V, and the threshold current $(I_{\rm th})$ is about 1.7 mA. Since the circular current aperture diameter is 12 μm, the corresponding threshold current density is 1.5 kA/cm^2. The maximum output power is 0.33 mW with a differential slope efficiency of 0.23 W/A. Our devices exhibit large series resistance of about 0.8 to 1.3 $k\Omega$ within the operational range, which is approximately four times larger than previously reported QD VCSELs with intracavity metal contacts [5]. We attribute this large series resistance to significant current heating due to unoptimized DBR interface grading and Zn diffusion conditions. Moreover, this additional Zn diffusion increases absorptive and scattering losses. These device losses conspire to cause an early rollover in the L–I curve and thus serve to limit the peak output power. The lasing spectrum of the fabricated device at a drive current of 3.2 mA is shown in Fig. 3. The peak lasing wavelength is 1.275 μm. As expected, this peak emission wavelength is coincident with the peak emission wavelength of our previously reported resonant cavity light-emitting diodes containing

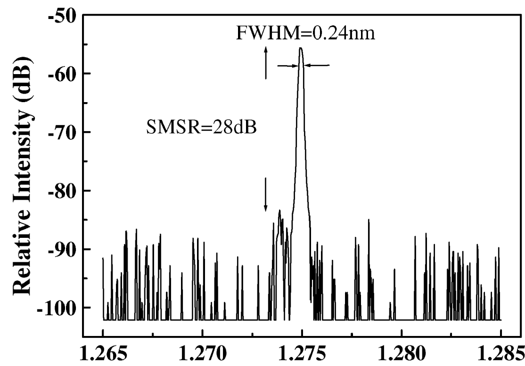

Fig. 3. Lasing spectrum of the InAs QD VCSEL with 3.2-mA drive current shows the peak wavelength is 1.275 μm and SMSR is 28 dB.

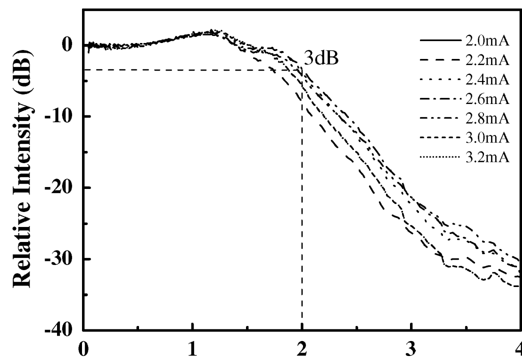

Fig. 4. Modulation response of the InAs QD VCSEL with additional proton implantation. The maximum 3-dB modulation bandwidth is 2 GHz.

similar active regions [6]. It is clear from the data in Fig. 3 that the fabricated QD VCSELs operate in a single mode with a sidemode suppression ratio (SMSR) of 28 dB and a full-width at half-maximum of 0.24 nm.

To improve the high-speed modulation performance of our QD VCSELs, we implanted protons to decrease the parasitic capacitance [7]. Protons were implanted at energies of 200, 300, and 400 keV with a dose of 5×10^{14} cm^{-2} at each of these energies. The implanted aperture lay over the oxide aperture and the diameter is also 12 μm. According to the stopping and range of ions in matter (SRIM) simulation results, the peak implant depth is about 3.57 μm from the surface to keep from damaging the active region. The measured modulation response of the implanted QD OC-VCSEL at several bias currents from 2.0 to 3.2 mA is shown in Fig. 4. The 3-dB frequency $(f_{3\text{ dB}})$ at a bias current of 2.6 mA is 2 GHz. Fig. 5 is a plot of the 3-dB frequency versus $(I - I_{\text{th}})^{1/2}$. From the slope of the data in Fig. 5, the modulation current efficiency factor (MCEF) can be extracted. The MCEF is constant at about 2.5 GHz/(mA)$^{1/2}$ for current drive currents between about 1.7 to 2.6 mA. These results indicate that our QD OC-VCSELs have great potential to be modulated at data rates up to 2.5 Gigabit per second (Gb/s), and thus, our devices should meet the OC-48 standard.

IV. Conclusion

We have reported one of the first demonstrations of InAs–InGaAs QDs OC-VCSEL with fully doped DBRs grown by MBE. The device has been successfully fabricated and can be operated

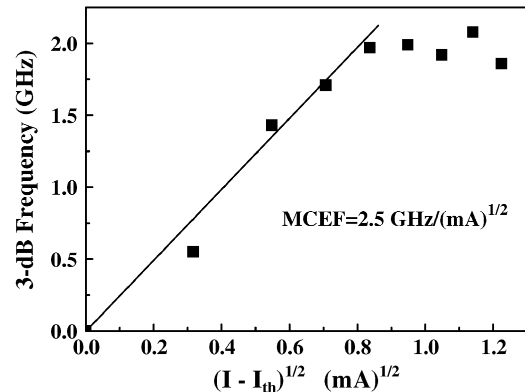

Fig. 5. MCEF of the fabricated device with additional implantation is 2.5 GHz/(mA)$^{1/2}$.

CW at RT. Neither intracavity coplanar contacts nor polyimide planarization has been used for the fabrication. The processing technology is identical to that used for MOVPE-grown 850-nm OC-VCSELs, which is a well suited approach for large-scale manufacturing with high yields. The I_{th} of the fabricated device is 1.7 mA and the peak output power is 0.33 mW. The QD VCSELs lase at 1.275 μm and possess a single-mode operation ability with 28-dB SMSR. The modulation bandwidth of the device after implantation is 2 GHz. We expect that with further device optimization to reduce series resistance, to reduce absorptive losses, and to improve thermal management, we will achieve output powers up to about 1 mW with differential slope efficiencies exceeding 0.4 W/A and modulation bandwidths exceeding 4 GHz.

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