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Effects of Postdeposition Annealing on the Characteristics of HfO_xN_y Dielectrics on Germanium and Silicon Substrates

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We have systematically investigated the impact that postdeposition annealing (PDA) has on the physical and electrical properties of HfO_xN_y thin films sputtered on Ge and Si substrates. These two substrates display contrasting metal-oxide-semiconductor characteristics that we attribute to the different compositions of their interface layers (ILs). We observed an increased GeO_2 incorporation into the HfO_xN_y dielectric and severe volatilization of the IL on Ge after higher PDA processing. These undesired phenomena in the HfO_xN_y/Ge gate stacks may be responsible for their different electrical properties with respect to those of the HfO_xN_y/Si gate stacks, i.e., a further scaling of the capacitance-equivalent thickness, a significant presence of fixed positive charges and electron-trapping sites, and a degradation of dielectric reliability. In addition, the anomalous low-frequency-like behavior of the high-frequency capacitance–voltage curves in inversion for the Ge capacitors was predicted from theoretical calculations.
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The rapid advancement of complementary metal oxide semiconductor (MOS) integrated circuit technologies during the past few decades has forced the Si-based microelectronics industry to face several huge technological challenges and to test some theoretical limits. Consequently, many novel device structures and materials have been proposed and are being explored eagerly in an effort to alleviate the tremendous scaling pressure required to improve device performances. High-permittivity (high-*k*) materials will probably be introduced as alternative gate dielectrics, in place of ultrathin conventional SiO_2 or oxynitrides, in light of leakage concerns and reliability issues. Meanwhile, substrate engineering, e.g., pseudomorphic SiGe channels grown on the Si substrates for p-type field effect transistors (FETs)[1] and strained Si channels on the relaxed graded SiGe buffer layers for n-type FETs,[2] is being pursued to enhance the carrier mobility in the channel also. Inspired by the advanced progress in the development of high-*k* dielectrics in Si-based metal oxide semiconductor field effect transistor (MOSFET) applications, increasingly attention is being focused on the feasibility of integrating high-*k* gate dielectrics with Ge because of its intrinsically higher mobility than Si. To date, the superior electrical properties of several high-*k* metal oxides deposited on the Ge substrate have been demonstrated, including ZrO_2,[3] HfO_2,[4,5] and Al_2O_3.[6] It has been suggested that surface pretreatment with SiH_4[7] or NH_3[8] prior to deposition of these metal oxides is required to obtain high-quality gate dielectrics on Ge substrates. In this paper, we describe our study into the physical and electrical characteristics of sputtered HfO_xN_y thin films deposited onto bulk Ge and conventional Si substrates. The incorporation of nitrogen into HfO_2 gate dielectrics cannot only increase the crystallization temperature but also strengthen immunity toward oxygen diffusion and resistance toward boron penetration without lowering the dielectric constant.[9] Apart from the poor interface quality that results from the presence of nitrogen, HfO_xN_y films are expected to have advantages over HfO_2 in regard to some other essential properties. HfO_xN_y has improved thermal stability with respect to those of surface-nitrided and top-nitrided HfO_2 because the nitrogen atoms exist in the bulk dielectric and at the dielectric-Si interface. Several investigators have reported Si-based MOSFETs possessing Hf-oxynitride gate dielectrics.[9-11] Nevertheless, fundamental differences exist between the thermochemical properties of not only the Ge and Si substrates but also their oxides.[12] Clearly, the implication is that each interface layer (IL) formation process, as well as the nature of the interactions at the surface, might possess quite different features during post-thermal treatment. Indeed, the starting surface of these two substrates is a critical parameter in determining both the final thickness of a HfO_2 film grown through physical vapor deposition (PVD) and the IL formed.[13] The bulk properties of high-*k* films deposited on Ge substrates also might be different from those on Si substrates. This study was an attempt to clarify these concerns through a comprehensive comparison of the physical and electrical characteristics of HfO_xN_y/Ge and HfO_xN_y/Si systems; in this paper we discuss the impact that postdeposition annealing (PDA) has on both the high-*k* dielectric and the interfacial compositions on Ge and Si substrates.

Experimental

(100) Ga-doped p-type Ge wafers having a resistivity of 25–29 Ω cm and (100) p-type Si wafers having a resistivity of 1–10 Ω cm were used. All the wafers were subjected to a cleaning process involving several cycles of sequential rinsing with deionized (DI) water followed by dipping in HF acid solution (DI water/HF, 1:30). After N_2 drying, HfN thin films were first deposited through reactive sputtering in an $Ar + N_2$ ambient $[N_2/Ar + N_2 = 0.33]$ with a 99.9% pure Hf target. During deposition, the chamber pressure was 7.6 mTorr and the sputtering power was 150 W. In an attempt to suppress any additional oxidation, which can help to minimize the thickness of IL, the following PDA was performed to convert HfN into HfO_xN_y in an N_2 ambient rather than an O_2 ambient.[9] The samples were split into many groups so that PDA could be performed at different temperatures (400, 500, and 600°C) and various durations (1, 3, and 5 min) to study their impact on the interfacial characteristics of the HfO_xN_y gate dielectrics on both the Ge and Si substrates. Next, a 1000 Å thick layer of platinum (Pt) was deposited using electron-beam evaporation through a shadow mask to pattern the capacitor electrode. Postmetallization annealing (PMA) was then performed at 400°C for 30 s. The capacitance area was evaluated through optical microscopy of the circular capacitor dots. Finally, aluminum (Al) was deposited on the back side of the wafer, followed by sintering in the forming gas (N_2/H_2, 90:10) at 300°C for 30 min.

High-resolution transmission electron microscopy (HRTEM) was employed to characterize the thicknesses and interfacial structures of the Hf-oxynitride films on both the Ge and Si substrates before and after PDA. The compositions and chemical bondings of the HfO_xN_y films were analyzed using angle-resolved X-ray photoelectron spectroscopy (AR-XPS) with an Al Kα radiation source operating at 1486.6 eV for excitation. Photoelectrons were collected at two take-off angles (30 and 60° with respect to the surface horizontal) and the

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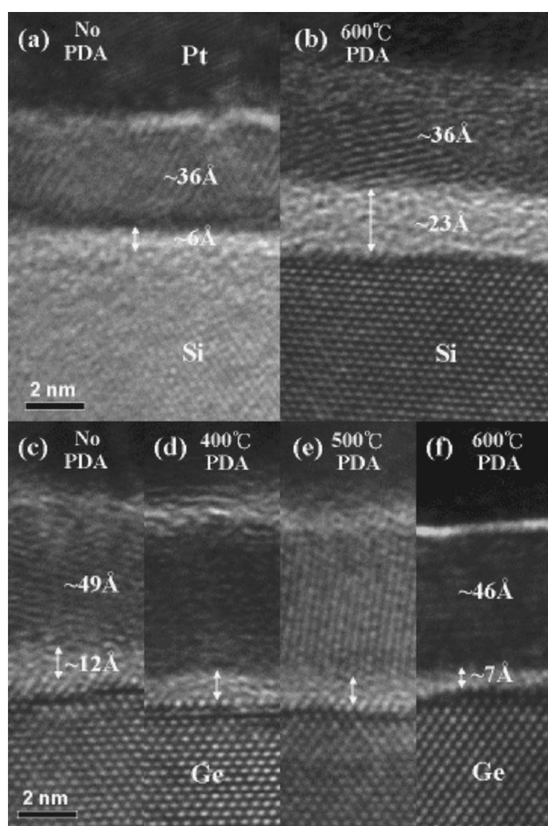

Figure 1. HRTEM images of sputtered HfO_xN_y thin films on (a, b) Si and (c–f) Ge substrates before and after PDA. (a) Si: No PDA; (b) Si: PDA at 600°C; (c) Ge: no PDA; (d) Ge: PDA at 400°C; (e) Ge: PDA at 500°C; and (f) Ge: PDA at 600°C. The PDA time for all annealed samples was 5 min.

binding energy was calibrated from the Pt $4f_{7/2}$ peak at 71.20 eV. The element depth profiles of these films were analyzed through Auger electron spectroscopy (AES) using Ar^+ ion sputtering; the *LM*2 and *MN*2 transitions were used for germanium and hafnium, respectively, while *KL*1 transition was used for both nitrogen and oxygen. For characterization of electrical properties, capacitance-voltage (C-V) and conductance-voltage (G-V) curves were measured using an HP4284 LCR meter. The gate leakage characteristics were measured using a Keithley 4200 semiconductor analyzer system.

Results and Discussion

Physical characterization.— HRTEM images.— Figure 1a and b displays cross-sectional HRTEM images of the HfO_xN_y-sputtered films on the Si substrates before and after N_2 PDA. As expected, an additional IL growth appeared on the Si substrate after annealing at 600°C for 5 min. By contrast, we observed that the thickness of the IL between the HfO_xN_y dielectric and the Ge substrate did not increase upon increasing the PDA temperature; indeed, it shrank somewhat, as illustrated in Fig. 1c-f. After PDA at 600°C, the IL thickness in the HfO_xN_y/Si increased from ca. 6 to ca. 23 Å; in contrast, that in the HfO_xN_y/Ge decreased from ca. 12 to ca. 7 Å. Such shrinking after rapid thermal annealing in an N_2 ambient has also been observed for a HfO_2/Ge gate stack.[14] We propose two possible causes for this phenomenon: (*i*) bond breaking in the IL, which leads to subsequent desorption, or (*ii*) densification of the IL; the mechanisms are discussed in further detail below. Even so, from the viewpoint of performance, we were gratified to observe the occurrence of such contraction of the IL on the Ge system because aggressive equivalent oxide thickness (EOT) scaling may be more readily achieved. On the other hand, irrespective of the PDA conditions, the thickness of the HfO_xN_y film on the Ge substrate was larger than that on the Si substrate. This tendency is different from that reported by Kita et al. for the case of a sputtered HfO_2 film;[13] they demonstrated that both the HfO_2 film and the IL were thinner on the Ge substrate than those on the Si substrate. We suspect that these contradictory findings might arise from the use of different oxidizing gases during sputtering.

AR-XPS and AES depth profiles.— Figure 2a-d displays the AR-XPS spectra of Hf 4f, Si 2p, N 1s, and O 1s, respectively, of the HfO_xN_y film on the Si substrate before and after PDA at 600°C. In this case, the take-off angle θ was 60°. The peak for the Hf $4f_{7/2}$ binding energy of the as-deposited film appeared at 16.70 eV with spin-orbital splitting (SOS) of 1.5 eV; no additional components corresponding to metallic Hf appeared. When compared with the reported values of the binding energies for Hf–N $4f_{7/2}$ (15.55 ± 0.25 eV) and Hf–O $4f_{7/2}$ (17.35 ± 0.20 eV),[15-18] our result indicates that a considerably large component of the as-deposited HfN film has been oxidized during deposition, even though N_2 was used as the only feed gas. Moreover, the peak in the Hf $4f_{7/2}$ spectrum shifted toward higher binding energy after the subsequent PDA at 600°C for 5 min. The value of the binding energy for this peak is even higher than that of Hf–O binding; this finding reflects the fact that high-temperature annealing can further eliminate Hf–N bonds and lead to the formation of Hf–O–Si chemical bond. This high binding energy can be explained by considering the enhanced charge transfer from oxygen to hafnium and silicon.[19-21] Further evidence to support this argument is present in the Si 2p spectra. The as-deposited film displays a pronounced oxidized peak at a binding energy that is 3.7 eV higher than that of the Si substrate peak; this finding verifies the fact that a thin IL exists between the high-*k* dielectric film and the Si substrate. Moreover, this oxidized Si peak shifted slightly toward a lower binding energy, corresponding to Hf–O–Si bonding, with enhanced intensity after PDA at 600°C.[21,22] The N 1s spectrum confirmed that the reduction of nitrogen had also occurred. The content of Si–N and Hf–N bonds obviously decreased after annealing, and the signals for N–O bonds and/or N_2 molecules also reduced significantly. These results imply that the residual oxygen in an N_2 ambient plays important roles during annealing: it is able to replace nitrogen, bond to Hf atoms, and consequently leave residual SiN_x as the major nitrogen-related mode of bonding.[23,24] In addition, the O 1s peak also shifted toward higher binding energy, concomitant with an enhanced intensity. Again, this result is closely related to the degree of Hf–O–Si bond formation. Based on these experimental data, we believe that the main composition of the IL of the as-deposited film was SiO_xN_y; the further increase in IL thickness, as observed from the TEM results, arises from the formation of an additional Hf-silicate layer after high-temperature processing.

As stated earlier, increasingly greater efforts are being devoted to the deposition and study of the properties of high-*k* films on Ge substrates;[25,26] detailed material analyses using XPS, however, remain quite rare. Figure 3 presents the Hf 4f spectra of the HfO_xN_y films on the Ge substrate with respect to the PDA temperature; the inset displays the O 1s core-level spectra for the as-deposited and 600°C PDA films. As the PDA temperatures and times increased, well-resolved Hf 4f spectra (i.e., an increasing ratio of the intensities of the Hf $4f_{5/2}$ and Hf $4f_{7/2}$ peaks) appeared that gradually approximated that of pure Hf–O bonding. The dielectric film obtained after annealing at 600°C for 5 min exhibited a Hf $4f_{7/2}$ peak energy of 17.1 eV and a branch ratio of 0.75, coinciding with the ideal core-level degeneracy. Similar to HfO_xN_y deposited on the Si substrate, oxygen can readily substitute for nitrogen to be the first nearest neighbor of an Hf atom and, consequently, cause the deposited film to transform into a near-stoichiometric HfO_2 film. The asymmetric energy band in the O 1s spectrum (inset) is likely to arise from the IL, which probably contained GeO_x ($x \leqq 2$) or the Hf–Ge mixed oxide. Unfortunately, overlapping of the Ge *LMN* Auger signal with the O 1s core level makes it impossible to identify the exact contribution of each of these chemical species, but from the variation in

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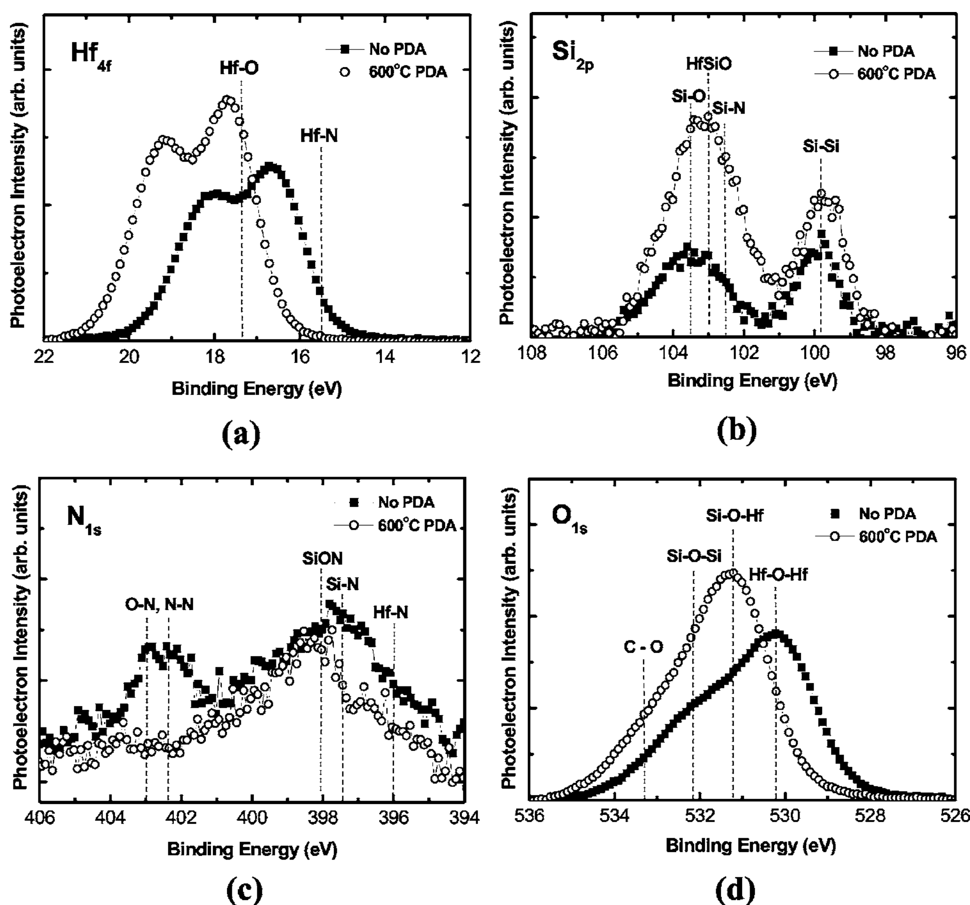

Figure 2. (a) Hf 4f, (b) Si 2p, (c) N 1s, and (d) O 1s core-level spectra of HfO_xN_y thin films on Si substrates before and after PDA at 600°C (θ = 60°). The PDA time was 5 min.

intensity in the O 1s spectrum we conclude that no other chemical bonding exists for oxygen after high-temperature thermal processing; this finding indicates that subsequent growth of an additional intermediate layer between HfO_xN_y and the Ge substrate, as we had observed for the HfO_xN_y/Si system, did not proceed. Figure 4a presents a profile, obtained through AES, of the ratio of the N_{KL1}/O_{KL1} atomic concentration as a function of the sputtering time. The trend of a declining N_{KL1}/O_{KL1} concentration ratio suggests that upon increasing the PDA temperature and duration, the substitution of nitrogen atoms by oxygen atoms became more significant in the HfO_xN_y dielectric. Figure 4b presents the corresponding N 1s spectra. From its peak intensity, Ge–N bonding appears to be the main type of bonding; it is accompanied by a very small number of Hf–N bonds. Upon increasing the PDA temperature we observed decreases in the intensities of both the Hf–N and Ge–N bonds; this finding seems to be closely related to the decomposition of these bonds in a high-temperature ambient. As discussed earlier, Hf–N bonds can be replaced by Hf–O bonds during the sputtering process; in contrast, the reported dissociation temperatures for Ge–O, Ge–N, Si–O, and Si–N bonds are ca. 360, 490, 740, and >1000°C, respectively,[27] suggesting that Ge–N bonds are less stable than Si–N bonds. Our experimental results are consistent with the previous report: the most obvious reductions in intensity of the Ge–N peak occurred at annealing temperatures above 500°C. As mentioned earlier, we believe that one of the possible reasons for the shrinkage of the IL is bond breakage, but our preliminary evidence suggests that it is too early to draw any conclusions. Because of the lower stabilities of Ge-related chemical species, however, it seems reasonable to speculate that a correlation exists between IL dissociation and shrinkage.

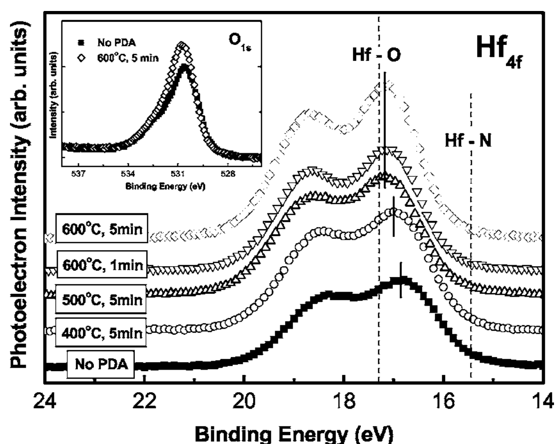

Figure 3. Hf 4f core-level spectra of HfO_xN_y thin films on Ge substrates before and after PDA under various conditions. (Inset) O 1s spectra (θ = 60°).

To obtain more evidence to support our hypothesis, we used AES and AR-XPS to perform further analyses of Ge-related bonding. Figure 5a displays the AES depth profiles of the Ge/Hf ratio with respect to the annealing temperature. A clear incremental accumulation of Ge toward the dielectric surfaces occurred upon increasing the PDA temperature. Secondary ion mass spectroscopy (SIMS) was used recently to detect the significant diffusion of Ge elements into HfO_2 films that had been deposited either at 485°C through metallorganic chemical vapor deposition (MOCVD) or subjected to PDA at 550°C.[28] Taking into consideration the resulting AR-XPS spectra for Ge 2p (Fig. 5b) allows us to further understand the chemical bonding states of the incorporated Ge atoms. Because Ge 2p spectra are more surface-sensitive than Ge 3d core-level spectra, as a result of the extremely reduced inelastic mean free path (IMFP; ca. 8 Å in our case) for photoelectrons having low kinetic energies,[29] we used

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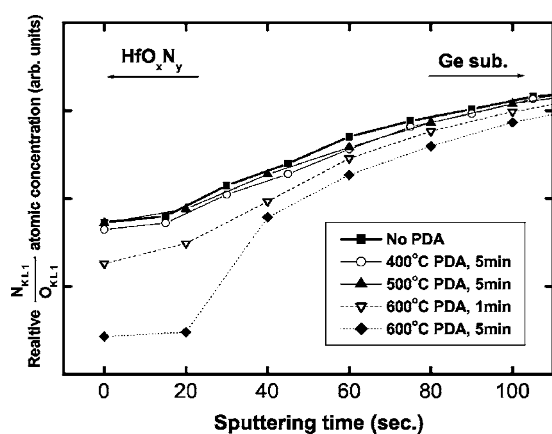


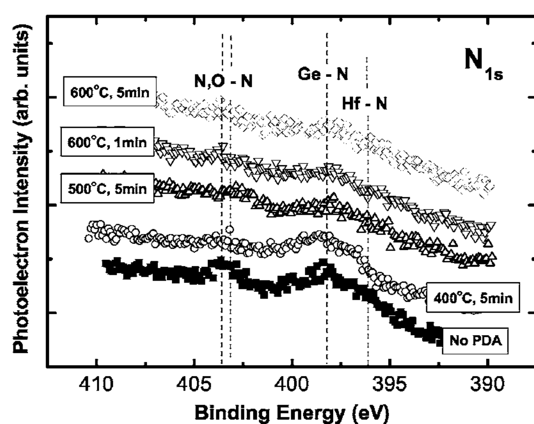
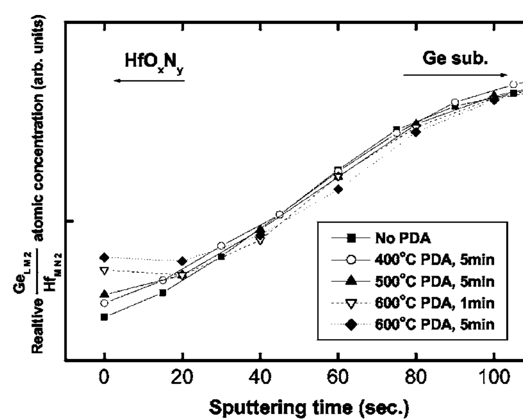
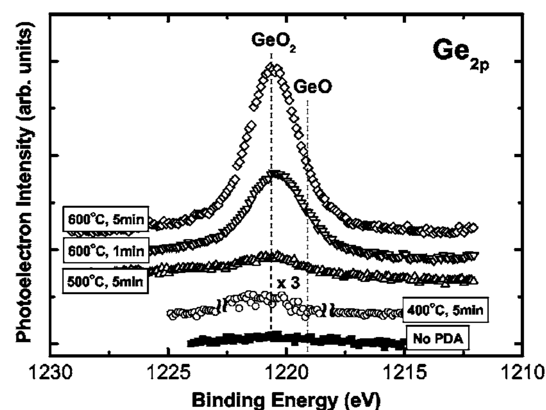


Figure 4. (a) Variation of relative N_{KL1}/O_{KL1} atomic concentration as a function of the sputtering time and the PDA conditions. (b) N 1s core-level spectra of HfO_xN_y thin films on Ge substrates before and after PDA under various conditions (θ = 60°).

them to study the changes in the composition of the high-*k* dielectric film on the Ge substrate that occurred during the PDA. The results of a previous report[30] regarding the spectra of oxidized Ge 2p allowed us to assign the peaks corresponding to elemental Ge, GeO, and GeO_2 at 1217.6, 1219.1, and 1220.6 eV, respectively; these peaks are marked in the figure. Initially, no Ge-related chemical species appeared within the high-*k* dielectric, but once PDA had been performed, we observed that the intensity of the signal for GeO_2 increased upon increasing both temperature and annealing time. The AR-XPS spectra in Fig. 5c indicate that the intensity of the signal for GeO_2 increased when the take-off angle was changed from 30 to 60°. This finding suggests that more GeO_2 was incorporated into the upper portion of the gate dielectric, which is similar to the AES examination. The volatilization sources as well as the chemical form of Ge during diffusion process are still in debate and fervently discussed.[31,32] There are two possible mechanisms responsible for the GeO_2 incorporation into HfO_xN_y thin film: one is diffusion of Ge atom from the dissociated IL and/or substrate itself, which is then oxidized by the incoming residual oxygen; the other is the subsequent oxidation of a volatile product such as GeO, formed as a result of the same origins, caused by residual oxygen during annealing. No matter which of these mechanisms is correct, we believe the out-diffusion can be achieved through the grain boundaries of the crystallized high-*k* film. Thus, we believe that the dissociation of the IL is the real cause of the shrinkage, rather than densification,





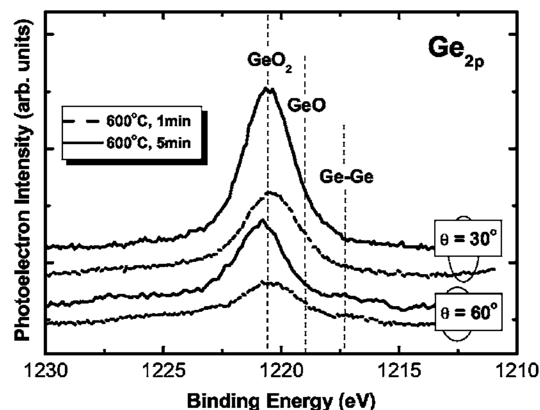


Figure 5. (a) Variation of relative Ge_{LM2}/Hf_{MN2} atomic concentration as a function of the sputtering time and the PDA conditions. (b) Ge 2p core-level spectra of HfO_xN_y thin films on Ge substrates before and after PDA under various conditions (θ = 30°). (c) Angle-resolved Ge 2p spectra of these samples.

because of the detection of GeO_2 within the bulk of the high-*k* dielectric. Further discussion for this identification is presented in the next section.

XPS-ultrathin HfON layer on Ge.— For more-direct characterization of IL desorption on the Ge substrate, we deposited an ultrathin HfO_xN_y film. Because the IL formed inherently during the initial sputtering stages, we manipulated the sputtering time to deposit the bulk dielectric (i.e., HfO_xN_y) as thin a layer as possible. The interesting changes that occurred to the Ge 2p and O 1s AR-XPS spectra before and after PDA at 600°C are presented in Fig. 6a and b,

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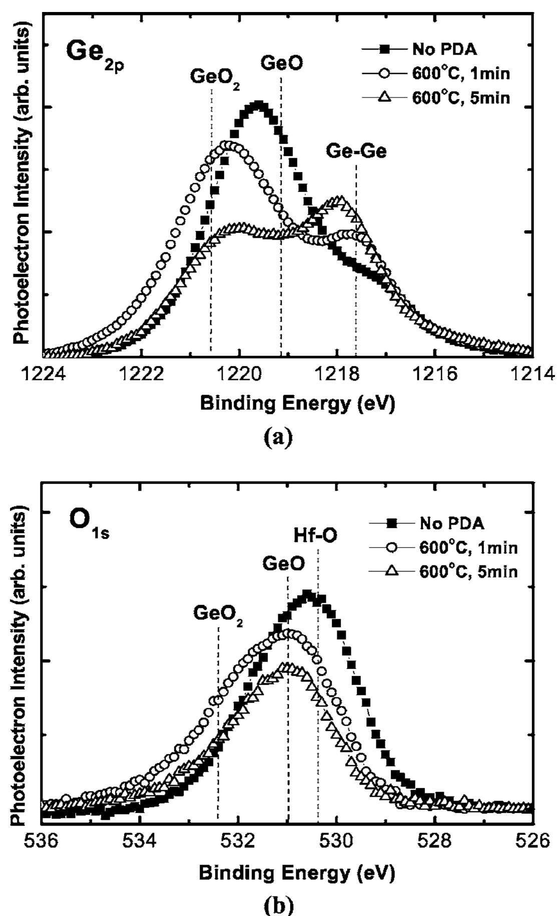

Figure 6. (a) Ge 2p and (b) O 1s core-level spectra of ultrathin HfO_xN_y thin films on Ge substrates before and after PDA under various conditions ($\theta = 60°$).

respectively. Apart from the Ge substrate signals in Fig. 6a, the IL of the no-PDA film exhibited a broad band having its main peak at 1219.7 eV; this feature is likely to result from a mixture of GeO_xN_y and HfO_xN_y. Because high-temperature annealing at 893°C is capable of forming the tetragonal $Hf_{1-x}Ge_xO_2$ structure, that upon further heating to 1200°C yields scheelite $HfGeO_4$ phase,[33] strongly suggesting poor intermixing and alloying in Ge and Hf systems. The IL peak after annealing at 600°C moved closer to the value expected for GeO_2. This result provides evidence for the dissociation and oxidation of the Ge–N bonds. Another noteworthy feature is that the ratio of the peak intensities of this broad peak and that of the Ge substrate deceased with increasing both the temperature and time; this result indicates implicitly that the thickness of the IL was reduced after annealing. To obtain a quantitative description of the IL shrinkage process, we assumed that the Ge 2p spectrum was composed simply of two components: GeO_x ($x \leqq 2$) and Ge. From this assumption, we calculated the thickness of the IL in the as-deposited sample to be ca. 9.5 Å using a GeO_x/Ge ratio of 1.3 and an IMFP of ca. 8 Å.[34] After annealing at 600°C for 1 and 5 min, the IL thicknesses decreased to ca. 7.9 and 4.5 Å, respectively. These values confirm that the IL does undergo certain chemical changes during high-temperature processing. Because the Hf 4f spectrum shifted (not shown) in a manner similar to that of the thick film discussed earlier but with lower intensity because of the ultrathin layer, we believe these out-diffused species escaped into the air. Ogino and Amemiya proposed several possible mechanisms for the loss of Ge.[35] Three possible reactions are the following[35,36]

$$GeO(s) \rightarrow GeO(v) \quad [1]$$

$$Ge(s) + GeO_2(s) \rightarrow 2GeO(v) \quad [2]$$

$$2Ge(s) + O_2(v) \rightarrow 2GeO(v) \quad [3]$$

First, perhaps the GeO chemical species directly transforms into gaseous GeO.[37] Second, the chemical reduction of GeO_2 into volatile GeO has been characterized at temperatures ranging from 350 to 550°C.[12,38-40] Thus, PDA at 600°C should accelerate desorption rate through these mechanisms. Third, considering the ready oxidation of Ge, mechanism 3 is likely to occur during annealing. It also implies that the entire exposed Ge substrate as well as the top Ge surface with HfO_xN_y covering are probably oxidized by residual oxygen in an N_2 ambient. It is reasonable to suspect that the resultant higher GeO_2 concentration near the top of thicker HfO_xN_y film is intimately related to gaseous GeO diffusion from the back side and sidewall of Ge substrate.[41] With additional XPS measurements, we did observe that the surface of high-*k*/Si samples were contaminated with GeO_2 when they were annealed alongside the high-*k*/Ge samples in an N_2 ambient above 500°C (not shown here). Thus, we cannot exclude the possibility that the presence of higher GeO_2 concentration near the surface might result from the further oxidation of airborne GeO in the chamber. However, in our case of ultrathin HfO_xN_y film, we found that the resultant peak intensity in the O 1s spectrum, presented in Fig. 6b, decreases with increasing annealing time after PDA at 600°C; the longer the time, the more significant was the out-diffusion of GeO_x. This fact implies that the amount of GeO_2 arising from gaseous GeO diffusion from the back side and sidewall of Ge substrate is limited in our case; in other words, it only plays a minor role with respect to the volatilization processes. As a result, we thought that the GeO_2 detected inside the bulk of the thicker HfO_xN_y film probably arose mainly from further oxidation of GeO from the IL and top Ge surface during annealing.

Electrical characterization.— C-V and G-V properties.— Figure 7a-d presents the multifrequency C-V and G-V characteristics of the HfO_xN_y/p-Ge and HfO_xN_y/p-Si MOS capacitors, respectively. For the as-deposited HfO_xN_y film on the Ge and Si substrates, we observe two noteworthy features: one is that the frequency dispersion at the accumulation region of HfO_xN_y/Ge is more obvious than that of the HfO_xN_y/Si, and the other is that the frequency dispersion at the inversion region is unique for the capacitors on the Ge substrate. The dispersion effects at both regions are apparently reduced after annealing at 600°C. Here, we estimated the frequency dispersion in the accumulation simply from the differences between the 1 MHz and 100 kHz curves at $V_g = -2$ V. We obtained a value of only 8% for the as-deposited HfO_xN_y/Si; in contrast, it was as high as 82% for the as-deposited HfO_xN_y/Ge and it decreased to 41% after PDA at 600°C. As far as the frequency dispersion of the accumulation capacitance is concerned, the series resistance (R_s), which is dependent on the bulk wafer resistivity and the contact resistances, can be the dominated mechanism; its effect will be amplified with the measured conductance (G_m).[42] Nevertheless, the Ge substrates that we used had slightly higher bulk resistivity than that of Si, together with the same accumulation G_m measured at 1 MHz. Thus, the effect of R_s only partly explains the difference between the dispersions of these two capacitor systems. In other experiments, we found that larger frequency dispersions also existed when depositing ZrO_xN_y or Hf-silicate high-*k* films onto the Ge substrate, relative to those on the Si substrate, when using Al or Pt metal gates (not shown here). Wu et al. reported that a large frequency dispersion of accumulation capacitance existed in high-*k*/Ge capacitors with NH_3 passivation, which was significantly improved by using the SiH_4 annealing instead of NH_3 pretreatment.[7] We may conclude that the dispersion behavior in the accumulation region is strongly related to the interface quality, e.g., the amount of the existing defects, before and after the annealing.

We clearly observed the anomalous low-frequency-like behavior of the high-frequency (in the kHz range) C-V curves in inversion for the capacitors on the Ge substrate but not on the Si substrate. Simi-

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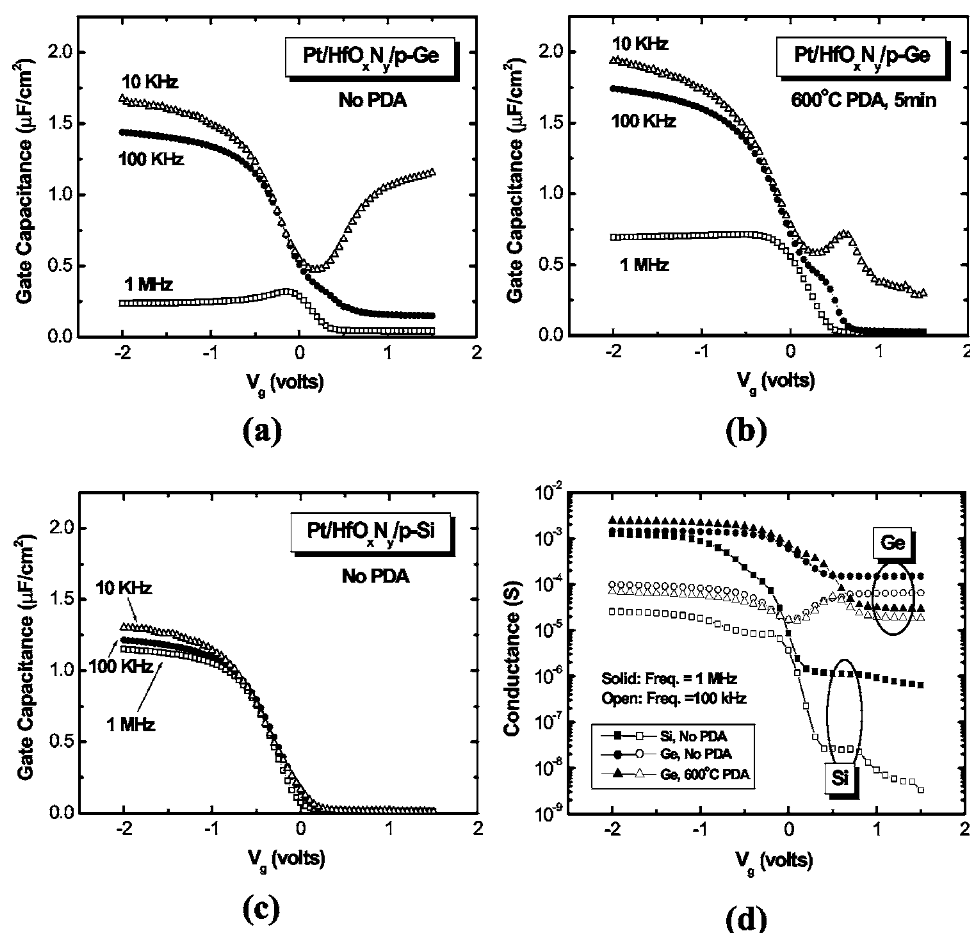

Figure 7. Multifrequency (a)–(c) C-V and (d) G-V characteristics of Pt/HfO$_x$N$_y$/p-Ge and Pt/HfO$_x$N$_y$/p-Si MOS capacitors before and after PDA at 600°C.

lar phenomena have been explored by several groups, who attributed them to the fast rate of minority carrier generation in Ge.[43] To clarify this behavior, we undertook a theoretical prediction model of the minority carrier response in the semiconductor. It is well known that two major mechanisms are responsible for the buildup of inversion charge, or the so-called generation current density, J_{gen}: (*i*) the thermal generation of electron/hole pairs via the trap levels within the space charge region (scr), denoted as J_{scr}, and (*ii*) the diffusion of minority carriers from the bulk substrate across the scr, denoted as J_{diff}. For low-frequency-like behavior to emerge, the value of J_{gen} arising from these two contributions, J_{scr} and J_{diff}, must be greater than the required displacement current (J_{disp}) flowing through the oxide. While under strong inversion, the following equations describe these relations[44]

$$J_{gen} = J_{scr} + J_{diff} = \frac{en_i w}{\tau_{mir}} + en_i^2 \frac{1}{N_{maj}} \sqrt{\frac{D_{mir}}{\tau_{mir}}} \quad [4]$$

$$J_{disp} = C_{ox} \frac{dV_g}{dt} \leqslant J_{gen} \quad [5]$$

$$f_{eff} \approx \frac{dV_g/dt}{V_{oc}} \leqslant \frac{J_{gen}}{C_{ox}V_{ac}} \quad [6]$$

where e is the electronic charge, n_i is the intrinsic carrier concentration, w is the scr width, and N_{maj} is the majority carrier concentration; D_{mir} and τ_{mir} are the diffusion coefficient and the generation lifetime of the minority carriers, respectively. The oxide capacitance C_{ox} can be approximated as being equal to the accumulation capacitance; V_{ac} is the applied ac voltage. Table I lists all of the parameters used in our calculations; among them, the natural difference in n_i between Si and Ge is the governing factor. For the Si substrate, the magnitude of J_{scr}, which is on the order of 10^{-9} A/cm^2, obviously dominates at room temperature because the magnitude of J_{diff} is on the order of 10^{-12} A/cm^2. In comparison, even though the value of J_{scr} for Ge increases to the order of 10^{-7} A/cm^2, as a result of the larger value of n_i, the value of J_{diff} increases drastically to the order of 10^{-4} A/cm^2. The fact that J_{diff}, rather than J_{scr}, becomes the major component for Ge is predictable from the lower energy gap. Dimoulas et al. reported that the activation energy E_{act} extracted from the Arrhenius plot of the inversion conductance was ca. 0.66 eV for a temperature above ca. 45°C.[45] This value of E_{act} is close to the Ge bandgap at room temperature, suggesting that a greater fraction of the minority carrier originates from J_{diff}, rather than from J_{scr}. We define an effective frequency f_{eff} for the occurrence of low-frequency-like behavior; the values correspond to ca. 0.01 Hz and ca. 2 kHz for Si and Ge, respectively. That is to say, the sufficiently high value of f_{eff} in Ge leads to the observed minority carrier response in the C-V characteristics, even in the kilohertz

Table I. Material and electrical parameters at 300 K used in the calculations.[44,51]

	Si	Ge
R_s (Ω cm)	1–10	25–29
N_{maj} (cm^{-3})	5×10^{15}	1×10^{14}
n_i (cm^{-3})	1×10^{10}	2×10^{13}
w (μm)	0.41	1.16
D_{mir} (cm^2 s^{-1})	40	100
τ_{mir} (s)	8×10^{-5}	5×10^{-3}
C_{ox} (μF/cm^2)	1.25	1.5
V_{ac} (mV)	50	50

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regime, which is consistent with our experimental findings. In addition, the reduced frequency response of the inversion capacitance after PDA may be explained in term of the minority generation lifetime. The high-temperature step assists to eliminate the process-induced bulky defects in the Ge substrate and thus, increases the value of τ_{mir} as well as lowers the rate of generation of the minority carrier.

Evaluating the measured capacitance C_m and conductance G_m at strong inversion led to a minority carrier response time (τ_R) of ca. 10^{-6} for the Ge system; this value is 3 orders of magnitude shorter than that (ca. 10^{-3}) of the Si system. As a result of the shorter value of τ_R for Ge, an inversion layer is formed rapidly in response to an external ac signal at the gate; this result agrees well with our theoretical predictions. The detailed calculation processes and basic assumptions are available in Ref. 45; in addition, we note that the contribution from the generation/recombination of e/h pairs through the interface states is excluded in the calculations because a hump appears in the HfO_xN_y/Ge system after annealing at 600°C, indicating the generation of some additional interface states. The interface state density (D_{it}) at the midgap, as determined using Hill's method,[46] is 4×10^{12} cm^{-2}. At this level of D_{it} we should observe a larger frequency dispersion in inversion, but our experimental result conflicts with this prediction. Thus, we believe that the contribution of the value of D_{it} plays only a very minor role in the frequency dispersion in the Ge case, even though this factor may be critical in the Si case.

Oxide charge trapping and gate leakage current.— To correctly elucidate the effect of postannealing on the underlying shift in V_{FB}, we carefully chose the maximum and minimum gate biases in the bi-directional C-V sweeps to avoid significant charge trapping. Interestingly, we observe opposing trends in the V_{FB} shift for these two gate stacks (Fig. 8a). Upon increasing the annealing temperature, the value of V_{FB} of HfO_xN_y/Si undergoes a positive shift, whereas that of HfO_xN_y/Ge exhibits a negative shift. As far as the charges of high-*k* film deposited on Si substrates are concerned, nitrogen-induced positive charges have been reported as being present in HfO_xN_y systems, relative to the charges of the pure metal oxides.[11] The presence of positive fixed charges leads to the lowered value of V_{FB} in the as-deposited HfO_xN_y film on the Si substrate. Similar results have been presented for other nitrogen-incorporated metal oxides, e.g., ZrO_xN_y[47] and TaO_xN_y.[48] The subsequent N_2 PDA is expected to eliminate the bond imperfections, such as dangling bonds, nitrogen-related defects, and oxygen vacancies, thereby compensating for the positive charges in the dielectric film and returning V_{FB} to its ideal value. We deduce that the bond repairing and charge neutralization processes also occur reasonably in the HfO_xN_y/Ge system. In fact, the continuing negative shift in the value of V_{FB} upon increasing the PDA temperature departs from its ideal value. This deviation suggests that the value of V_{FB} in HfO_xN_y/Ge may be driven not only by the mechanisms above but also by a certain predominant mechanism unobserved and/or inhibited in HfO_xN_y/Si.

In addition to the differences in V_{FB}, we also observe in Fig. 8b opposing dependences of the oxide charge trapped density (N_{eff}) with respect to the PDA temperature for these two MOS structures. The value of N_{eff}, i.e., the electron trap, is evaluated quantitatively by measuring the hysteresis width at V_{FB}.[49] We observe that the PDA reduces charge trapping effectively in HfO_xN_y/Si, but it increases the charge trapping in HfO_xN_y/Ge. We speculate that the presence of these considerable positive fixed charges and electron-trapping sites in high-*k*/Ge capacitors correlates closely with the volatilization processes. Bond breaking and/or chemical reduction may result in the interface degradation. A high density of charged defects is probably generated near and/or at the interface, thereby causing a negative shift in V_{FB} as a result of acting as positive fixed charges. Meanwhile, the GeO_2 units present throughout the high-*k* dielectric and IL may behave as trapping centers, leading to the severe charge-trapping effect. These resultant electron traps also emerge as a potential problem for further high-*k* applications, e.g., the instability of the threshold voltage in a MOSFET. As a result, means of suppressing the Ge-mixed oxides at the interface will be indispensable in the pursuit of high-performance high-*k* gate dielectrics and interfaces on Ge substrates.

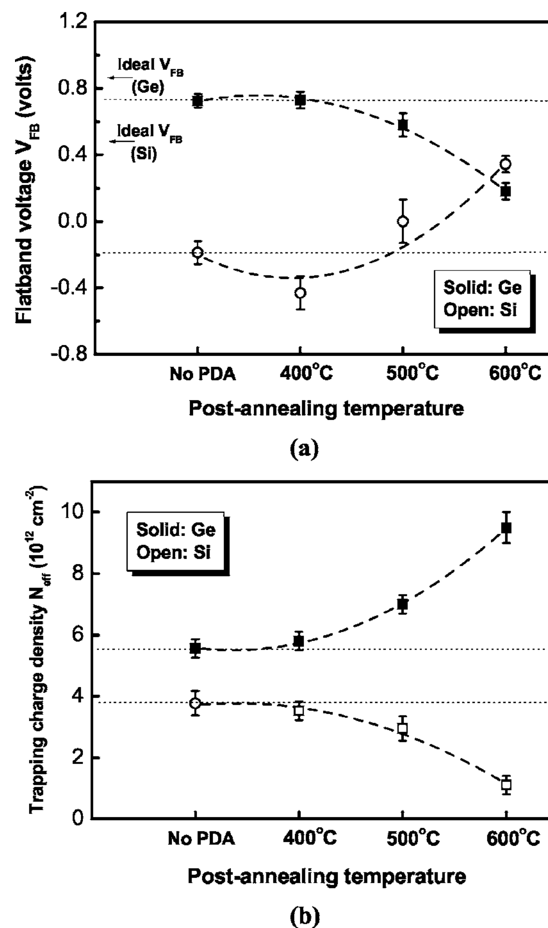

Figure 8. PDA temperature dependence of the values of (a) V_{FB} and (b) N_{eff} of HfO_xN_y/p-Ge and HfO_xN_y/p-Si MOS capacitors, respectively. Note that the error bars include difference arising from the processing durations (1, 3, and 5 min). The dashed lines are provided merely to guide the eye.

We estimated the capacitance-equivalent thickness (CET) based on the accumulation capacitance of 100 kHz C-V curves at a V_g value of −2 V. As displayed in Fig. 9a, a longer annealing time increased the CET of the HfO_xN_y film on the Si substrate, but it decreased the CET of the corresponding film on the Ge substrate. The further CET scaling upon extending the PDA time for the HfO_xN_y/Ge gate stacks may be interpreted as resulting from the inhibited growth of the IL. The left axis in Fig. 9b presents the corresponding gate leakage (J_g) characteristics of the HfO_xN_y/Ge system, while the right axis presents the increase in J_g at (V_{FB} − 2) V with respect to the PDA temperature. The leakage path of the high-*k* dielectric has several origins, e.g., film crystallization, thickness reduction, and defect generation. Among these factors, the contamination of GeO_2 may contribute substantially to gate leakage above 500°C. Despite the rapidly increasing value of J_g, it is noteworthy that these values for our HfO_xN_y/Ge sample remain extremely low, by nearly 4 orders of magnitude, when compared with those of a standard SiO_2/Si sample having a similar value of CET.[50]

Dielectric reliability testing.— Before stepping into a discussion of the reliability characteristics, we present in Fig. 10a the variation of the equivalent breakdown field (E_{BD}) of the HfO_xN_y film as a result of PDA processing. The value of E_{BD} was obtained by the formula $E_{BD} = (V_{BD} - V_{FB})$/CET, where V_{BD} is the breakdown voltage. The

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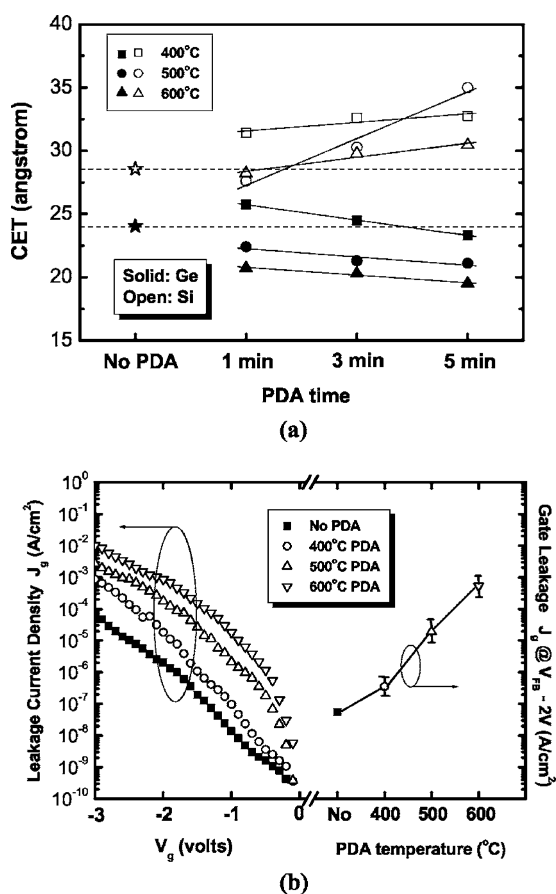

Figure 9. Left axis: PDA-dependent values of J_g as a function of gate bias (V_g) in accumulation for HfO_xN_y/p-Ge. Right axis: Plot of J_g vs PDA temperature.

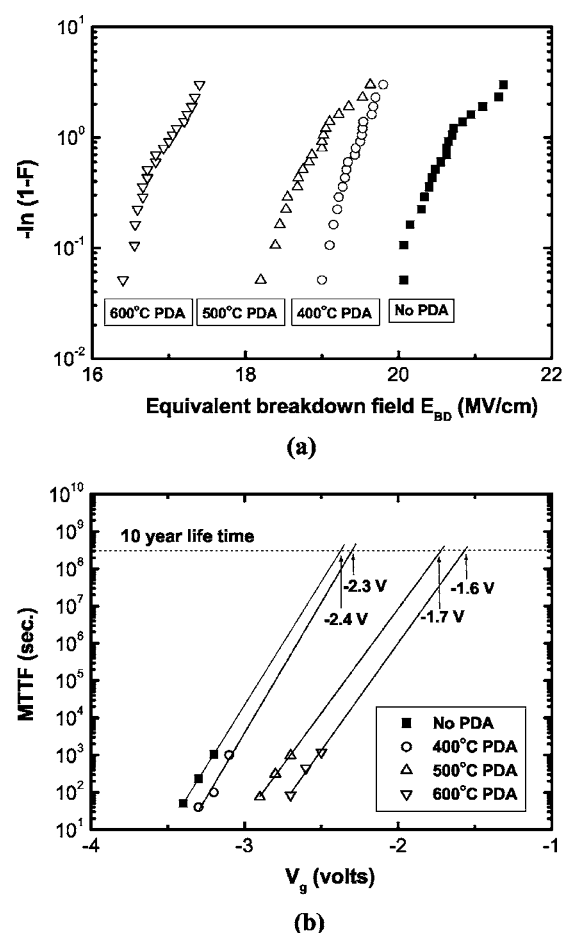

Figure 10. (a) Weibull distribution of the values of E_{BD} of HfO_xN_y/p-Ge as a function of the PDA temperature. (b) The projected 10 year lifetimes extracted from the TDDB data, displaying a decreasing trend with respect to the PDA temperature.

results in the Weibull plot indicate that the robustness of the gate dielectric displays a strong dependence on the PDA temperature. In other words, the higher the annealing temperature, the lower the value of E_{BD} of the dielectric gate stack. Furthermore, these four samples were subjected to constant-voltage-stress tests; Fig. 10b presents the time-dependent dielectric breakdown (TDDB) reliability data. The operating voltages through 10 year lifetime projections for the as-deposited, 400°C PDA, 500°C PDA, and 600°C PDA films, are −2.4, −2.3, −1.7, and −1.6 V, respectively; i.e., they are also characterized by a decreasing trend. We believe that a much higher electric field is applied to the ILs because its dielectric constant is lower than that of the bulk dielectric layers. Consequently, the occurrence of dielectric breakdown is induced mainly by the breakdown in the ILs. Thus, we deduce that the reliability degradation after PDA may be understood by considering weakly bound ILs rather than bulk layers. Considering that more electron traps and fixed charges are present in the HfO_xN_y sample after high-temperature thermal processing, defect-induced dielectric degradation may be regarded as the major cause of both the reduced value of E_{BD} and the continuously dropping allowable operation voltage.

Conclusions

We have systematically studied the effects that PDA have on the characteristics of HfO_xN_y sputtered thin films on Ge and Si substrates. We attribute the opposing MOS characteristics of these two substrates to the different nature of the chemical bonding in the ILs formed. As the PDA temperatures and times increase, increasingly more GeO_2 is incorporated into the high-k gate dielectric and severe desorption of the IL occurs for the HfO_xN_y/Ge gate stacks. Because of these unique phenomena, the electrical properties of HfO_xN_y/Ge differ from those of HfO_xN_y/Si, e.g., further CET scaling, increases in the number of positive fixed charges and the degree of oxide charge trapping, and the degradation of dielectric reliability. In addition, the anomalous low-frequency-like behavior of high-frequency C-V curves in inversion for the capacitor fabricated on the Ge substrates, relative to that of those on Si substrates, was predicted from theoretical calculations. We believe that the continuous optimization of the interface structure through process modification will improve the electrical performances of the HfO_xN_y/Ge gate stacks even further; as a result, they will be considered as promising gate dielectrics for Ge devices.

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