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Comparison of MiM Performance with Various Electrodes and Dieletric in Cu Dual Damascene of CMOS MS/RF Technology

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In this paper, we have compared the performance of metal–insulator–metal (MiM) capacitors for different bottom electrode materials including Cu, TaN, and Al in Cu–back-end-of-the-line (BEOL) process. A high-performance and low-defect-density MiM capacitor for mixed-signal and radio frequency (MS/RF) technology based on a 130 nm complementary metal oxide semiconductor (CMOS) process was demonstrated. Q-factor can achieve >100 for both Cu and Al at 2.4 GHz with 0.7 pF MiM capacitors. TaN showed a low Q-factor (<60) due to high resistivity. The process incorporates aluminum electrode into Cu–BEOL for MiM capacitor with a cost-effective process. The roughness of electro-dielectric interface by a thin aluminum electrode is critical for MiM performance due to field enhancement by roughness of a thin aluminum electrode. We have demonstrated a way to eliminate the roughness effect of thin Al and provide a MiM capacitor with high performance and low defect density. In particular, a method is demonstrated to achieve better matching, leakage, electrical breakdown, and temperature coefficient of capacitance performance for MiM capacitors.
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High-quality passive elements integrated with logic have been the trend of mixed-signal and radio frequency (MS/RF) SoC. The on-chip integration of MiM inductors with logic process is popular for area, cost, and performance enhancement. For 0.18 μm technology and beyond, aluminum is used as the logic interconnects. While integrating MiM with the logic process, one interconnect layer is usually used as the bottom electrode plate of MiM capacitors. The thick Al interconnect (~4 k) offers a low resistivity and planar electrode which results in a high Q and low interface leakage. In the Cu back-end-of-line (BEOL) era, the use of Cu as the bottom electrode plate is the most cost-effective method because the Cu layer is also used for logic area without extra cost. Cu also has a very low resistivity and results in a high Q performance. Our results show that Cu can achieve $Q \approx 200$ at 2.4 GHz with 0.7 pF MiM capacitor. However, it has been reported that Cu roughness causes MiM reliability problems.[1-3] In addition, Cu can be used for small-area MiM but the performance is significantly degraded for larger area MiM capacitors. Cu roughness and Cu–chemical-mechanical polishing (CMP) μm-scratch are two factors for the worse early breakdown of the bottom electrode plate. To develop highly reliable, high-Q, and high-yield MiM capacitors, we have compared different MiM bottom electrodes (Table I) and developed an optimized TaN/Al/TaN bottom electrode plate with thin Al thickness for mass production. The Q value can achieve 115 at 2.4 GHz with 0.7 pF MiM capacitor for the Al bottom electroplate. For the pure TaN bottom electroplate, the Q factor is significantly degraded by more than half due to high resistivity. For Al process, serious roughness is observed for the thin Al layer. To resolve the field enhancement due to roughness of the thin Al bottom electroplate, we have developed a method to optimize the process of aluminum deposition to fully resolve the effect. A high-Q, highly reliable, and capable of manufacturing MiM process in Cu-BEOL is realized.

MiM Capacitor Process

The process was based on the standard 0.13 μm complementary metal oxide semiconductor (CMOS) technology provided by the foundry. After processing the 0.13 μm front-end-of-the-line (FEOL) and Cu dual damascene process with an eight-level Cu interconnect, an Al MiM capacitor was inserted into the top two metal layers. The MiM structure is shown in Fig. 1. After the 7th metal layer was patterned after Cu-CMP, an etching-stop layer was deposited for further processing. A thin aluminum layer was deposited and sequentially followed by TaN deposition as the material for bottom plate. Plasma-enhanced chemical vapor deposition (PECVD) SiO_2 or Si_3N_4 was then deposited as the capacitor dielectric, followed by TaN deposition as the top plate. Two masks were used to pattern the top plate and bottom plate. After oxide deposition, the via connection is formed to connect the top plate, bottom plate, and logic area at the same time. The oxide topography due to the stacked MiM structure is polished by Cu-CMP while forming the top metal interconnect. The resulting MiM capacitor has demonstrated high Q, high yield, and a wide process window for manufacturing. The current–voltage (I–V), capacitance–voltage (C–V), and quality factor (Q) were measured by HP4156, HP4284, and HP8510C, respectively.

MiM Capacitor Characterization

For rf application, the quality factor of MiM capacitors with different bottom electrodes is shown in Fig. 2. Copper can achieve a quality factor of ~200 and TaN/Al/TaN electrodes ~115 at 2.4 GHz with 0.7 pF. For the pure TaN bottom electrode plate, the Q factor can only achieve ~54 at 2.4 GHz due to higher resistivity. The capacitance increases at high frequency due to the resonance of the parasitic inductor, which can be flattened out by a proper de-embedding procedure.

Table I. Comparison of MiM performance for different bottom electrode materials.

Bottom Plate	Cu	TaN	Thin Al	Optimized Al	Optimized Al
Top plate	TaN	TaN	TaN	TaN	TaN
Masks	1	2	2	2	2
Dielectric	SiO_x	SiO_x	SiO_x	SiO_x	Si_3N_4
C (fF/um^2)	1	1	1	1	2
Q at 2.4 GHz, 625 um^2	~200	~54	~115	~115	
TCC (ppm/C)	−35	−50	−60	−50	
VCC1 (ppm/V)	30	16	30	30	55
VCC2 (ppm/V^2)	−30	−30	−33	−30	22
Mismatching (%, 625 um^2)	~0.05		~0.05	~0.038	~0.031
Defect density (1/cm^2), (Vbd <3.3 V failure)	>1.0		>0.3	<0.05	

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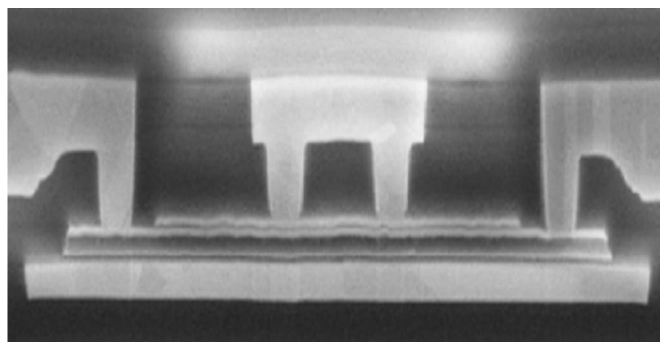

Figure 1. Structure of integrated MiM capacitor with TaN/Al/TaN bottom electrode and TaN top electrode.

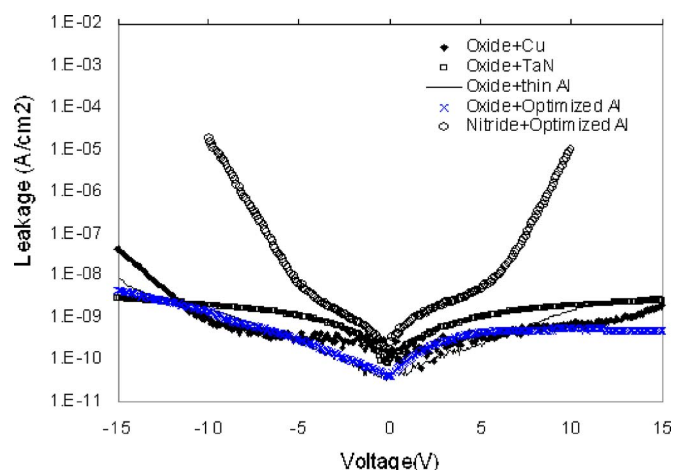

Figure 3. Comparison of current vs voltage behavior for different bottom electrode materials.

In addition to high Q, another important factor is the leakage current. This is especially important for high-density analog/rf integrated circuits (ICs) similar to the case of the dynamic random access memory (DRAM) capacitor.[4,5] In this work, we also optimized the MiM leakage current. Typical leakage (J–V) behavior of different bottom electrode materials is shown in Fig. 3. The asymmetrical leakage for applied voltage is due to the different roughness between top and bottom electrode plates. For positive applied voltage at the top electroplate, electrons are injected from the bottom plate to the top plate. The roughness of the bottom electro-plate is critical for creating sites with higher electric fields. Under low electric fields, the trap-assisted tunneling (TAT) of electrons from the electrode to trap states in the dielectric close to the electrode–dielectric interface dominate the capacitor leakage.[6] Nitride dielectric showed a higher MiM leakage dependence with the applied leakage compared with plasma-enhanced oxide (PEOX) dielectrics. This is caused by the intrinsic leakage characteristics of silicon nitride film. The leakage current is very low, in the range of $<1 \times 10^{-10}$ A/cm^2 at 1.2 V for optimized Al with SiO_x. On the other way, the impact of asymmetric leakage due to different top and bottom electrode plates is minor. The top electrode is deposited onto the dielectric material and there is no surface roughness issue. The top electrode plate is also designed to connect the top metal line through via array, and the resistance is much lower compared with the bottom electrode plate and has minimum impact on MiM performance.

The comparison of MiM breakdown voltage (Vbd) performance is shown in Fig. 4, with 1,000,000 μm^2 MiM area for bottom electrodes with TaN and Al and 640,000 μm^2 for bottom electrodes with Cu. The Vbd cumulative failure of the Cu electrode plate is much worse than TaN and Al/TaN electrodes due to worse surface roughness and inevitable Cu-CMP dishing. For the small-area MiM capacitor, the Cu electrode is still an option but high defect density is a concern. For thin TaN/Al ($<$1.5 k)/TaN electrode, the surface roughness is observed to be critical, which was not significant for conventional Al ($>$3 k)/TiN bottom electrode plates beyond 0.18 μm technology. By optimizing the process temperature and other process conditions of Al deposition process, the degradation of MiM Vbd by surface roughness is significantly reduced.

The reflectivity of the Al/TaN electrode vs the waiting time of the Al process also demonstrated robust process after optimization, as shown in Fig. 5. Before the process is optimized, the reflectivity decreases significantly with process waiting time. For the optimized thin Al process, the dependence on the waiting time of the Al deposition process is negligible compared with the original one. This indicates that the optimized Al deposition has a stable surface roughness with a manufacturable process window.

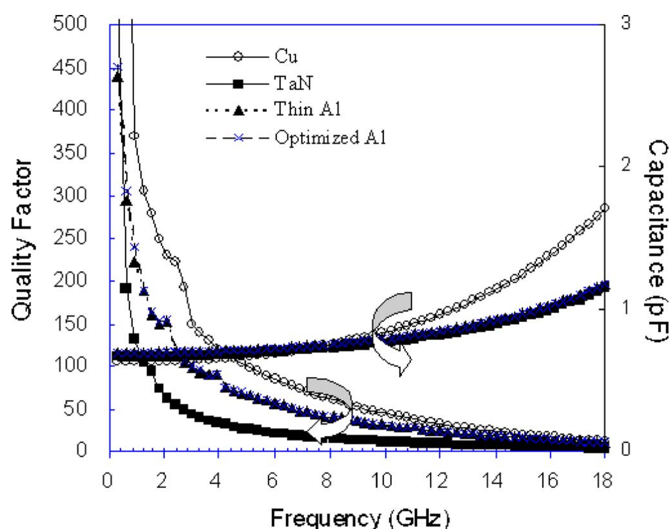

Figure 2. The quality factor of 25 × 25 μm MIM capacitors. Cu has the highest quality factor with ~200 at 2.4 GHz. TaN/Al/TaN showed Q ~ 115, but TaN can achieve only 54 at 2.4 GHz.

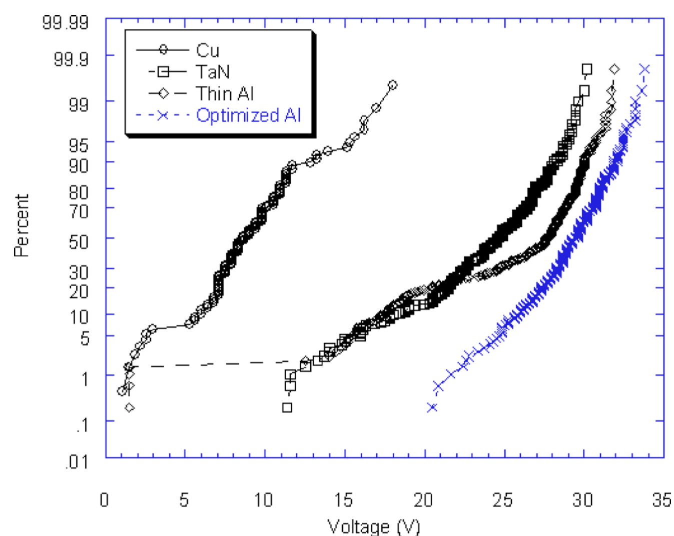

Figure 4. MiM Vbd comparison with different bottom electrode plates. Wafers with optimized Al/TaN bottom electrodes showed the best breakdown voltage.

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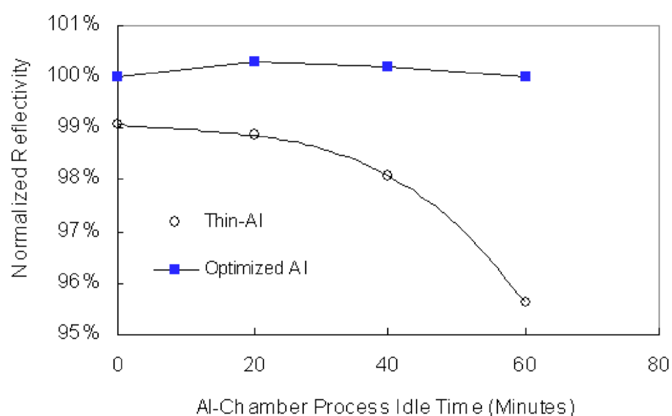

Figure 5. Normalized reflectivity vs Al-deposition waiting time to show the relative surface roughness effect. Conventional thin Al has a decreasing reflectivity with longer Al-chamber waiting time. This means the surface roughness is unstable for conventional Al process condition.

Linearity is a critical characteristic for capacitors. Figure 6 shows the normalized capacitance for four different bottom electrode plates vs temperature from 25 to 125 C. Cu demonstrates minimal first-order temperature coefficient of capacitance with less than 40 ppm/°C and ~30% reduction compared to TaN and TaN/Al/TaN. Figure 7 shows the normalized capacitance for three different bottom electrode plates and two dielectric materials vs the bias voltage from −5 to 5 V. TaN demonstrated much better first-order voltage coefficient of capacitance (VCC1) compared with TaN/Al/TaN. The second-order voltage coefficient of capacitance (VCC2) is comparable for different bottom electroplates. However, MiM dielectric with nitride has a positive VCC2 (22 ppm/V^2) compared to a negative VCC2 (−30 ppm/V^2) for SiO_x MiM dielectrics. The negative second-order voltage coefficient of capacitance for SiO_x dielectrics is due to the intrinsic leakage current while applying voltage. The positive VCC2 of silicon nitride film is due to charge trapping in the nitride film.[7]

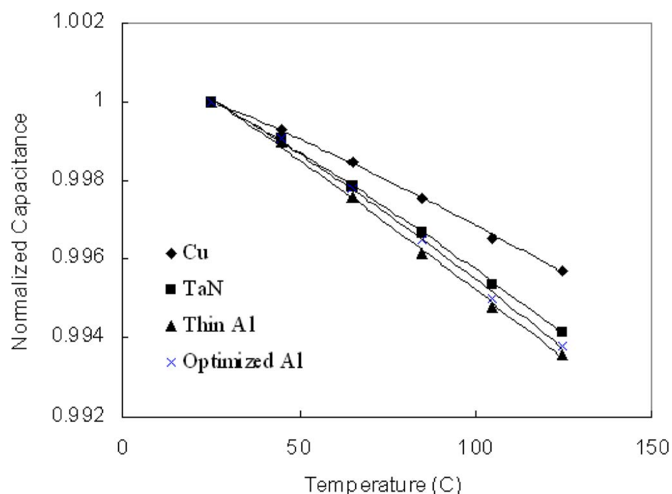

Figure 6. Comparison of temperature linearity on MiM capacitors. Cu bottom electroplate has the smallest TCC1 with −35 ppm/°C.

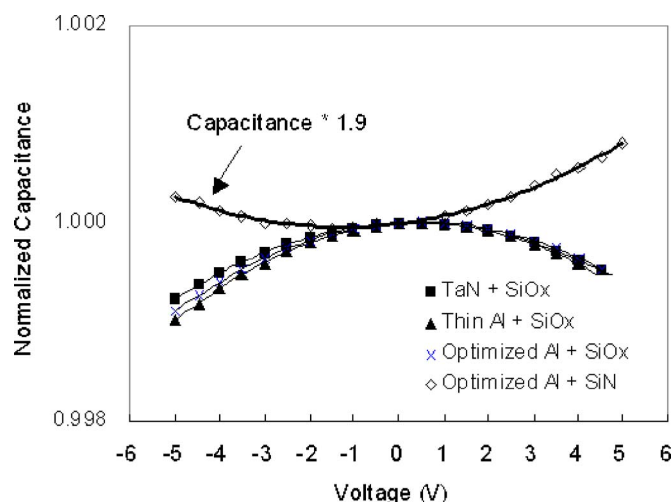

Figure 7. Comparison of voltage linearity on MiM capacitors. Nitride dielectric showed a positive VCC2 compared with a negative VCC2 of SiO_x.

Conclusion

The incorporation of MiM capacitor into Cu-BEOL needs a different approach compared with 0.18 μm technology. The adoption of process options depends on the intent of product design and MiM area. For high-Q and small MiM area product, Cu as a capacitor bottom plate is a suitable option but has a lower process yield. TaN-based MiM capacitor can achieve low leakage and linearity but a penalty of a low quality factor of ~54 at 2.4 GHz due to high resistivity. A MiM capacitor with a thin Al bottom plate can also be achieved with optimized process condition. The Al-based MiM capacitor can achieve $Q > 100$ at 2.4 GHz with ~0.7 pF. The optimized process conditions can achieve a very low defect density suitable for manufacturing.

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