Journal of The Electrochemical Society, **153** (2) G144-G148 (2006)
0013-4651/2005/153(2)/G144/5/$20.00 © The Electrochemical Society

The CMP Process and Cleaning Solution for Planarization of Strain-Relaxed SiGe Virtual Substrates in MOSFET Applications

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The effects of different polishing pads and slurry solid contents on the SiGe chemical mechanical polish (CMP) process were investigated. By optimizing the polishing conditions, a smooth strained-Si surface on a flattened $Si_{0.8}Ge_{0.2}$ buffer layer of 0.6 nm can be achieved. The novel cleaning solutions with various surfactants and chelating agents for post-CMP SiGe were studied. There was about 10% current enhancement of the optimal cleaning conditions, showing high performance in particle removal, metallic cleaning, and electrical characteristics.
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Manuscript submitted February 22, 2005; revised manuscript received October 11, 2005.
Available electronically December 30, 2005.

Strained silicon on relaxed silicon–germanium (SiGe) substrates is a promising candidate for transistor performance enhancement.[1] Strain splits the degeneracy in the conduction and valence bands of Si, enhances the transport properties of electrons and holes, and provides transistor speed enhancement. High-quality strained–relaxed buffer layers are required for high-performance devices, but the relaxed SiGe layers tend to have threading dislocations and rough surfaces. Several methods such as the graded buffer layers[2,3] and low-temperature buffer[4] methods have been studied. Relaxation during the growth of the visual substrate results in a crosshatch (misfit dislocations) which increases surface roughness. The chemical mechanical polishing (CMP) process has become the mainstream of global planarization techniques in fabrication of deep submicrometer integrated circuits. To reduce surface roughness, the CMP process is being applied to the grown layers. A few researchers have introduced it into polishing SiGe buffer layers.[5-9] The high crystalline quality of the regrowth layer with a smooth interface makes it possible to fabricate high-performance SiGe devices with low surface roughness scattering. However, the wafer surface after the CMP process is seriously contaminated with particles and metallic impurities from the polishing slurry. In addition, the metallic impurities induce many crystal defects in the Si wafers during thermal processing,[10] and planarized SiGe buffer layer roughness is increased due to the etching effect.[11] Our previous studies have found that the novel post-CMP cleaning solution can significantly reduce contamination retention.[12,13] The surfactant tetramethylammonium hydroxide (TMAH) and the chelating agent ethylenediaminetetraacetic acid (EDTA) were used to enhance the removal efficiency of particle and metal impurities. We found that removal efficiency of particle and metallic impurities was enhanced by post-poly-Si CMP cleaning. The electrical characteristics can be also improved by the novel post-CMP solution. In this paper, we applied the post-CMP cleaning on SiGe buffer layers. Furthermore, the capacitor and metal oxide semiconductor field effect transistor (MOSFET) electrical characteristics of strained-Si regrowth on the substrate treated with various solutions were also evaluated.

Experimental

The SiGe epitaxy layers on 6-in.-diam Si(100) substrates were prepared by ultrahigh-vacuum chemical vapor deposition (UHV-CVD). The novel relaxed 700-nm-thick SiGe buffer with a 50-nm-thick Si inserted layer was used in this work.[14] For measuring the SiGe layer thickness, we used the electron cyclotron resonance (ECR) etcher to form a trench on the SiGe buffer layer and a surface profiler to measure the height of the trench in order to monitor thickness. The CMP experiment was carried out on a Westech model 372M CMP processor consisting of a Rodel IC 1400 pad and Politex buffering pad with diluted CABOT SS-25 slurry. The solid content of the experimental slurry was diluted by deionized (DI) water at volume ratios of 1:9 and 1:18. The downforce pressure was fixed at 3 psi for studying the time effects. In the following, it was varied from 3 to 7 psi for 1 min to investigate the effects of the downforce pressure and removal rate. Surface morphologies were characterized by atomic force microscopy (AFM).

In the post-CMP cleaning experiment, wafers were sprayed with diluted NH_4OH solution with megasonic, followed by dispensing the cleaning solution with a poly(vinyl alcohol) (PVA) brush after the CMP process. There were four kinds of cleaning solution separated as following: (SC1) diluted 29% NH_4OH, (SC1 + T) 29% NH_4OH + 2.38% TMAH (volume ratio to NH_4OH is 1%), (SC1 + E) 29% NH_4OH + EDTA (100 ppm), and (SC1 + TE) 29% NH_4OH + 2.38% + TMAH (1%) + EDTA (100 ppm). The particle number was counted by the TENCOR surface scan model 4500 system. Total refection X-ray fluorescence spectrometry (TXRF), Atomika model 8030W, was used to determine the metallic impurity. After the post-CMP cleaning process, 20-nm strained-Si film was form on the CMP SiGe buffer layer. For verifying the clean solution effect, a 20-nm TEOS oxide formed a capacitor and MOSFET structures. The electrical properties of the capacitor, i.e., current–voltage and time-dependent dielectric breakdown (TDDB) characteristics, were measured using the Hewlett-Packard (HP) 4156 semiconductor parameter analyzer.

Results and Discussion

Various slurry solids containing different pad properties are shown in Table I. Figures 1 and 2 show the SiGe AFM image of the as-grown buffer layer before and after planarization. There are four kinds of conditions. The effects of polishing pad properties on the

Table I. Different slurry and pad conditions for Ge01, Ge02, Ge03, and Ge04 samples.

Pad condition \ Slurry condition	Slurry : H_2O 1 : 9	Slurry : H_2O 1 : 18
Politex pad	**Ge01** (AFM RMS) 20.6 Å → 2.52 Å	**Ge03** (AFM RMS) 25.3 Å → 3.39 Å
IC1400 pad	**Ge02** (AFM RMS) 22.1 Å → 2.69 Å	**Ge04** (AFM RMS) 22.3 Å → 3.59 Å

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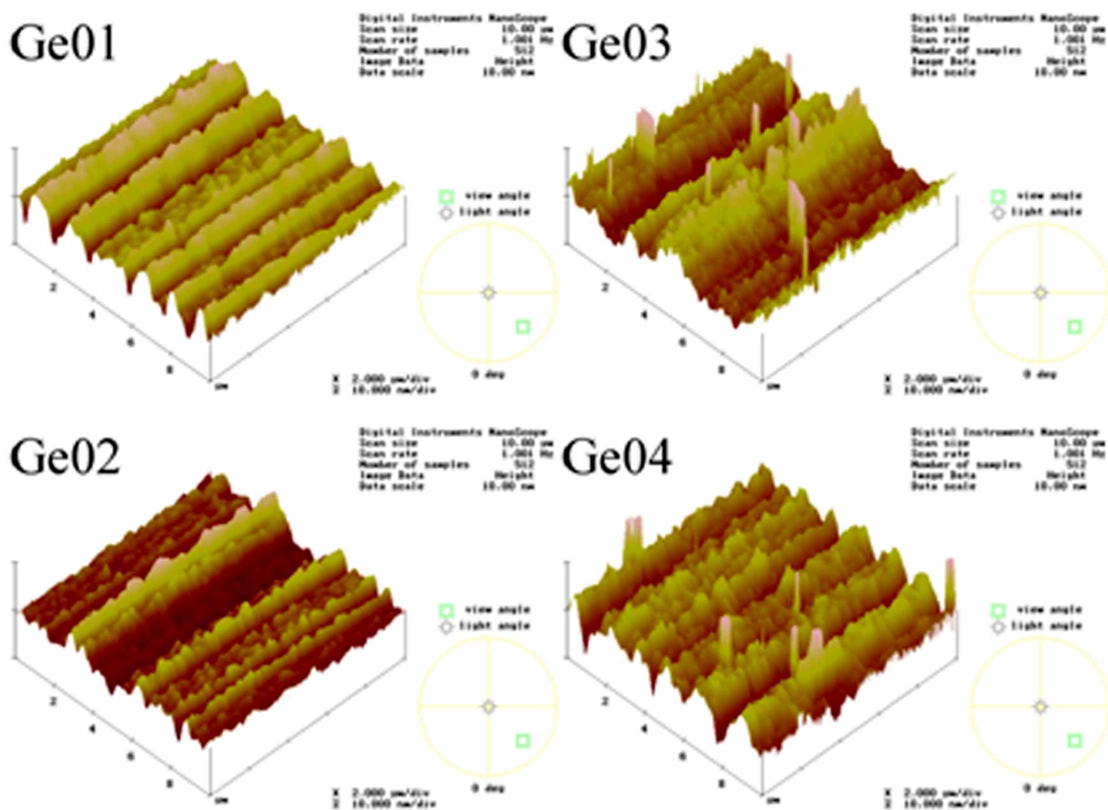

Figure 1. AFM images of strained–relaxed SiGe buffer layers before CMP processing.

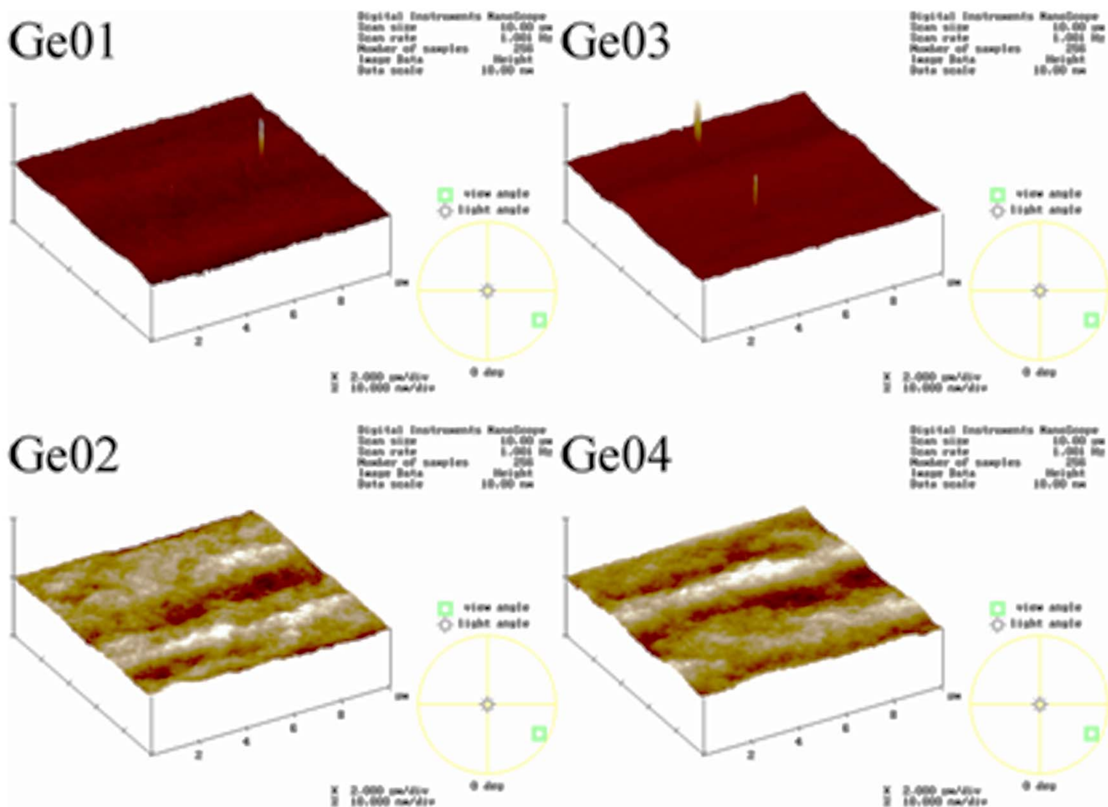

Figure 2. AFM images of strained–relaxed SiGe buffer layers after CMP processing.

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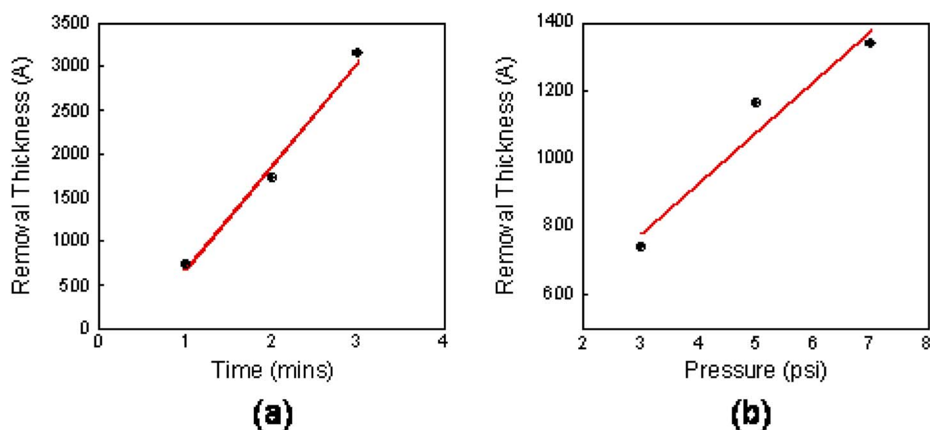

Figure 3. Removal rate of (a) time-dependence and (b) pressure-dependence in SiGe layers.

process characteristics were studied. The IC 1400 pad was compared with the Politex polishing pad regarding surface roughness. By polishing with the Politex pad, a better uniformity was achieved. As shown in Fig. 2, Ge01 and Ge03 samples almost have no crosshatch pattern. The softer Politex pad is a composite of the porous polymer and it could have uniformly distributed the polish particles. No differences in the pad influenced the geometry effects, which can be explained with the same near-surface layer affecting the interaction between pad and wafer. The hardness of the IC 1400 allows the material to planarize across wide areas with minimal dishing and good planarity, but the Politex polishing pad improves resilience and compressibility of the pad and enhances global uniformity in the polish removal. For the different solid content, a volume ratio of 1:9 shows better surface morphology in the AFM root-mean-square (rms) results of Table I. In order to have the controllable removal rate, different periods of time from 1 to 3 min in 3 psi are shown in Fig. 3a. The removal rate is a linear distribution time scale, but the time extrapolation is not zero. As we started to polish the surface, a thin oxide covered the SiGe buffer layer and slowed the polish rate. Figure 3b shows that the pressure-dependent removal rate is saturated at a higher pressure. Compared to the conditions of 5 and 7 psi, the 3-psi condition has a higher removal thickness difference. When applied at higher pressure on the exitaxy SiGe surface, it could introduce some mechanical stress on the initial surface. We use a low-pressure condition to avoid the additional stress. The conditions of stable removal rate and smooth surface interface are achieved by a Politex pad polish and a 1:9 solid content ratio for 1 min and 3 psi. As Fig. 4 illustrates, the samples with and without the CMP process were followed by strained-Si regrowth. The rms values with and without CMP are 0.6 and 1.8 nm, respectively. The surface roughness and crosshatch pattern were eliminated by CMP. Figure 5 shows residual particles on the post-CMP cleaning surface with different solutions. It is found that the SC1 + TE sample exhibits the highest efficiency. The slight surface etching of the wafer and electrical repulsion between the wafer surface and the particle can enhance removal of particles. It has been shown that the hydrophobic surface resides more heavily on particles on the wafer surface than the hydrophilic surface.[15] Figure 6 shows the metallic impurity concentration measured by TXRF. The metallic contaminants are significantly removed by the SC1 + E and SC1 + TE solution. EDTA can trap the potassium ions to reduce solution ionic strength and enhance the electric double-layer repulsion between the particle and wafer surface.[16] In our previous study,[13] it seems that combination of TMAH and EDTA play important roles in contamination removal and results in the best efficiency. The metallic contaminants are removed significantly, and the chelating agent reacts with metallic ion in the form of a metal-chelating complex.[17,18] In Fig. 7, the current vs electric voltage of the metal oxide semiconductor (MOS) capacitor cleaned by four solutions is shown. The MOS capacitor using SC1 + TE solution depicts the lowest leakage current and highest breakdown voltage among these four samples. It

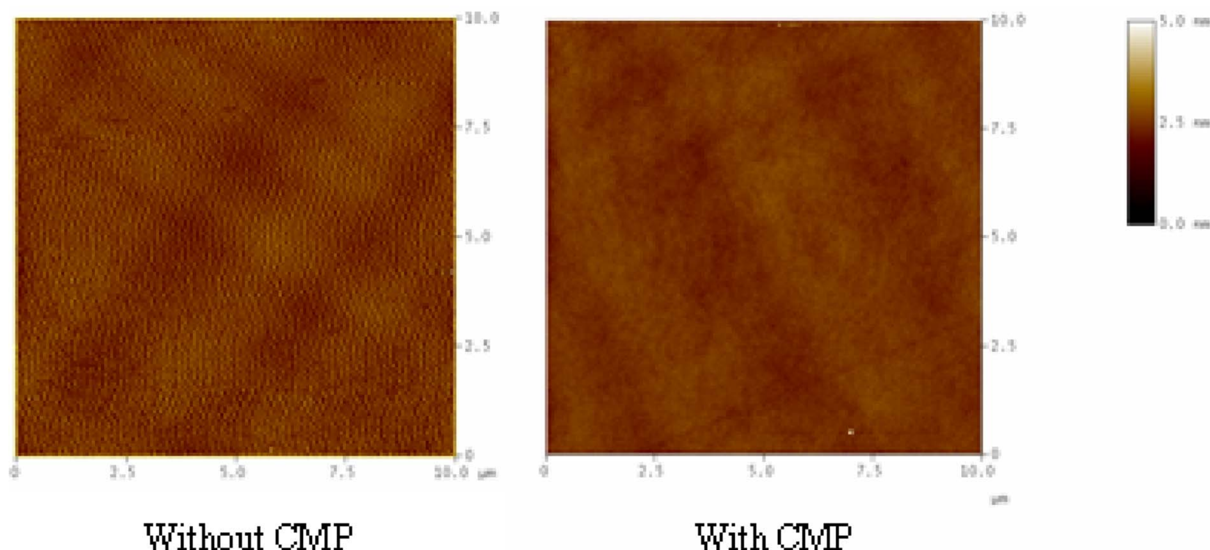

Figure 4. AFM images of strained-Si surfaces without and with the CMP process. The rms values are 0.6 and 1.8 nm, respectively.

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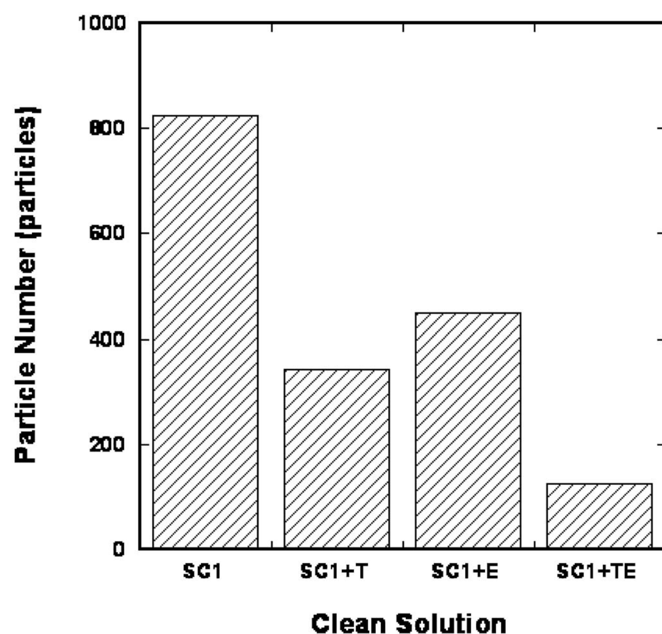

Figure 5. Particle residual number on post-CMP cleaning surfaces of SiGe buffer layers in different solutions.

is obviously seen that SC1 and SC1 + T samples exhibit the second breakdown effect, possibly due to the metallic and particle containment shown in Fig. 5 and 6. Figure 8 shows the Weibull plot of leakage current measured at 3 V. The breakdown voltage distribution is shown in Fig. 9. A constant current stressing is used to investigate the gate oxide integration. The charge to breakdown (Q_{bd}) measurements were performed on the post-CMP cleaning samples (see Fig. 10). The distribution for solution SC1 + TE shows high Q_{bd} that can be attributed to efficient removal of the particle and metal contaminations on strained-Si MOS capacitors. We also applied it in MOSFET fabrications. The output characteristics of devices with channel length of 5 μm are shown in Fig. 11, and the drain current increased about 10% between SC1 and SC1 + TE samples. The novel cleaning solutions with TMAH and EDTA showed the improvements which indicated that this solution for post-CMP on SiGe virtual substrates is a critical technique for developing high-performance strained-Si MOSFETs.

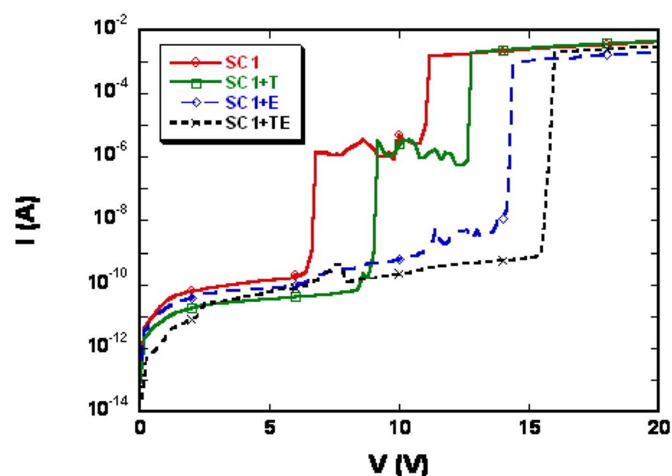

Figure 7. The current vs voltage characteristic of MOS capacitors with 20 -nm TEOS oxide on the strained Si with different cleaning methods.

Conclusions

We have investigated planarization of rough surfaces of strain-relaxed $Si_{0.8}Ge_{0.2}$ buffer layers by CMP and post-CMP cleaning. It was found that a softened polish pad can eliminate SiGe surface roughness. The optimum conditions can achieve a strained-Si surface roughness of 0.6 nm. For the post-CMP cleaning process, various cleaning solutions were applied to the SiGe buffer layer. By adding the surfactant (TMAH) and chelating agent (EDTA) into the diluted ammonium solution, removal efficiency of particles and metallic impurities is increased. The electrical performances of capacitors such as breakdown voltage, leakage current, and Q_{bd} are significantly improved for post-CMP cleaning. Furthermore, the

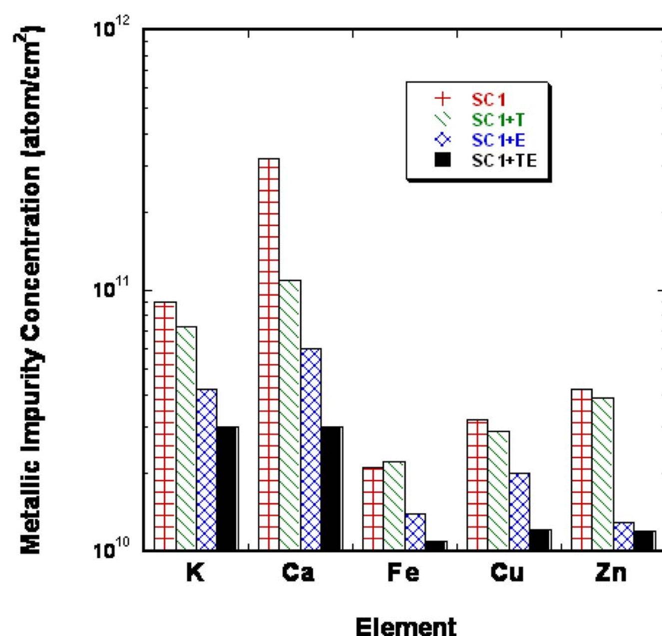

Figure 6. The metallic contaminant concentration on SiGe buffer layers by TXRF.

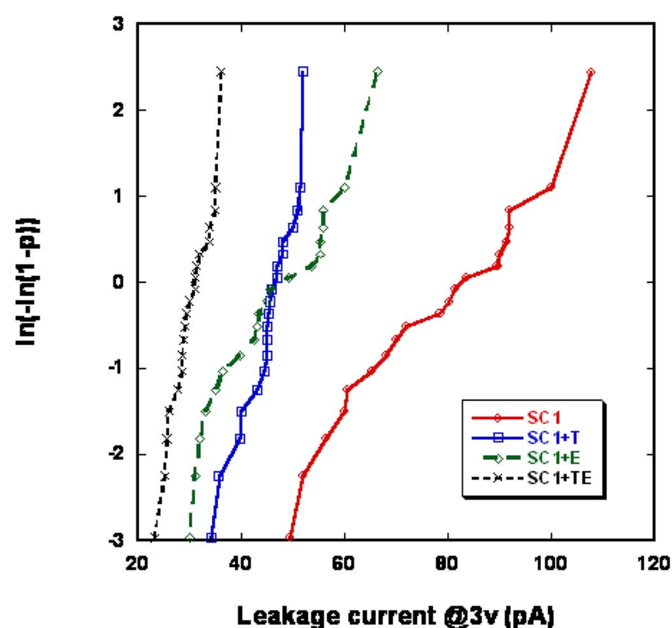

Figure 8. The cumulative distribution of leakage current of MOS capacitors with different cleaning methods.

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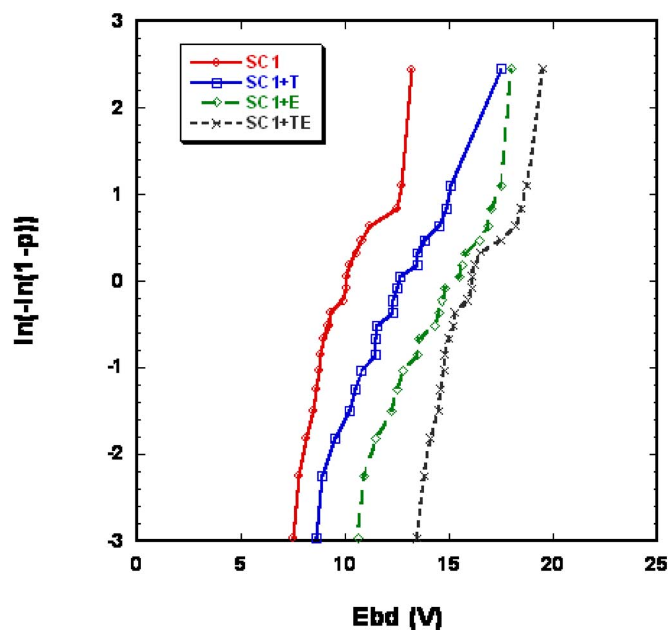

Figure 9. The breakdown voltage distribution of MOS capacitors.

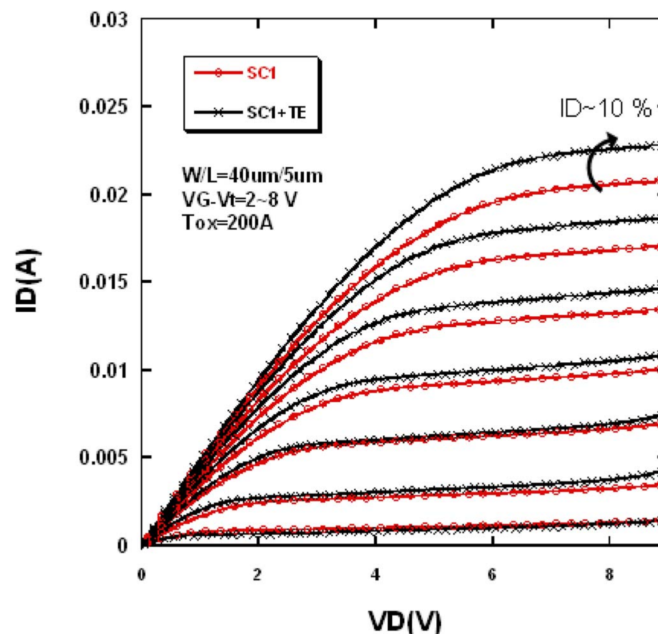

Figure 11. The 10% current enhancement between SC1 and SC1 + TE samples.

optimal condition of the SC1 + TE sample increased about 10% in drive current. This post-CMP cleaning process is useful for planarization of strain-relaxed SiGe virtual substrates in MOSFET applications.

Acknowledgment

This work was supported by the joint project of Electronics Research and Service Organization and the Industrial Technology Research Institute of Taiwan through contract no. C93079.

National Chiao Tung University assisted in meeting the publication costs of this article.

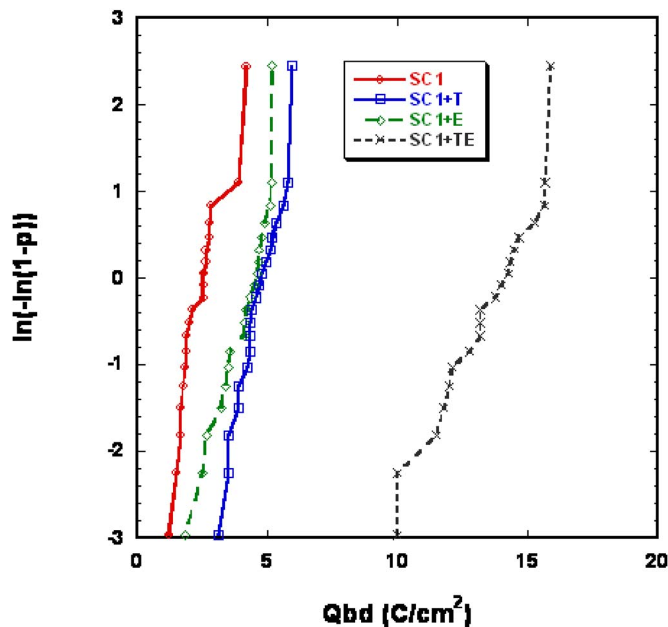

Figure 10. The charge-to-breakdown of MOS capacitors under constant current stress in four kinds of different solutions.

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