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A Quantum Trap MONOS Memory Device Using AlN

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We report a IrO_2–HfAlO–AlN–SiO_2–Si MONOS device that displays excellent characteristics in terms of speed (100 μs at ±13 V for program/erase) and memory window (3.7 V) at 85°C operation. This device also shows good 10-year extrapolated data retention with a large 1.9 V window at 85°C. The achieved performance compares well with the best reported memory device data.
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The [poly-Si/metal]-oxide-nitride-oxide-silicon (SONOS/MONOS) device[1-6] is a promising nonvolatile memory suitable for downscaling below 20 nm.[2] Discrete quantum traps are used rather than the continuous charge storage in poly-Si floating gate flash memory, which gives better data retention and is useful for 2 bits/cell. The high density and small size of such traps in SONOS/MONOS may have an advantage over quantum dot memory where the dots are nonuniform and have typical dimensions of ~5 to 10 nm. Goals for improving memory device performance include better program/erase (P/E) speed, memory window, and data retention. A large memory window is important in multilevel data storage,[4] which is beyond the current 2 bits/cell technology.

In this paper, we demonstrate an IrO_2–HfAlO–AlN–SiO_2–Si MONOS memory device to meet the requirements mentioned above. At an elevated temperature of 85°C, a large memory window of 3.7 V was initially obtained along with a speed of 100 μs and ±13 V P/E. The data suggested a 1.9 V window from 10-year extrapolated data retention. Good endurance was evident from the small 0.3 V threshold voltage (V_{th}) increase, within a 3.7 V memory window, after 10,000 P/E cycles. Therefore, fast 100 μs speed, large memory window, good data retention, and cycling endurance can be simultaneously obtained in the SiO_2/AlN/HfAlO/IrO_2 memory device. Such excellent device performance is among the best in the literature.[2-4] The good memory device performance is primarily due to the deeper energy charge trapping in the AlN layer,[7-9] which yields a large memory window and good data retention together with low leakage through the thin 2.8 nm SiO_2 barrier. The fast erase speed, which is the bottleneck for P/E and is much slower than the program speed, is due to the high-κ property of the AlN (κ = 10) trapping layer[7-9] and the HfAlO (κ = 17) barrier, which gives higher electric field across the SiO_2 tunnel layer. The high work function of 5.1 eV IrO_2 metal-gate[10] also plays an important role in enabling a fast erase function by reducing the leakage current through the thin HfAlO barrier.

Experimental

We have studied the trapping capability of various high-κ dielectrics such as Si_3N_4 and AlN.[7-9] After device isolation, the 16 nm AlN was deposited by physical vapor deposition (PVD). For comparison, the capacitor with the same thickness (16 nm) Si_3N_4 was also fabricated. A 400°C anneal under N_2 ambient was used to reduce the leakage current via defects. After standard process steps the Al-metal/high-κ/Si metal–insulator–semiconductor (MIS) capacitors were formed, shown schematically in Fig. 1a. For the IrO_2–HfAlO–AlN–SiO_2–Si MONOS devices (Fig. 1b), a 2.8 nm thermal SiO_2 was first grown at 850°C in dilute O_2.Then a 12 nm AlN trapping layer was deposited by PVD, followed by 13 nm HfAlO deposition by atomic layer chemical vapor deposition (ALCVD), and 50 nm IrO_2 deposition by PVD.[10] After standard processing, the MONOS device was created by self-aligned phosphorous ion implantation and 950°C rapid thermal anneal (RTA) activation to form the source/drain (S/D) region of an n-type metal oxide semiconductor field effect transistor (n-MOSFET). The resulting structure is shown in Fig. 1c. The memory devices were characterized by different P/E times, retention tests, and cycling endurance at 25 or 85°C.

Results and Discussion

Single trapping layer MIS capacitor.— Figures 2 and 3 show the measured capacitance–voltage (C–V) characteristics of high-κ AlN and Si_3N_4 MIS capacitors, respectively, after applying +4 or −4 V for 0.1–100 ms. For AlN MIS devices the memory function was obtained from the positive and negative shifts of the C–V curves, corresponding to the different polarities of the applied voltages. The shift of C–V curves saturates as the P/E time is increased >1 ms, suggesting a 1 ms switching time. A memory window of 0.5 V was obtained at ±4 V P/E for 1 ms, which can be increased using the MONOS structure with additional quantum well (QW) confinement from the two barriers, as depicted in Fig. 1b.

In contrast, an Al/Si_3N_4/Si MIS capacitor, fabricated with the same thermal cycle process as the AlN MIS device, showed only a few millivolt changes in the C–V curves. It is well known that good memory functions can be obtained in Si_3N_4 MONOS devices through additional programmed charge confinement within the Si_3N_4 QW formed by two SiO_2 barriers. Therefore the poor memory capability in the single-layer Si_3N_4 MIS capacitor may be due to the charge leakage out to the metal–gate and Si substrate, after removing the applied voltages. Note that the equivalent oxide thickness (EOT) of the Si_3N_4 is larger than for the AlN layer due to the smaller κ value and capacitance density (3.5 fF/μm^2 vs 4.5 fF/μm^2 for AlN capacitor). This suggests that the traps in Si_3N_4 are either shallower, in energy, or lower in density than those for AlN but are still the most important properties for the trapping layer in a MONOS device.

We also measured the retention characteristics of a single-layer AlN MIS capacitor. As shown in Fig. 4, a good retention time of 10,000 s is shown with a small change in the memory window, after the 1 ms ±4 V P/E. This simple AlN capacitor, fabricated with only a 400°C thermal budget, can be integrated into very large scale integration (VLSI) as a backend process. The high capacitance density of ~5 fF/μm^2 is useful for analog/radio frequency (r/f) applications and is ~5 times larger than capacitors currently provided in

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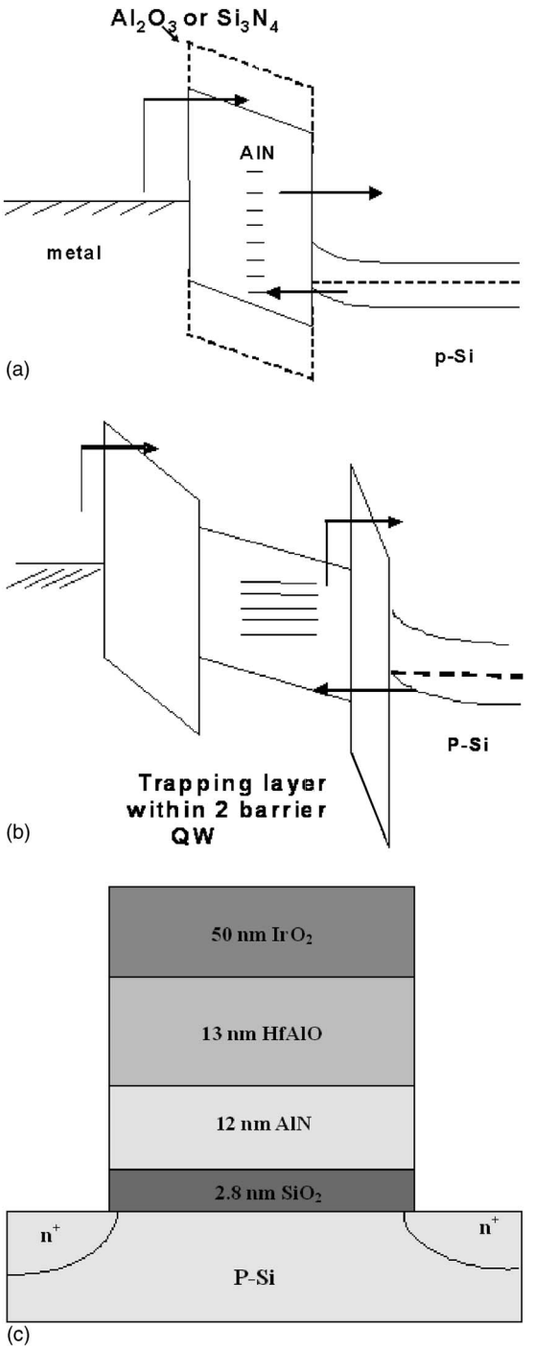


Figure 1. Schematic structures for (a) a metal-gate/high-κ/Si MIS capacitor and (b) an IrO_2–HfAlO–AlN–SiO_2–Si MONOS device with discrete quantum traps.

an integrated circuit (IC) foundry. The 10^4 s retention time in the high-density AlN capacitors can be used as devices intermediate between static and dynamic RAM.

MONOS memory device.— To increase the memory window and data retention further, a MONOS device structure is required, having additional quantum confinement within high energy barriers as in Fig. 1b. Figure 5 shows the C–V hysteresis characteristics of the MONOS capacitor. A large memory window of 7–9 V was obtained with applied P/E voltages of ±11 to ±13 V. Such a memory window is significantly larger than that of a single-layer AlN MIS device due

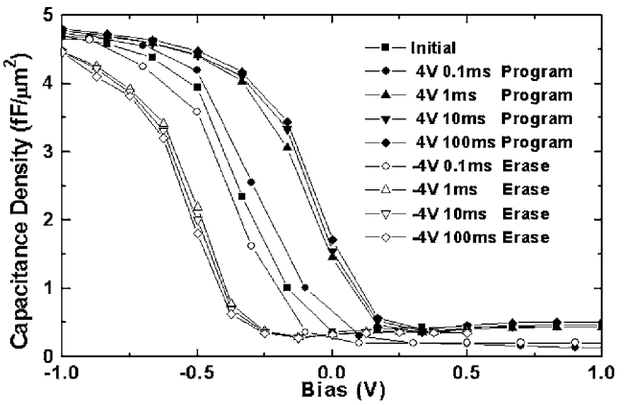


Figure 2. C–V characteristics of an Al/AlN/Si MIS capacitor. The memory device function is obtained by applying program and erase voltages of +4 and −4 V, respectively.

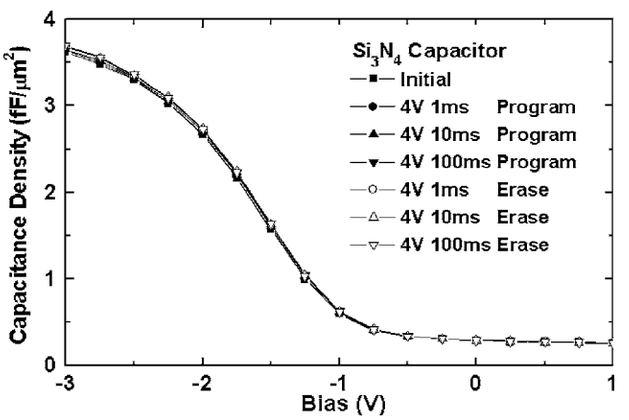


Figure 3. C–V characteristics of an Al/Si_3N_4/Si MIS capacitor. In contrast, a small C–V shift was shown after applying voltages of +4 and −4 V to an Al/AlN/Si device, which suggests shallower trap energy or lower trap density in the Si_3N_4 MIS device.

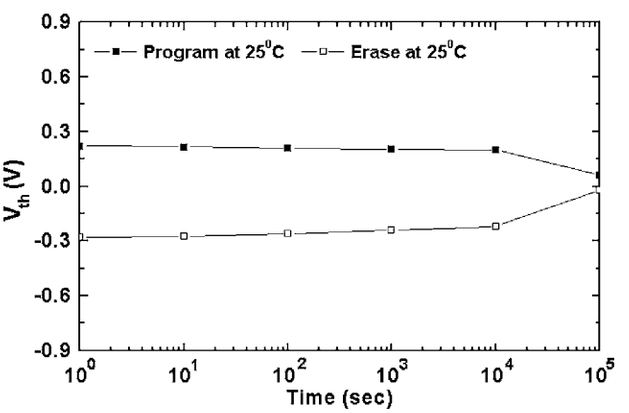


Figure 4. The retention characteristics of an Al/AlN/Si MIS capacitor obtained from C–V curves. The data was measured after ±4 V P/E voltages were applied for 1 ms.

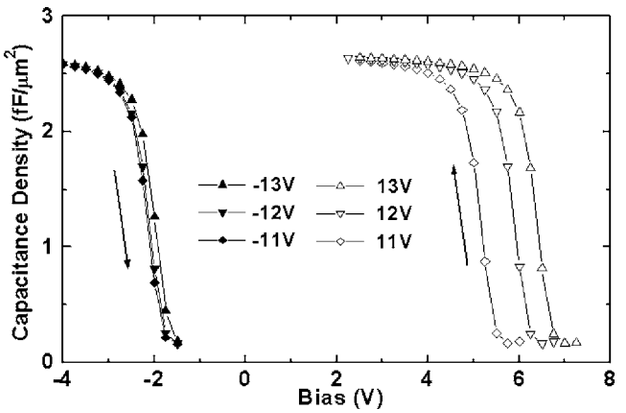


Figure 5. The C–V hysteresis characteristics of an IrO_2–HfAlO–AlN–SiO_2–Si MONOS memory device.

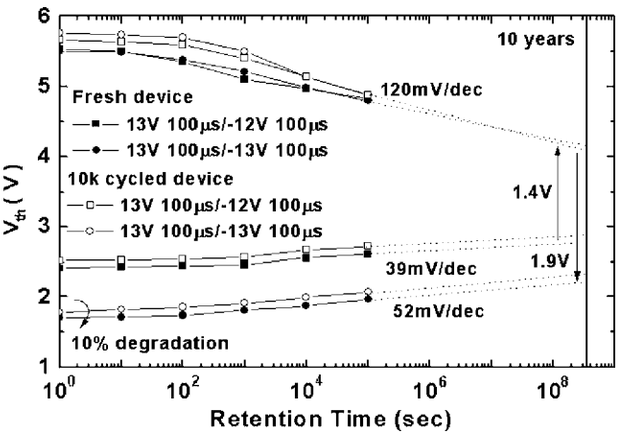
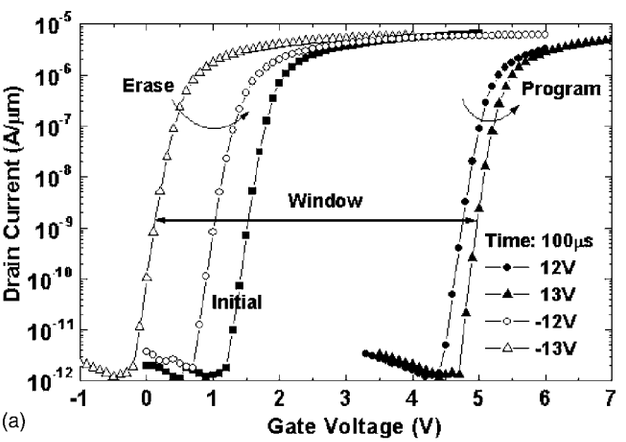


Figure 7. The data retention of fresh and 10 K-cycled AlN MONOS memory devices at 85°C.

to the charge confinement in the AlN traps within the HfAlO and SiO_2 barriers. In addition, use of a thinner 12 nm AlN trapping layer in MONOS memory devices is to give a smaller EOT and lower operation voltage. Figures 6a and b show the I_d–V_g characteristics of a MONOS device with 10 μm gate length and the threshold voltage (V_{th}) as a function of P/E time from the peak g_m of the linear I_d–V_g, respectively. Therelative large initial V_{th} of 2.1 V may be due to intrinsic properties or process-induced charges in the AlN layer,



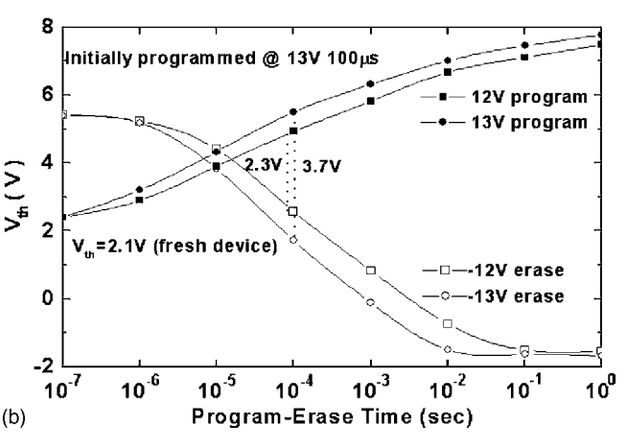


Figure 6. (a) The measured I_d–V_g characteristics of a MONOS device and (b) the detailed threshold voltage (V_{th}) program and erase characteristics from the peak g_m of an I_d–V_g plot.

because V_{th} of an n-MOSFET is only 0.2 V. V_{th} changes almost linearly with increasing program and erase times, although the V_{th} saturates when the erase time reaches 10–100 ms. This is due to the limited charge storage for the initial programming at 13 V for 100 μs. The large memory window of 2.3 or 3.7 V appears when the P/E time reaches 100 μs at ±12 or ±13 V. This is comparable with the best erase times in the literature,[2-4] and is important because of the large memory window and low P/E voltage. The operation speed of a nonvolatile Flash memory device is limited by the slow erase time, because programming can be achieved rapidly through the hot-carrier injection with a large current. The fast erase time arises from the high electric field across the thin 2.8 nm tunnel SiO_2 due to the high-κ HfAlO (κ = 17) and AlN (κ = 10) and the continuity of D ($\varepsilon_0 \kappa E$). The fast erase speed is also related to the high work function IrO_2 metal gate and low charge injection over the thin HfAlO barrier.[10]

Figure 7 shows the retention behavior of an AlN MONOS device at 85°C. Initially ΔV_{th} was 3.1 or 3.7 V under 100 μs 13 V program and −12 V or −13 V erase, and gave a good 10-year memory window of 1.4 or 1.9 V, respectively, and a decay rate of 120 (1-state) and only 39 mV/dec (0-state). The good data retention arises from the ionic-bond-related trapping capabilities of Al–N.[7-9] The good retention is also due to the fast (100 μs) switching speed; this helps to reduce the stress degradation of the 2.8 nm tunnel oxide which is involved in confining the stored charge in the QW. Table I summarizes the important memory device characteristics. The AlN MONOS device shows a fast erase time, a good 10-year retention memory window at 85°C, and retention decay rates comparable with published data.[2,3] These excellent device characteristics are due to high trapping abilities of AlN, the high work function IrO_2 gate, and the low voltage drop across the high-κ HfAlO barrier.

Conclusion

We have demonstrated a novel AlN MONOS memory which uses an IrO_2 metal gate and shows a large initial memory window of 3.7 V at ±13 V and a 100 μs P/E time. Extrapolated data suggests good 10-year data retention and only 10% ΔV_{th} degradation after 10^4 P/E cycles at 85°C.

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Table I. Comparison of memory characteristics of this work with published data.

	P/E condition for retention		V_{th} at 85°C (V)		
	Program	Erase	Initial	10 years	85°C decay rate (mV/dec)
This work	13 V 100 μs	13 V 100 μs	3.7	1.9	172
Tri-gate $SiO_2/Si_3N_4/SiO_2$/poly (Infineon, VLSI'04[2])	11.5 v 3 ms	11.5 V 100 ms	1.2	1.1 (25°C)	25 (25°C)
MONOS $SiO_2/Si_3N_4/Al_2O_3$/TaN (Samsung, IEDM'03[3])	13.5 V 100 μs	−13 V 10 μs	4.4	2.07	215

References

1. M. H. White, D. A. Adams, and J. Bu, *IEEE Circuits Devices Mag.*, **16**, 22 (2000).
2. M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R. J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch, *Symposium on VLSI Technology*, p. 244 (2004).
3. C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, *Tech. Dig. - Int. Electron Devices Meet.*, **2003**, 613.
4. Y. K. Lee, S. K. Sung, J. S. Sim, C. J. Lee, T. H. Kim, S. H. Lee, J. D. Lee, B. G. Park, D. H. Lee, and Y. W. Kim, *Symposium on VLSI Technology*, p. 208 (2002).
5. T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, *Symposium on VLSI Technology*, p. 27 (2003).
6. A. J. Walker, S. Nallamothu, E.-H. Chen, M. Mahajani, S. B. Herner, M. Clark, J. M. Cleeves, S. V. Dunton, V. L. Eckert, J. Gu, S. Hu, J. Knall, M. Konevecki, C. Petti, S. Radigan, U. Raghuram, J. Vienna, and M. A. Vyvoda, *Symposium on VLSI Technology*, p. 29 (2003).
7. A. Chin, C. H. Lai, B. F. Hung, C. F. Cheng, S. P. McAlister, C. X. Zhu, M.-F. Li, and D. L. Kwong, *5th Non-Volatile Memory Technology Symposium Digest*, p. 18 (2004).
8. C. H. Lai, C. F. Lee, A. Chin, C. Zhu, M. F. Li, S. P. McAlister, and D. L. Kwong, *IEEE RF IC Symposium Digest*, p. 259 (2004).
9. C. H. Lai, B. F. Hung, Albert Chin, C. Zhu, M. F. Li, S. P. McAlister, and D. L. Kwong, *IEEE Electron Device Lett.*, **26**, 148 (2005).
10. D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, p. 181.