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PolySi-SiO_2-ZrO_2-SiO_2-Si Flash Memory Incorporating a Sol-Gel-Derived ZrO_2 Charge Trapping Layer

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In this paper, we propose a method for depositing the charge trapping layer of a high-*k* polySi-SiO_2-ZrO_2-SiO_2-Si (SOZOS) memory device. In this approach, the trapping layer was formed through simple two steps: (*i*) spin-coating of the $ZrCl_4$ precursor and (*ii*) rapid thermal annealing for 1 min at 900°C under an oxygen atmosphere. The morphology of the ZrO_2 charge trapping layer was confirmed through X-ray photoemission spectroscopy analysis. The sol-gel-derived layer exhibited improved charge trapping in the SOZOS memory device, resulting in a threshold voltage shift of 2.7 V in the I_d-V_g curve, P/E (program/erase) speeds as fast as 0.1 ms, good data retention up to 10^4 s (only a 5% charge loss due to deep trapping in the ZrO_2 layer), and good endurance (no memory window narrowing after 10^5 P/E cycles).
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The first floating-gate (FG) nonvolatile semiconductor memory was invented by Sze and Kahng in 1967.[1] Conventional FG memory uses polysilicon as a charge-storage layer surrounded by the dielectric.[2] Although floating-gate structures can achieve high densities and good program/erase (P/E) speeds and exhibit good reliability in portable flash memory devices, there are concerns regarding the ability to scale up their production.[3] When the tunneling oxide thickness is below 10 nm, the storage charge in the FG leaks readily because defects form in the tunneling oxide after repeated write-erase cycles or through direct tunneling of the current.

PolySi-oxide-nitride-oxide-silicon (SONOS) memory devices have been studied recently as an approach to solving the issue of scaling FG memory.[3] Because of their spatially isolated deep-level traps, SONOS memories exhibit better charge retention than do FG memories that have a bitcell tunneling oxide layer thinner than 10 nm. As a result, a single defect in the tunneling oxide will not cause the discharge of the memory cell.[3] SONOS memory devices use silicon nitride as a charge trapping layer; the conduction band offset between the tunneling oxide and nitride is 1.05 eV. When a positive voltage is applied on the gate, the band bends downward so that the electrons in the Si subconduction band will tunnel through the tunneling oxide and a portion of the nitride will become trapped in the charge trapping layer. Before they become trapped in the nitride, the electrons must tunnel through a portion of the nitride, which degrades the program speed. In addition, because the conduction band offset of the nitride is only 1.05 eV, back tunneling of the trapped electron may also occur. To solve these problems, high-*k* materials are potential candidates to replace the traditional silicon nitride as the charge trapping layer.

The advantages of using high-*k* materials are the larger band offset with the tunneling oxide and the greater number of trapping sites than those found in silicon nitride. For an HfO_2 high-*k* material, the conduction band offset between the tunneling oxide and HfO_2 is 1.6 eV. When programming, the electron will tunnel through a shorter distance in HfO_2 than in the nitride to become trapped. This feature can be exploited to achieve high P/E speeds. Thus, it will be beneficial to use a high-*k* material as the charge trapping layer in a SONOS-type memory device, provided that there are many deep-level trapping sites in the high-*k* material.[4] The electron trap levels of ZrO_2 (Ref. 5) and JVD HfO_2 (Ref. 6) are 1.0 and 1.5 eV, respectively, which are both deeper than that of the nitride (0.8 eV). It is desirable to choose a high-*k* material having a large band offset with the tunneling oxide and a deep trapping level for use as the charge trapping layer to achieve high P/E speeds and good reliability, respectively. ZrO_2 has a dielectric constant of 25, a wide bandgap, good thermal stability, and a high trap site density; it is also suitable for SONOS-type memory applications.

Many technologies have been developed recently for the deposition of high-*k* layers onto tunneling oxides,[7-10] including atomic layer deposition (ALD), metallorganic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD). In the ALD method, $ZrCl_4$ and H_2O are used to prepare the ZrO_2 films. For the PVD process, a zirconium metal target is used for sputtering under ambient oxygen to deposit the ZrO_2 films. In the CVD method, $ZrCl_4$ is used as a precursor to deposit ZrO_2 films. Recently, we proposed the first so-called sol-gel spin-coating method for the deposition of the thin film.[11] Sol-gel spin-coating methods use metal halides hydrolyzed in organic or colloidal solvents to form precursor compounds that undergo hydrolysis, condensation, and polymerization to form metal-oxide networks. The advantages of using sol-gel methods to fabricate high-*k* films are that they are cheaper than ALD, PVD, and MOCVD approaches, and that various types of thin films can be synthesized. To the best of our knowledge, sol-gel spin-coating of a high-*k* film has yet to be reported for the preparation of charge trapping layers for flash memory devices.

In this paper, we describe the fabrication of a polySi-SiO_2-ZrO_2-SiO_2-Si (SOZOS) flash memory device prepared through the deposition of $ZrCl_4$ using the sol-gel spin-coating method and subsequent rapid thermal annealing (RTA). We performed physical and electrical analyses, including X-ray photoemission spectroscopy (XPS), I_d-V_g, retention, and P/E speed measurements, to evaluate the performance of the sol-gel ZrO_2 films for their potential use as charge trapping layers in SOZOS memory devices.

Experimental

$ZrCl_4$ (99.5%, Aldrich, USA) was used as the synthetic precursor of the zirconia. A mother sol solution was first prepared by dissolving $ZrCl_4$ in isopropanol (IPA; Fluka; water content $<0.1\%$) under vigorous stirring in an ice bath. The sol solution was obtained by fully hydrolyzing $ZrCl_4$ with a stoichiometric quantity of water in IPA to yield a Zr:IPA molar ratio of 1:1000.

The fabrication of the sol-gel spin-coated SOZOS memory began with LOCOS isolation process on p-type 150 mm silicon (100) substrate. At first, a 4 nm tunneling oxide layer was grown thermally at 925°C through furnace oxidation. The Zr:IPA solution (molar ratio: 1:1000) was coated using a spin-coater at 3000 rpm for 60 s at 25°C. A TEL Clean Track model-MK8 (Japan) spin-coater was used. The as-deposited thin film was initially baked at 200°C for 10 min to perform densification, followed by high-*k* RTA for 1 min in an O_2 atmosphere to form the ZrO_2 charge trapping layer. The film thickness, measured using an ellipsometer, was 10 nm. A 30 nm thick blocking oxide was deposited using high-density-plasma-enhanced chemical vapor deposition (HDPCVD), followed by deposition of a poly-Si gate (200 nm). After gate deposition, the following processes were applied to fabricate the SOZOS memory:

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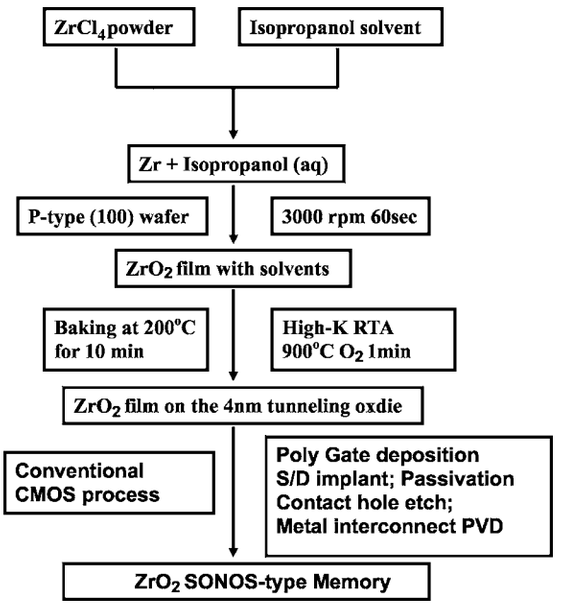

Figure 1. Process flow chart for the fabrication of the ZrO_2 SOZOS memory.

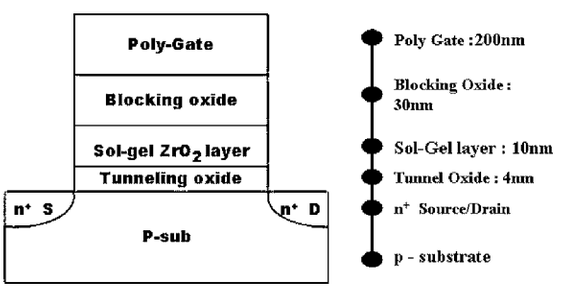

Figure 2. Structure of the ZrO_2 SOZOS memory.

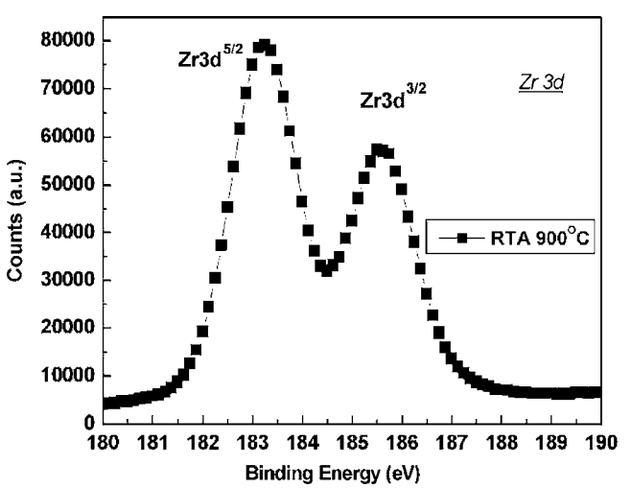

Figure 3. XPS curve of the sol-gel-derived ZrO_2 thin film.

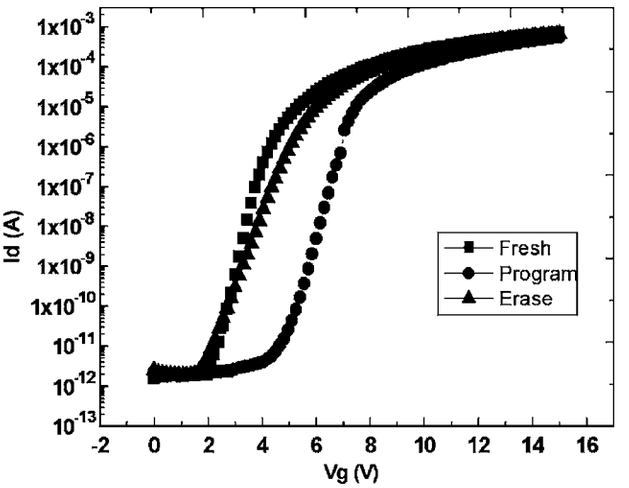

Figure 4. I_d-V_g curve of the sol-gel-derived ZrO_2 SOZOS memory.

gate patterning, source/drain (S/D) implanting of the dosage of phosphorus 5E15 20 KeV, S/D activation, CVD of a passivation oxide, and the subsequent MOS processes. The process flow and the structure of the ZrO_2 charge trapping layer in the SOZOS flash memory are depicted in Fig. 1 and 2, respectively.

Results and Discussion

We used XPS to analyze the chemical composition of the elements of the film. Figure 3 presents the high-resolution spectrum displaying the Zr 3d peaks of the film; two typical peaks, Zr $3d_{5/2}$ (183.2 eV) and Zr $3d_{3/2}$ (185.6 eV), are observed clearly for the RTA sample, suggesting that the complete structural formation of ZrO_2 had occurred.[11]

Figure 4 displays the I_d-V_g curve of the ZrO_2 SOZOS memory. We used channel hot-electron injection (CHEI) to program and the band-to-band hot hole (BTBHH) method to erase the device. We observed that after programming at values of V_g and V_d of 15 and 10 V, respectively, for 1 ms, the threshold voltage (V_{th}) shifted from 3.45 V in the fresh state to 6.15 V in the programed state. This V_{th} shift of 2.7 V satisfies a main requirement of a typical memory device: i.e., a memory window larger than 0.7 V. The electron trapping can be explained by considering the band diagram presented in Fig. 5, in which the conduction band offset between the tunneling oxide and the ZrO_2 charge trapping layer is 1.6 eV. When the electrons in the conduction band of the silicon substrate gain enough

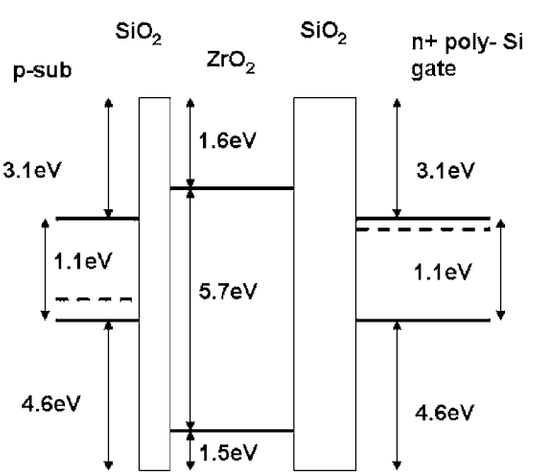

Figure 5. Band diagram of the ZrO_2 SOZOS memory.

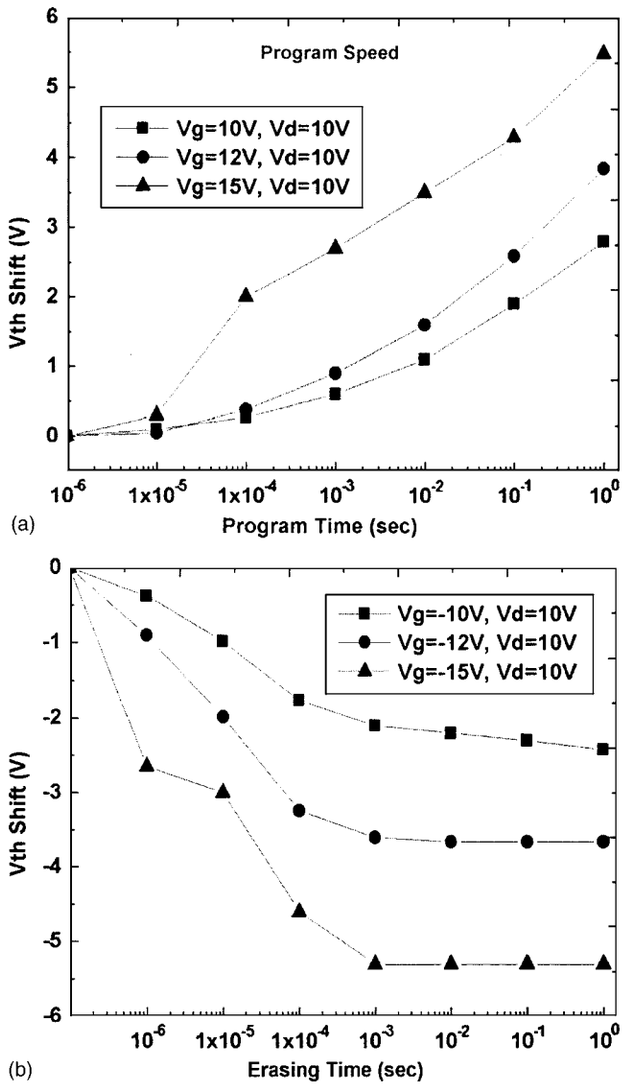

Figure 6. (a) Program and (b) erase speeds of the sol-gel-derived ZrO_2 SOZOS memory.

energy from the applied voltage to cross the barrier height, they can also cross the tunneling oxide to become trapped in the ZrO_2 layer. This electron trapping causes the I_d-V_g curve (in Fig. 4) to move to the right, and the value of V_{th} to increase, after programming. In addition, in the I_d-V_g curve we observe a subthreshold slope degradation of the erased cell and that the erased curve did not match the original fresh curve. The subthreshold slope degradation of the erased cell may have arisen because of BTBHH injection damaging the bottom oxide.[12,13] There are two possible reasons why the erased curve did not match the original fresh curve. One is that the distribution of trapped electrons programed by CHEI did not match with the holes formed by BTBHH; as a result, the holes injected during erasing may not have completely annihilated all of the trapped electrons, leading to some negative charge remaining in the ZrO_2 layer to result in the slight increase in the value of V_{th}.[13,14] The other reason is because some electrons became trapped in the deep trap level of ZrO_2; i.e., they became hard to escape from the trapping site. This situation is beneficial for the memory device retention.

Figure 6 displays the P/E speed of the ZrO_2 SOZOS memory. Figure 6a indicates the program characteristics for three different stress conditions: values of V_g of 10, 12, and 15 V, respectively, at a value of V_d of 10 V; the mechanism was also that of CHEI. At

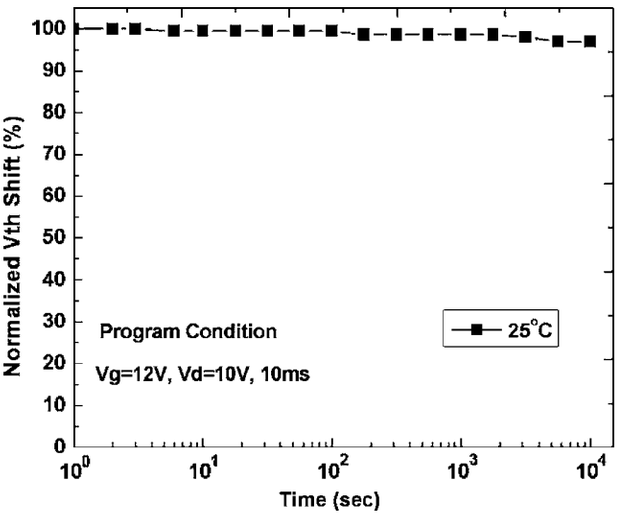

Figure 7. Charge retention curve of the sol-gel-derived ZrO_2 SOZOS memory.

values of V_g and V_d of 15 and 10 V, respectively, for 0.1 ms, we observed a V_{th} shift of ca. 2 V. We found that as the applied gate voltage increased, the V_{th} shift also increased, because more "hot" electrons were generated when a larger gate voltage was applied and, thus, more electrons were capable of crossing the barrier height to become trapped in the ZrO_2 layer. The normalized erase speed curve is presented in Fig. 6b; the same explanation can be applied to the V_{th} shift observed as the gate voltage becomes increasingly negative. Using a regime of CHEI to program and BTBHH to erase can provide a high P/E efficiency.

Figure 7 depicts the retention characteristics of the ZrO_2 SOZOS memory, recorded at 25°C. We observed a small charge loss with time in the sol-gel SOZOS memory; a charge loss of only 5% occurred after 10^4 s. We suggest that this feature arose from the deep electron trap of the sol-gel ZrO_2 charge trapping layer. The small amount of charge loss may be due also to the direct tunneling current from the ZrO_2 charge trapping layer to the Si substrate, or to oxide trap-assisted tunneling resulting from the presence of defects in the tunneling oxide. Figure 8 highlights the endurance of

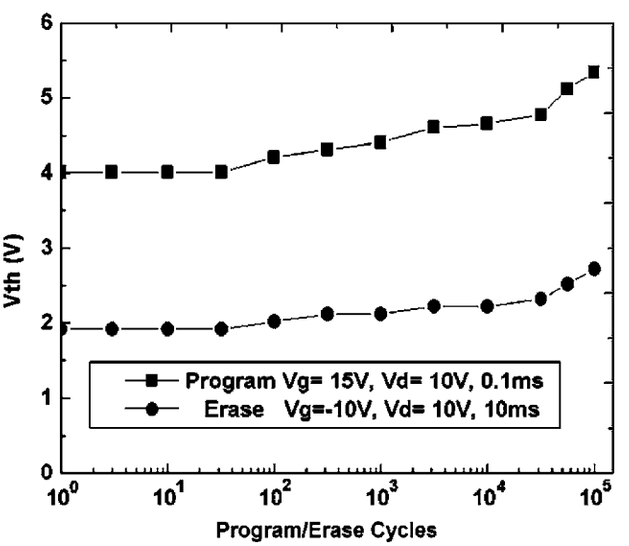

Figure 8. Endurance characteristics of the sol-gel-derived ZrO_2 SOZOS memory.

the sol-gel SOZOS memory, measured under the following conditions: programming at $V_g = 15$ V, $V_d = 10$ V, 0.1 ms; erasing at $V_g = -10$ V, $V_d = 10$ V, 10 ms. We observed a very small increase in the value of the erase V_{th}, in addition to no significant window narrowing, which was due to the formation of a deep trap level that made it difficult to erase all of the trapped electrons or to misalignment of the CHEI and BTBHH distribution profiles in the ZrO_2 layer. After 10^5 P/E cycles, the memory window still remained larger than 0.7 V. These findings suggest that our simple sol-gel process is suitable for use in the deposition of a ZrO_2 charge trapping layer and can be applied to the fabrication of SOZOS memory devices.

Conclusions

In this study, we fabricated a high-*k* SOZOS memory incorporating ZrO_2 as the charge trapping layer that was deposited through the sol-gel spin-coating of $ZrCl_4$ and subsequent RTA. We confirmed the formation of the charge trapping ZrO_2 thin-film layer through XPS measurements. We measured the I_d-V_g and P/E speed curves to demonstrate the memory performance. The data retention was high (only a 5% loss after 10^4 s) because of the deep trap level in the ZrO_2, and the endurance was good (up to 10^5 P/E cycles without narrowing of the memory window). Thus, this sol-gel spin-coating method is suitable for the deposition of a SOZOS high-*k* charge trapping layer.

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