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(54) **METHOD FOR GROWING EPITAXIES OF A CHEMICAL COMPOUND SEMICONDUCTOR**

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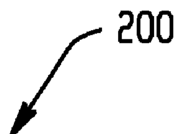
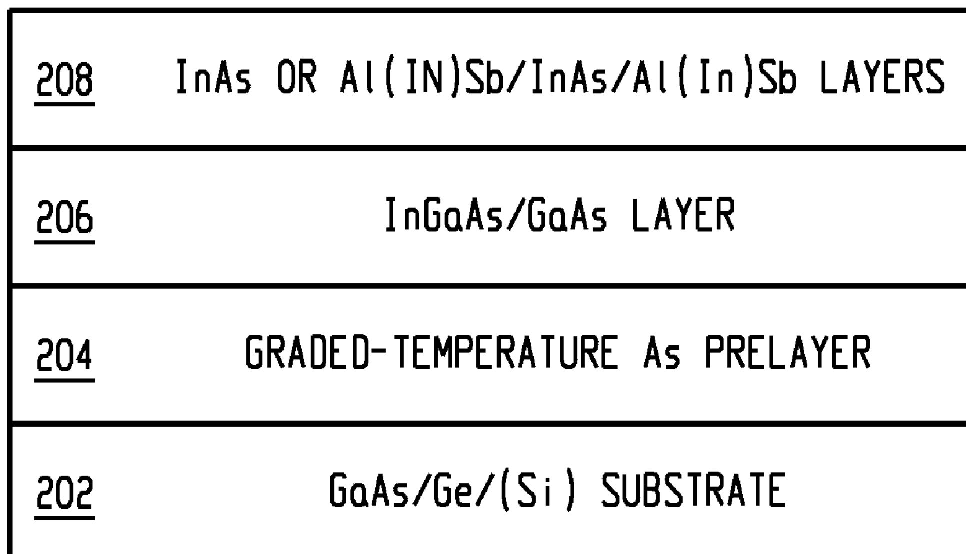
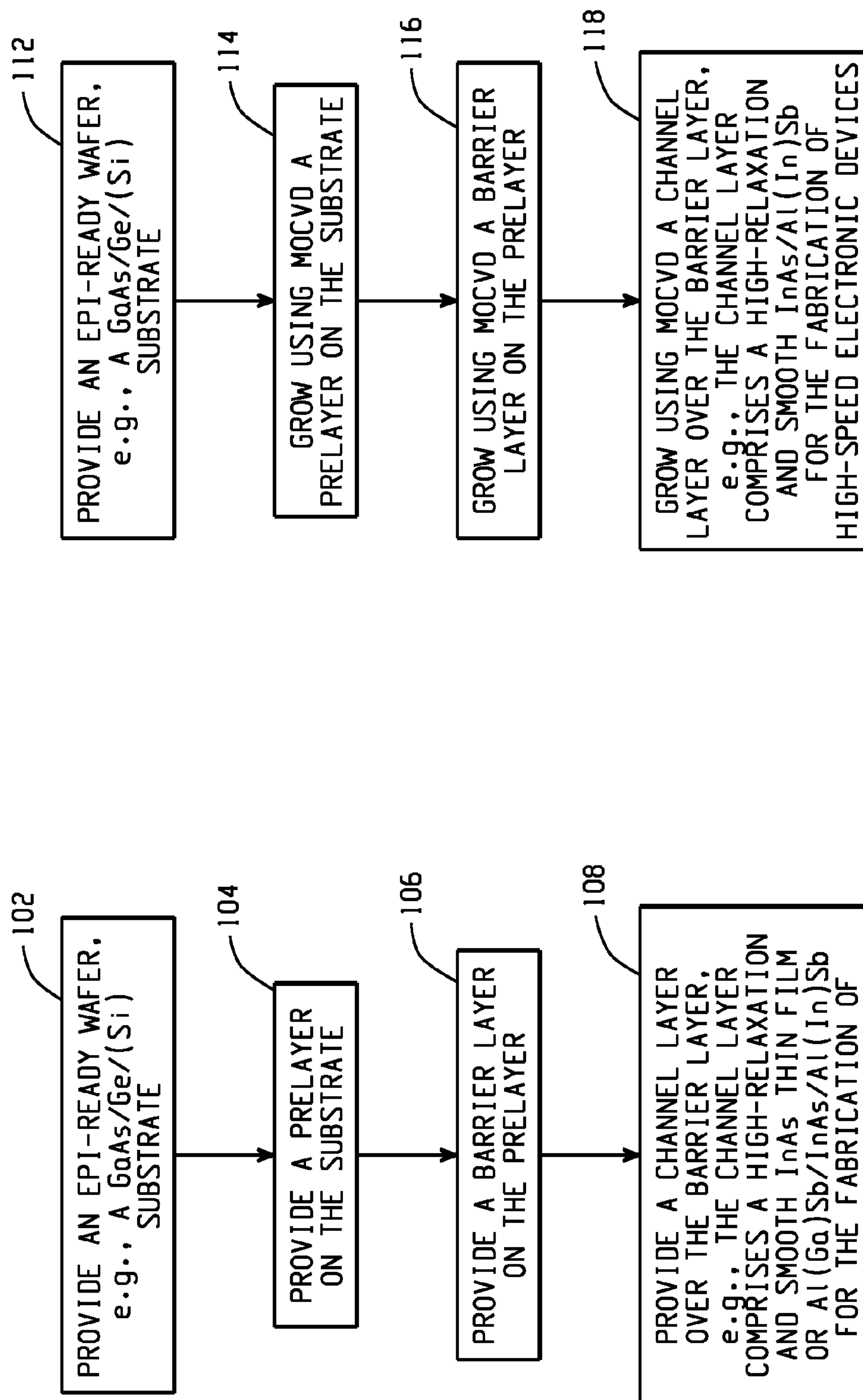
(57) **ABSTRACT**

Disclosed is a method of providing a chemical compound semiconductor channel layer on a substrate for use in a semiconductor fabrication process. The method comprises providing a prelayer over a substrate, providing a barrier layer over the prelayer, and providing an InAs or Sb-based channel layer over the barrier layer. The substrate comprises a gallium arsenide substrate, a silicon substrate, a germanium substrate, or a Ge/Si substrate. The prelayer comprises a graded-temperature arsenic prelayer grown with graded temperature ramped from 300 to 550° C. The barrier layer comprises GaAs with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or multiple GaAs-based layers. The channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures with one or more pairs. Also disclosed is a wafer comprising a prelayer grown over a substrate using MOCVD operations, a barrier layer grown over the prelayer using MOCVD operations, and a channel layer grown over the barrier layer using MOCVD operations.






112
PROVIDE AN EPI-READY WAFER, e.g., A GaAs/Ge/(Si) SUBSTRATE
114
GROW USING MOCVD A PRELAYER ON THE SUBSTRATE
116
GROW USING MOCVD A BARRIER LAYER ON THE PRELAYER
118
GROW USING MOCVD A CHANNEL LAYER OVER THE BARRIER LAYER, e.g., THE CHANNEL LAYER COMPRISES A HIGH-RELAXATION AND SMOOTH InAs/Al(In)Sb FOR THE FABRICATION OF HIGH-SPEED ELECTRONIC DEVICES
Fig. 2
102
PROVIDE AN EPI-READY WAFER, e.g., A GaAs/Ge/(Si) SUBSTRATE
104
PROVIDE A PRELAYER ON THE SUBSTRATE
106
PROVIDE A BARRIER LAYER ON THE PRELAYER
108
PROVIDE A CHANNEL LAYER OVER THE BARRIER LAYER, e.g., THE CHANNEL LAYER COMPRISES A HIGH-RELAXATION AND SMOOTH InAs THIN FILM OR Al(Ga)Sb/InAs/Al(In)Sb FOR THE FABRICATION OF HIGH-SPEED ELECTRONIC DEVICES
Fig. 1

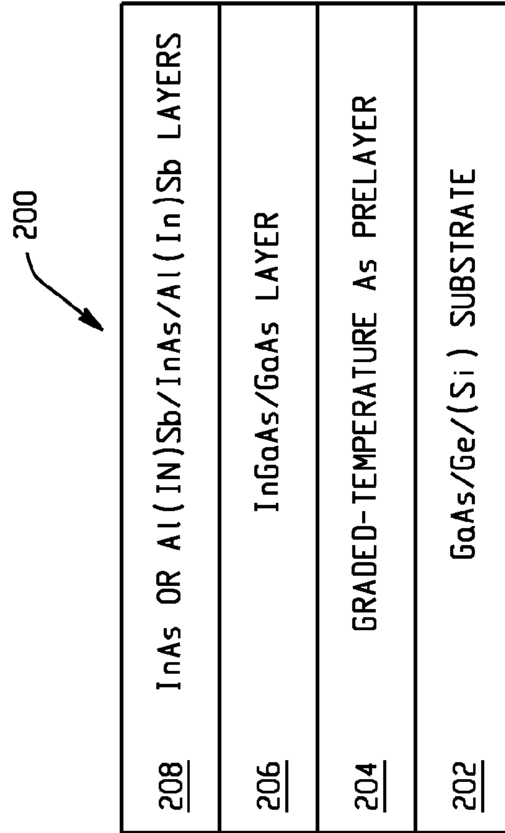


Fig. 4

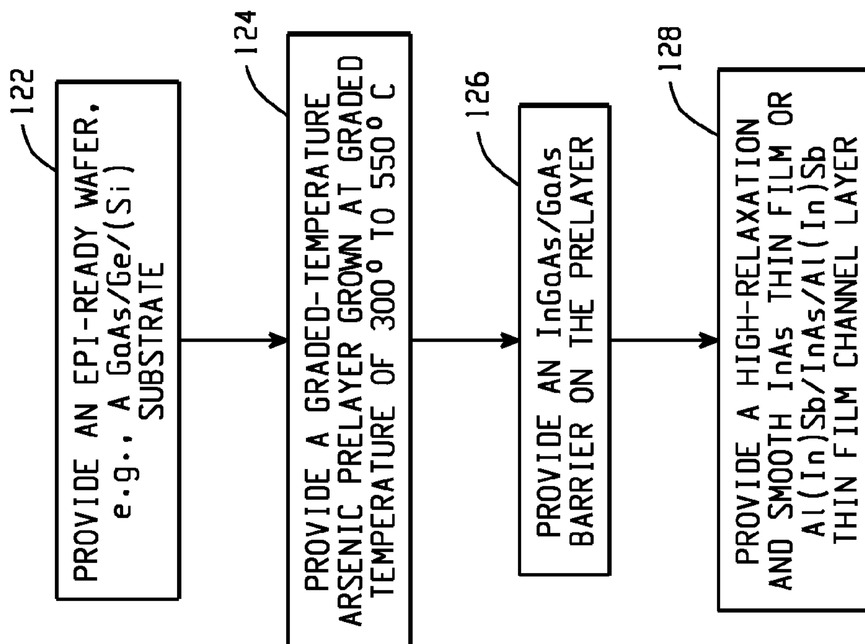


Fig. 3

METHOD FOR GROWING EPITAXIES OF A CHEMICAL COMPOUND SEMICONDUCTOR

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority from U.S. Provisional Application No. 61/953,963, filed on Mar. 17, 2014, entitled "Method For Growing Epitaxies Of A Chemical Compound Semiconductor," which is hereby incorporated into the present application by reference.

BACKGROUND

[0002] The technology described in this patent document relates to chemical compound semiconductors, and more specifically to forming a chemical compound semiconductor layer on a substrate.

[0003] Scaling of semiconductor devices, such as a MOSFET, has enabled continued improvement in speed, performance, density, and cost per unit function of integrated circuits over the past few decades. Improvements to the processes used in fabricating semiconductor structures can further the scaling of integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. **1** depicts an example process flow chart for creating a wafer that may be used in a semiconductor fabrication process.

[0006] FIG. **2** depicts another example process flow chart for creating a wafer that may be used in a semiconductor fabrication process.

[0007] FIG. **3** depicts another example process flow chart for creating a wafer that may be used in a semiconductor fabrication process.

[0008] FIG. **4** depicts a cross-sectional view of an example wafer that may be used in a semiconductor fabrication process.

DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Disclosed herein are structures and methods for growing type III-V materials as semiconductor layers on epi-ready wafers using MOCVD operations. In some examples, disclosed are techniques to grow In(Ga)As (or Al(Ga,In)Sb) epitaxy with high In content (~100%) or low In content on a GaAs substrate, a Ge substrate, a Si substrate and a Ge/Si substrate.

[0011] FIG. **1** depicts an example process flow chart for creating a wafer having a chemical compound semiconductor channel layer on a substrate that may be used in a semiconductor fabrication process. The example process comprises providing an epi-ready wafer, such as one comprising a GaAs substrate, a Ge substrate, a Si substrate, or a Ge/Si substrate (operation **102**). A prelayer is provided over the substrate (operation **104**). Next, a barrier layer is provided over the prelayer (operation **106**). Then, a chemical compound semiconductor channel layer is provided over the barrier layer (operation **108**). The example channel layer comprises a high-relaxation and smooth InAs thin film or In(Ga)As or Al(Ga)Sb/InAs/Al(Ga)Sb thin film for use in subsequent fabrication of high-speed electronic devices. This example process may allow for the use of a cheaper substrate, such as a Si, Ge, GaAs or Ge/Si substrate, instead of a GaSb or InP substrate and allow for In(Ga)As or Al(Ga)Sb/InAs/Al(Ga)Sb epilayers to be grown on the cheaper substrates.

[0012] FIG. **2** depicts another example process flow chart for creating a wafer having a chemical compound semiconductor channel layer on a substrate that may be used in a semiconductor fabrication process. The example process of FIG. **2** is similar to the example process of FIG. **1** and illustrates that each of the prelayer, barrier layer, and channel layer can be provided using metal organic chemical vapor deposition (MOCVD) operations. After providing an epi-reading wafer, such as one comprising a GaAs substrate, a Ge substrate, a Si substrate, or a Ge/Si substrate (operation **112**), a prelayer is grown over the substrate using MOCVD operations (operation **114**). Next, a barrier layer is grown over the prelayer using MOCVD operations (operation **116**). Then, a chemical compound semiconductor channel layer is grown over the barrier layer using MOCVD operations (operation **118**). The example channel layer comprises a high-relaxation and smooth InAs thin film or In(Ga)As or Al(Ga)Sb/InAs/Al(Ga)Sb thin film for use in subsequent fabrication of high-speed electronic devices. This example process may allow for the use of a cheaper substrate, such as a Si, Ge, GaAs, or Ge/Si substrate, instead of a GaSb or InP substrate and allow for In(Ga)As or Al(Ga)Sb/InAs/Al(Ga)Sb epilayers to be grown on the cheaper substrates.

[0013] FIG. **3** depicts another example process flow chart for creating a wafer having a chemical compound semiconductor channel layer on a substrate that may be used in a semiconductor fabrication process. In the example process of FIG. **3**, after providing an epi-ready wafer, such as one comprising a GaAs substrate, a Ge substrate, a Si substrate, or a Ge/Si substrate (operation **122**), a graded-temperature arsenic prelayer is grown over the substrate using MOCVD operations (operation **124**). The graded-temperature arsenic prelayer may be grown at a graded temperature ramped from 300 to 550° C. In this example, the prelayer thickness is several nanometers but less than 10 nm.

[0014] Next, a barrier layer is grown over the prelayer using MOCVD operations (operation **126**). The barrier layer in this example consists of a GaAs with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or multiple GaAs-

based layers. The thickness of the barrier layer(s) in this example is about 5-500 nm. Also, the barrier layer(s) is slightly P or N-type (~10^{17} cm^{-3}).

[0015] Then, an InAs or Sb-based channel layer is grown over the barrier layer using MOCVD operations (operation **128**). The example channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures with one or more pairs deposited at a temperature of about 300~600 degree. In this example, the channel thickness is about 20-500nm.

[0016] By using the example processes of FIGS. **1**, **2**, and **3**, periodic 90° misfit dislocations may be generated between the barrier and channel layers to relax the strain. The channel layer of the devices generated using the examples of FIG. **1**, **2**, or **3** may be used in a semiconductor fabrication process for fabricating, for example, a high electron mobility transistor (HEMT), a field-effect transistor (FET), a tunneling field-effect transistor (TFET), a fin field-effect transistor (FinFET), a metal-oxide-semiconductor field-effect transistor (MOSFET), and/or a heterojunction bipolar transistor (HBT).

[0017] FIG. **4** depicts a cross-sectional view of an example wafer **200** that may be used in a semiconductor fabrication process. The example wafer **200** comprises a substrate **202**. In this example, the substrate **202** comprises a GaAs substrate, a Ge substrate, a Si substrate, or a Ge/Si substrate.

[0018] The example wafer **200** further comprises an arsenic (As) prelayer **204** formed over the substrate **202**. The arsenic prelayer **204**, in this example, is a graded-temperature arsenic prelayer that may be grown at a graded temperature ramped from 300 to 550° C. In this example, the prelayer thickness is several nanometers but less than 10 nm.

[0019] A barrier layer **206** is formed above the arsenic prelayer **204**. The barrier layer **206** in this example is grown over the prelayer using MOCVD operations. The barrier layer **206** in this example consists of a GaAs with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or multiple GaAs-based layers. The thickness of the barrier layer(s) in this example is about 5-500 nm. Also, the barrier layer(s) is slightly P or N-type (~10^{17} cm^{-3}).

[0020] An InAs or Sb-based channel layer **208** is grown over the barrier layer **206**. The example channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures with one or more pairs deposited at a temperature of about 300~600° C. In this example, the channel thickness is about 20-500 nm.

[0021] The channel layer can be used for the deposition of high-performance electron devices such as tunneling field-effect transistor (TFET). The wafer **200** may be used in a semiconductor fabrication process for fabricating, for example, a high electron mobility transistor (HEMT), a field-effect transistor (FET), a tunneling field-effect transistor (TFET), a fin field-effect transistor (FinFET), a metal-oxide-semiconductor field-effect transistor (MOSFET), and/or a heterojunction bipolar transistor (HBT).

[0022] The use of the disclosed techniques may allow for a lattice mismatch between In(Ga)As and GaAs epilayers of about 7.2%. The relaxation degree between InAs and GaAs epilayers using techniques described herein may reach >90%.

[0023] The growth techniques disclosed herein may obviate the need for a graded buffer layer, and allow for high-relaxation In(Ga)As epitaxy or Al(Ga)Sb/In(Ga)As/Al(Ga)Sb epilayers to be grown on a GaAs/Ge(Si) heterostructure or various substrates. A cheaper substrate, such as Si, Ge, GaAs, or Ge/Si substrate, may be used with the techniques described herein, and In(Ga)As or Al(Ga)Sb/InAs/Al(Ga)Sb epilayers may be directly grown on cheaper substrates. In some examples, Al(Ga)Sb/In(Ga)As/Al(Ga)Sb heterostructures can be directly grown on a silicon substrate, gallium arsenic substrate, germanium substrate, or Ge/Si substrate by MOCVD operations.

[0024] In one embodiment, disclosed is a method of providing a chemical compound semiconductor channel layer on a substrate for use in a semiconductor fabrication process. The method comprises providing a prelayer over a substrate, providing a barrier layer over the prelayer, and providing a chemical compound semiconductor channel layer over the barrier layer.

[0025] These aspects and other embodiments may include one or more of the following features. The substrate may comprise a gallium arsenide substrate, a silicon substrate, a germanium substrate, or a Ge/Si substrate. Each of the prelayer, barrier layer, and channel layer may be provided using metal organic chemical vapor deposition (MOCVD) operations. The prelayer may comprise a graded-temperature arsenic prelayer grown with graded temperature ramped from 300 to 550° C. The prelayer thickness may be less than 10 nanometers. The barrier layer may comprise GaAs with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or more GaAs-based layers. The barrier layer thickness may be about 5-500 nanometers. The barrier layer may be slightly P or N-type. The channel layer may comprise an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures with one or more pairs deposited at a temperature of about 300 to 600° C. The channel thickness may be about 20-500 nanometers. Periodic 90° misfit dislocations may be generated between the barrier and the channel layers to relax the strain. The channel layer may be used for the deposition of high-performance electron devices such as a tunneling field-effect transistor (TFET).

[0026] In another embodiment, a wafer for use in a semiconductor fabrication process is provided. The wafer comprises a prelayer grown over a substrate, wherein the substrate comprises a gallium arsenide (GaAs) substrate, a silicon (Si) substrate, a germanium (Ge) substrate, or a Ge/Si substrate, and wherein the prelayer is a graded-temperature arsenic prelayer. The wafer further comprises a barrier layer grown over the prelayer, wherein the barrier layer comprises a GaAs layer with low-growth-temperature growth or an $In_xGa_{1-x}As$ with one or more GaAs-based layers. The wafer also comprises a channel layer grown over the barrier layer, wherein the channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures.

[0027] These aspects and other embodiments may include one or more of the following features. Each of the prelayer, barrier layer, and channel layer may have been grown using metal organic chemical vapor deposition (MOCVD) operations. The prelayer may have been grown with graded temperature ramped from 300 to 550° C. The prelayer thickness may be less than 10 nanometers. The barrier layer thickness may be about 5-500 nanometers. The barrier layer may be slightly P or N-type. The channel layer thickness may be about 20-500 nanometers. The wafer may comprise periodic 90° misfit dislocations between the barrier and the channel layers to relax the strain.

[0028] In yet another embodiment, a method of producing a wafer for use in a semiconductor process is disclosed. The method comprises growing using metal organic chemical

vapor deposition (MOCVD) operations a graded-temperature arsenic prelayer over a substrate comprising a gallium arsenide (GaAs) substrate, a silicon (Si) substrate, a germanium (Ge) substrate, or a Ge/Si substrate. The method further comprises growing using MOCVD operations a barrier layer over the prelayer, wherein the barrier layer comprises a GaAs layer with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or multiple GaAs-based layers. Additionally, the method comprises growing using MOCVD operations a channel layer over the barrier layer, wherein the channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures.

[0029] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

1. A method of providing a chemical compound semiconductor channel layer on a substrate for use in a semiconductor fabrication process, the method comprising:
- providing a prelayer over a substrate;
- providing a barrier layer over the prelayer; and
- providing a chemical compound semiconductor channel layer over the barrier layer.

2. The method of claim **1**, wherein providing the prelayer over the substrate comprises providing the prelayer over a substrate selected from the group consisting of a gallium arsenide substrate, a silicon substrate, a germanium substrate, and a Ge/Si substrate.

3. The method of claim **1**, wherein each of the prelayer, barrier layer, and channel layer is provided using metal organic chemical vapor deposition (MOCVD) operations.

4. The method of claim **1**, wherein providing the prelayer over the substrate comprises growing a graded-temperature arsenic prelayer with graded temperature ramped from 300 to 550° C.

5. The method of claim **1**, wherein providing the prelayer over the substrate comprises growing the prelayer with a thickness of less than 10 nanometers.

6. The method of claim **1**, wherein providing the barrier layer comprises selectively forming a GaAs barrier layer with low-growth-temperature growth and forming an $In_xGa_{1-x}As$ epitaxy barrier layer having at least one GaAs-based layer.

7. The method of claim **1**, wherein providing the barrier layer comprises forming the barrier layer with a thickness of about 5 nanometers to about 500 nanometers.

8. The method of claim **1**, wherein providing the barrier layer comprises proving a lightly doped barrier layer.

9. The method of claim **1**, wherein providing the compound semiconductor channel layer comprises selectively forming an InAs epitaxy layer with low-growth-temperature growth and depositing at least one pair of Al(In)Sb/InAs/Al(In)Sb heterostructures at a temperature of about 300 to 600° C.

10. The method of claim **1**, wherein providing the compound semiconductor channel layer comprises forming the channel layer with a thickness of about 20 to about 500 nanometers.

11. The method of claim **1**, wherein providing the compound semiconductor channel layer over the barrier layer generates periodic 90° misfit dislocations between the barrier and the channel layers, wherein the misfit dislocations relaxes a strain there-between.

12-19. (canceled)

20. A method of producing a wafer for use in a semiconductor process, the method comprising:
- growing using metal organic chemical vapor deposition (MOCVD) operations a graded-temperature arsenic prelayer over a substrate comprising a gallium arsenide (GaAs) substrate, a silicon (Si) substrate, a germanium (Ge) substrate, or a Ge/Si substrate;
- growing using MOCVD operations a barrier layer over the prelayer, wherein the barrier layer comprises a GaAs layer with low-growth-temperature growth or an $In_xGa_{1-x}As$ epitaxy with one or multiple GaAs-based layers; and
- growing using MOCVD operations a channel layer over the barrier layer, wherein the channel layer comprises an InAs epitaxy with low-growth-temperature growth or Al(In)Sb/InAs/Al(In)Sb heterostructures.

21. The method of claim **8**, wherein providing the barrier layer comprises selectively providing a lightly doped P-type and N-type barrier layer.

22. The method of claim **8**, wherein providing the barrier layer comprises providing the barrier layer with a dopant concentration of about 10^{17} cm^{-3}.

23. A method of providing a high mobility compound semiconductor channel layer on a substrate, the method comprising:
- providing, using metal organic chemical vapor deposition (MOCVD) processes, a prelayer over an epi-ready wafer;
- providing, using MOCVD processes, a graded barrier layer over the prelayer; and
- providing, using MOCVD processes, a thin film channel layer over the barrier layer.

24. The method of claim **23**, wherein providing the graded prelayer over the substrate comprises growing a graded-temperature arsenic prelayer with graded temperature ramped from 300 to 550° C.

25. The method of claim **24**, wherein providing the graded prelayer over the epi-ready wafer comprises growing the graded-temperature arsenic prelayer over an epi-ready wafer selected from the group consisting of a gallium arsenide substrate, a silicon substrate, a germanium substrate, and a Ge/Si substrate.

26. The method of claim **23**, wherein providing the barrier layer comprises forming a barrier layer selected from the group consisting of a GaAs barrier layer with low-growth-temperature growth and an $In_xGa_{1-x}As$ epitaxy barrier layer having at least one GaAs-based layer.

27. The method of claim **23**, wherein providing the thin film channel layer comprises selectively forming at least one of an InAs epitaxy layer with low-growth-temperature growth and at least one pair of Al(In)Sb/InAs/Al(In)Sb heterostructures at a temperature of about 300 to 600° C. to form the thin film channel layer with a thickness of about 20 to about 500 nanometers.

28. The method of claim **27**, wherein providing the thin film channel layer over the barrier layer generates periodic

90° misfit dislocations between the barrier and the channel layers, wherein the misfit dislocations relaxes a strain there-between.

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