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(54) **SEMICONDUCTOR DEVICE AND FORMATION THEREOF**

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H01L 21/02	(2006.01)
H01L 29/66	(2006.01)
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(52) **U.S. Cl.**

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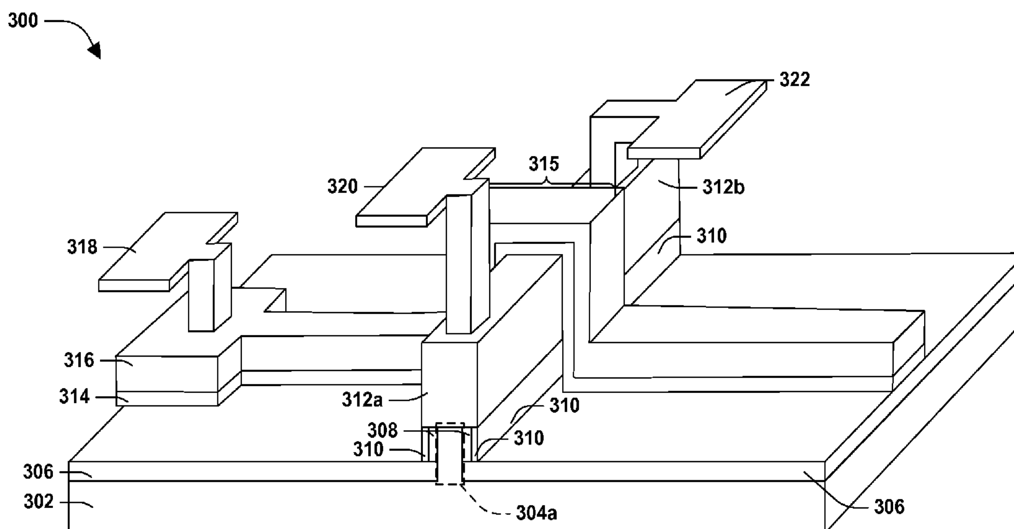
(57) **ABSTRACT**

A semiconductor device and methods of formation are provided. The semiconductor device includes a first metal alloy over a first active region of a fin and a second metal alloy over a second active region of the fin. A conductive layer is over a channel region of the fin. A semiconductive layer is over the conductive layer. The conductive layer over the channel region suppresses current leakage and the semiconductive layer over the conductive layer reduces electro flux from a source to a drain, as compared to a channel region that does not have such a conductive layer or a semiconductive layer over a conductive layer. The semiconductor device having the first metal alloy as at least one of the source or drain requires a lower activation temperature than a semiconductor device that does not have a metal alloy as a source or a drain.



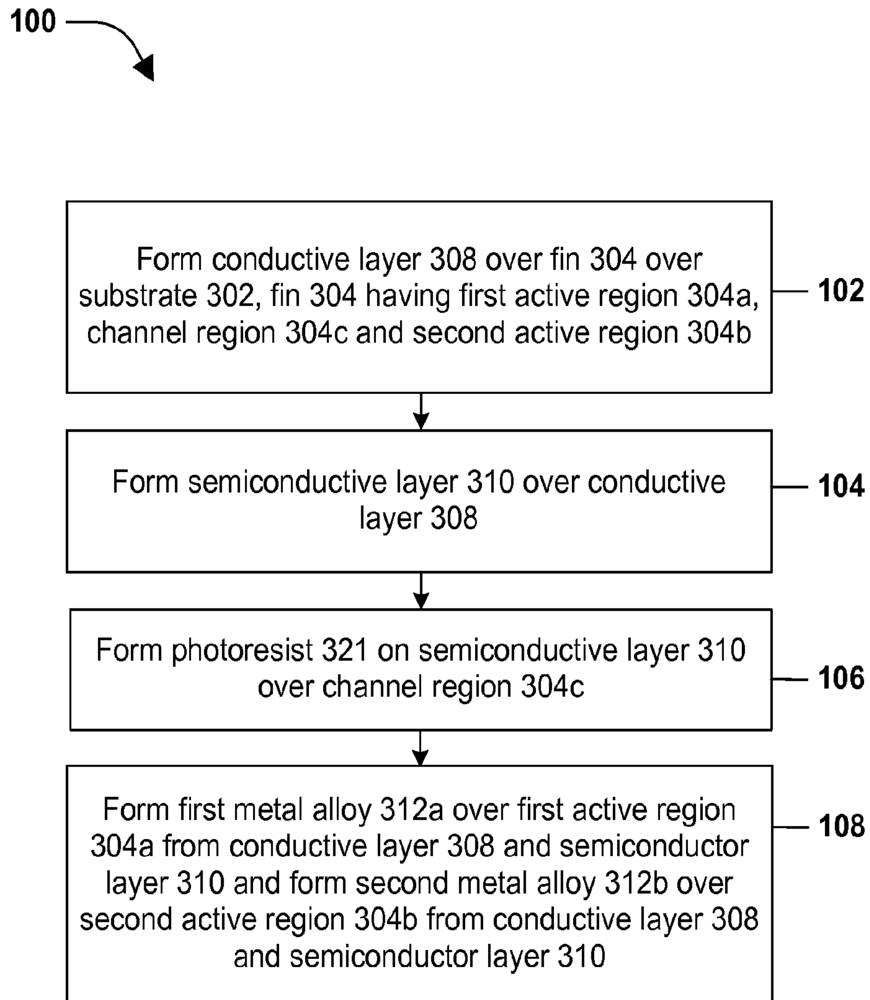


FIG. 1

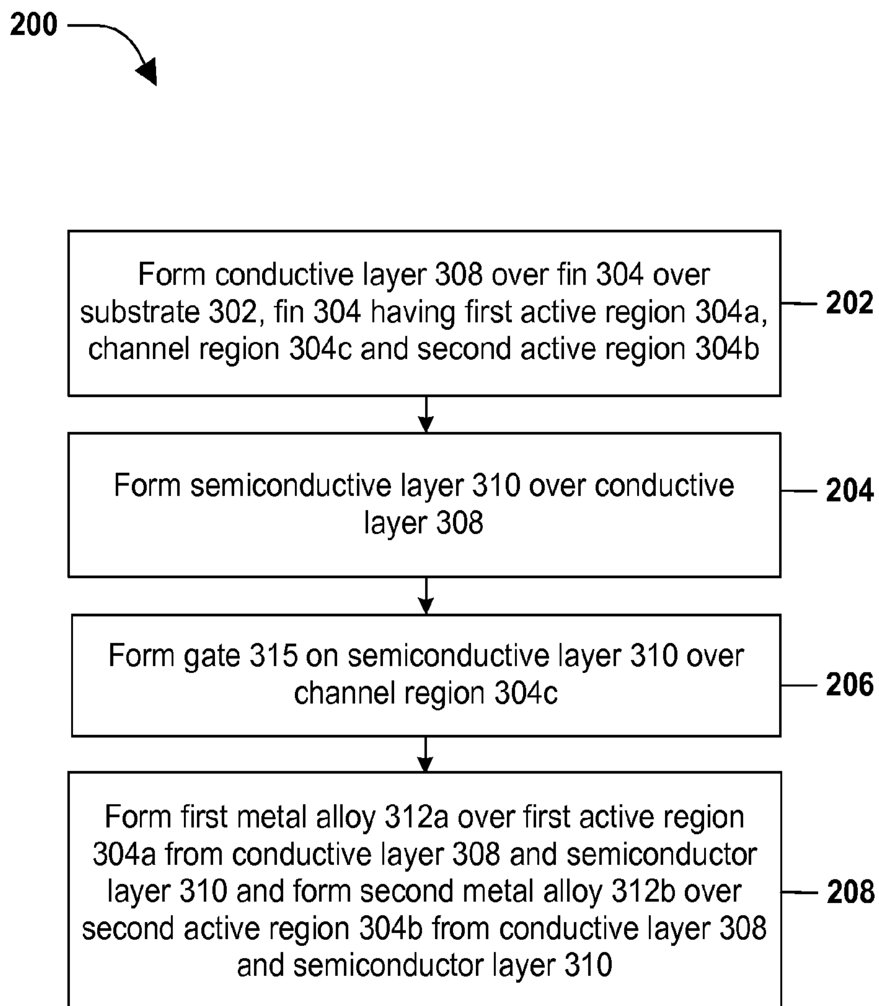


FIG. 2

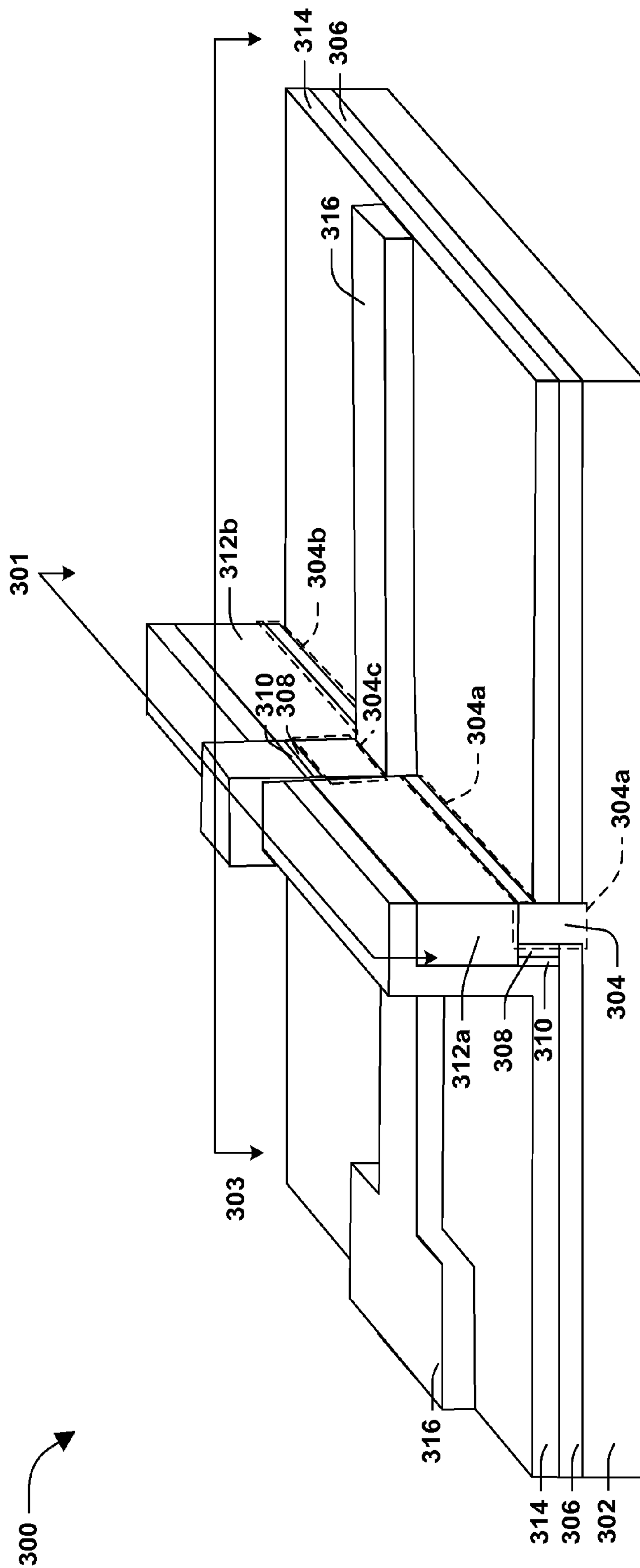


FIG. 3

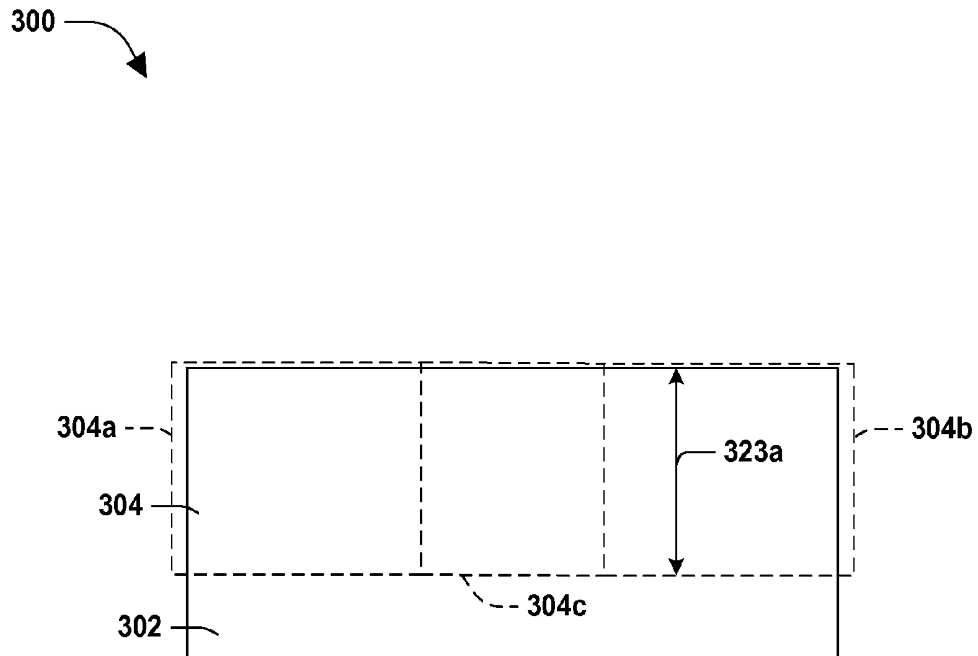


FIG. 4

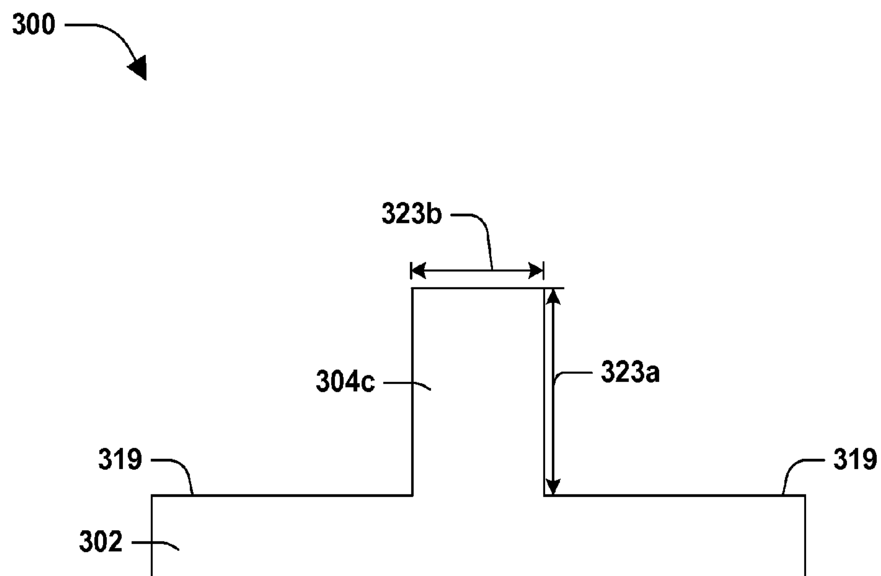


FIG. 5

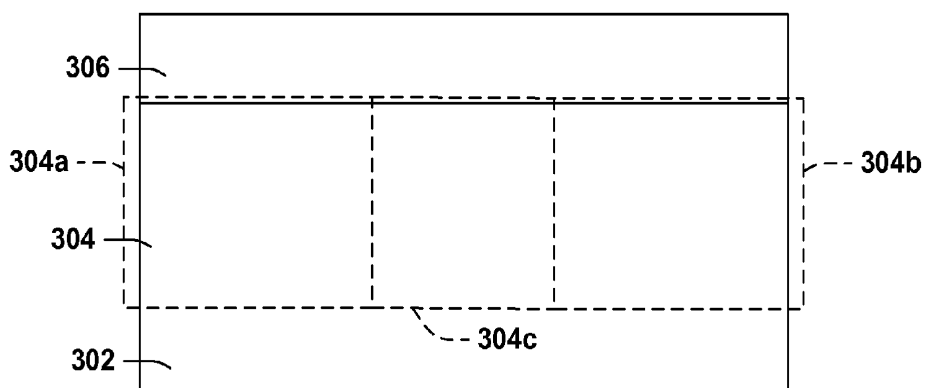


FIG. 6

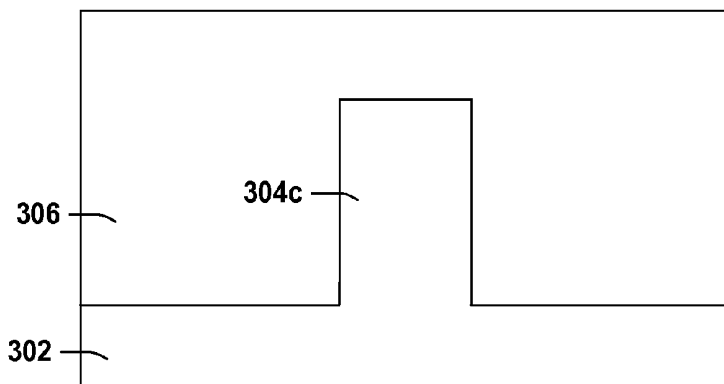


FIG. 7

300

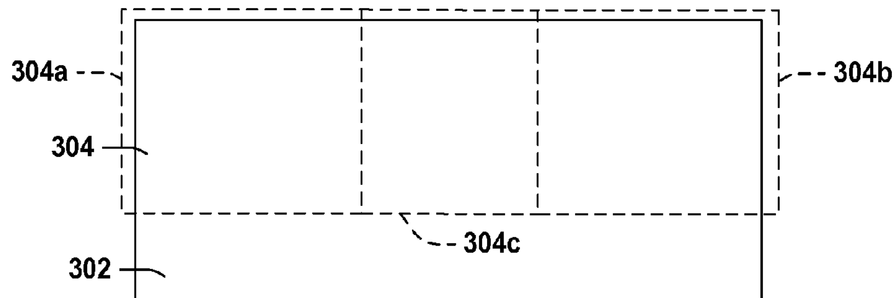


FIG. 8

300

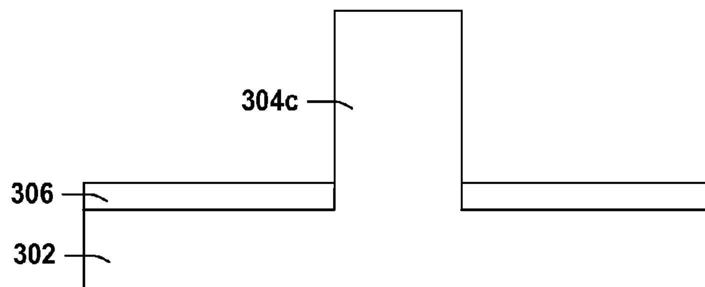


FIG. 9

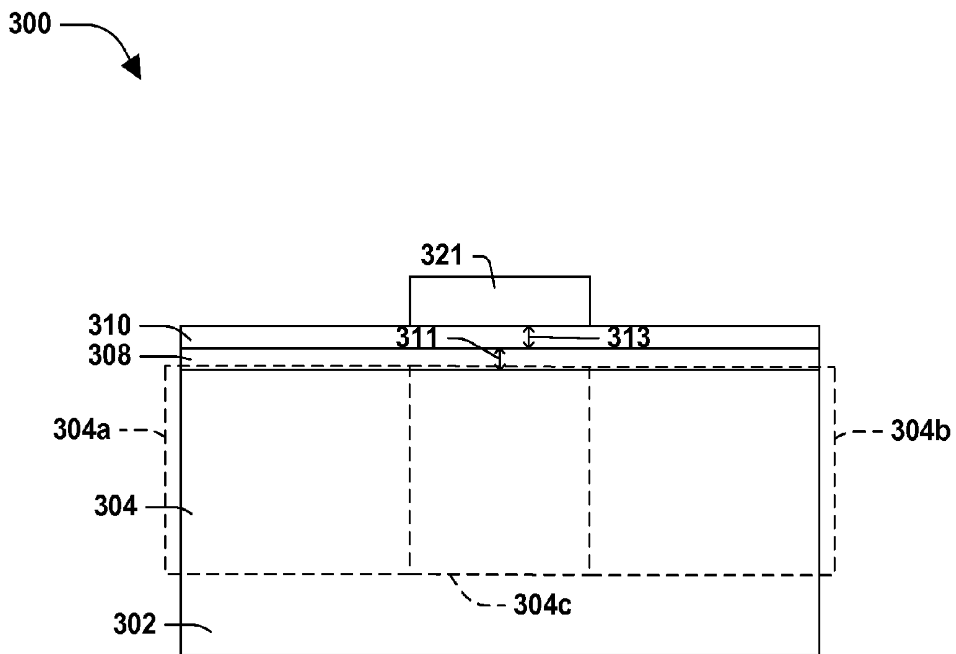


FIG. 10

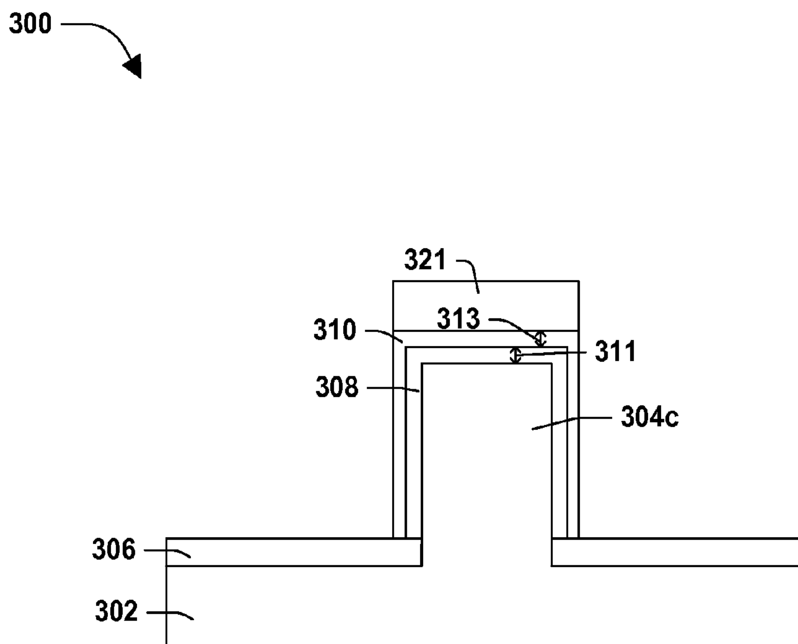


FIG. 11

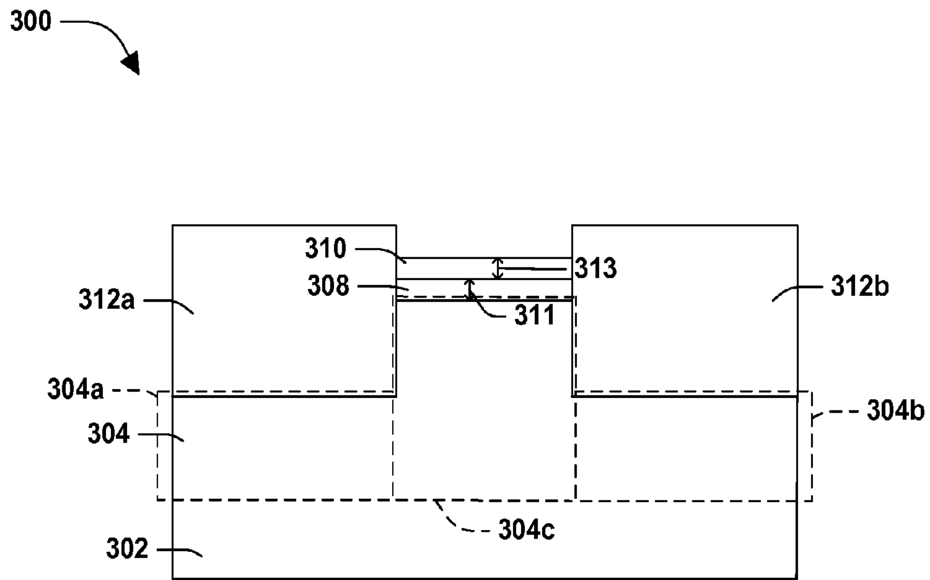


FIG. 12

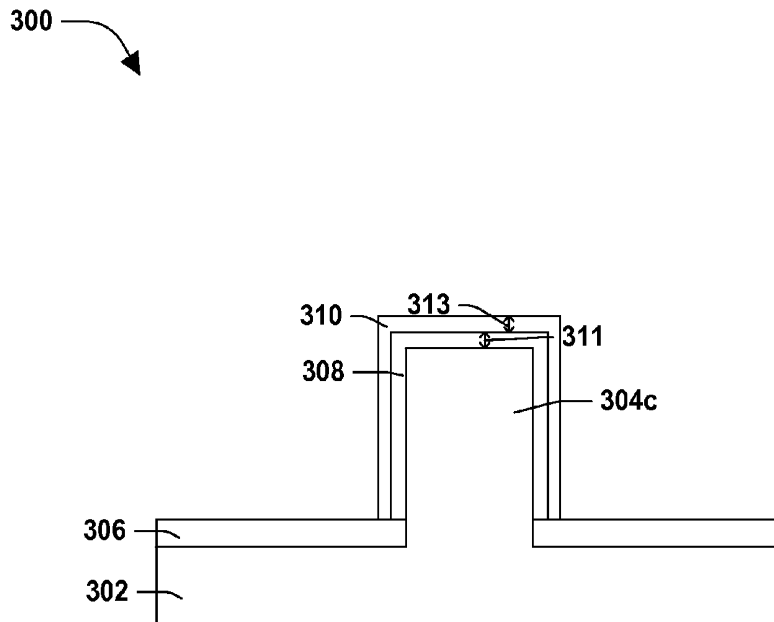


FIG. 13

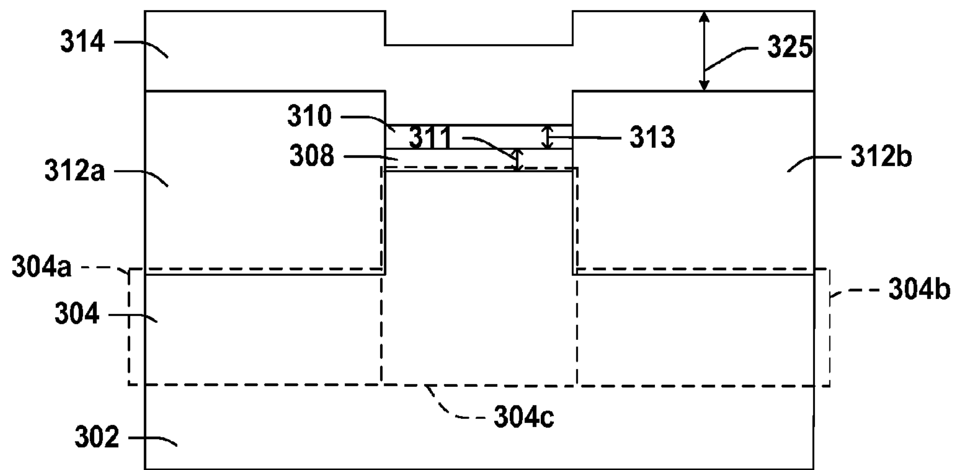


FIG. 14

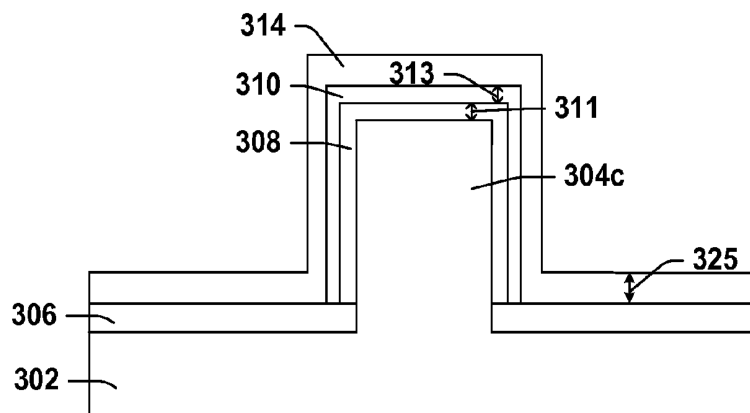


FIG. 15

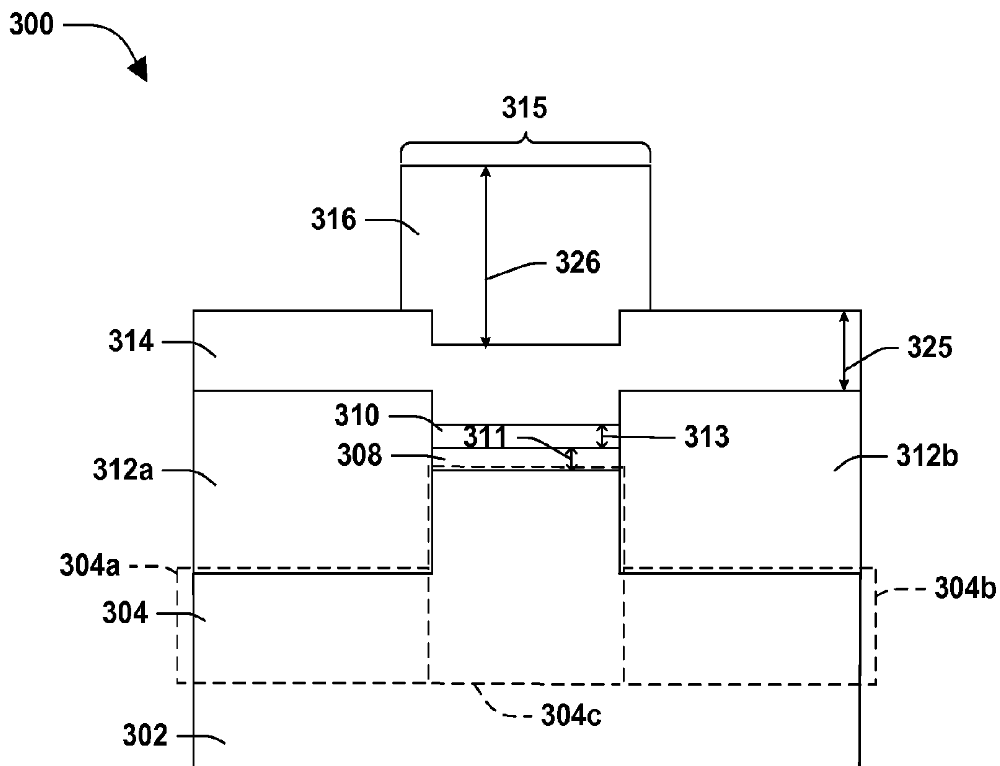


FIG. 16

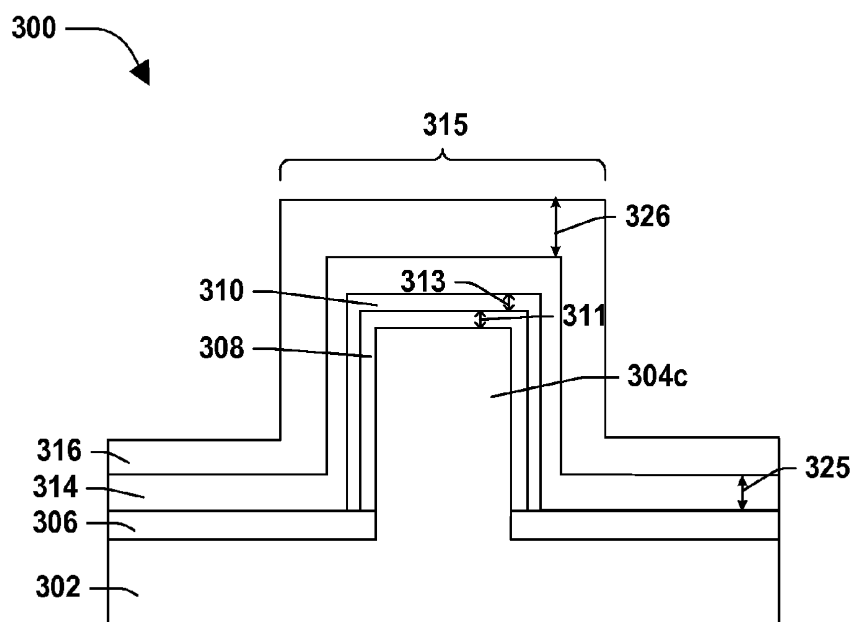


FIG. 17

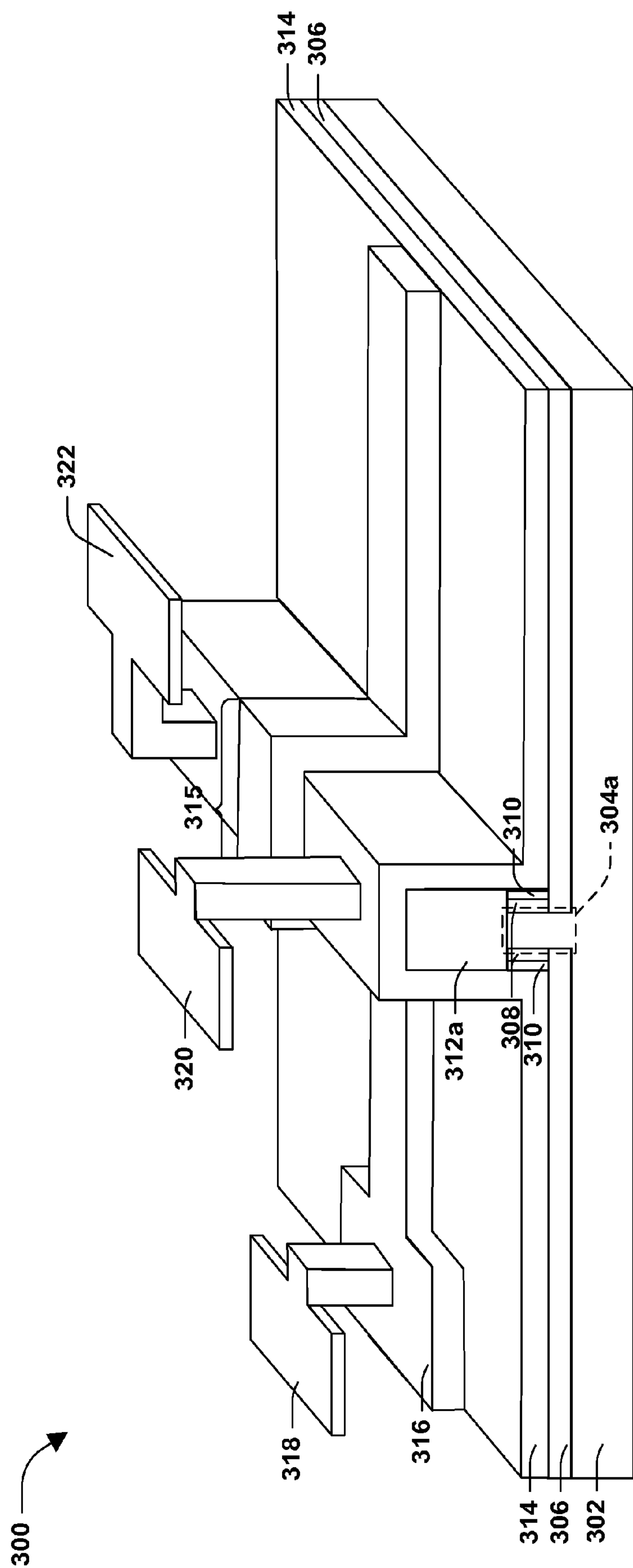


FIG. 18

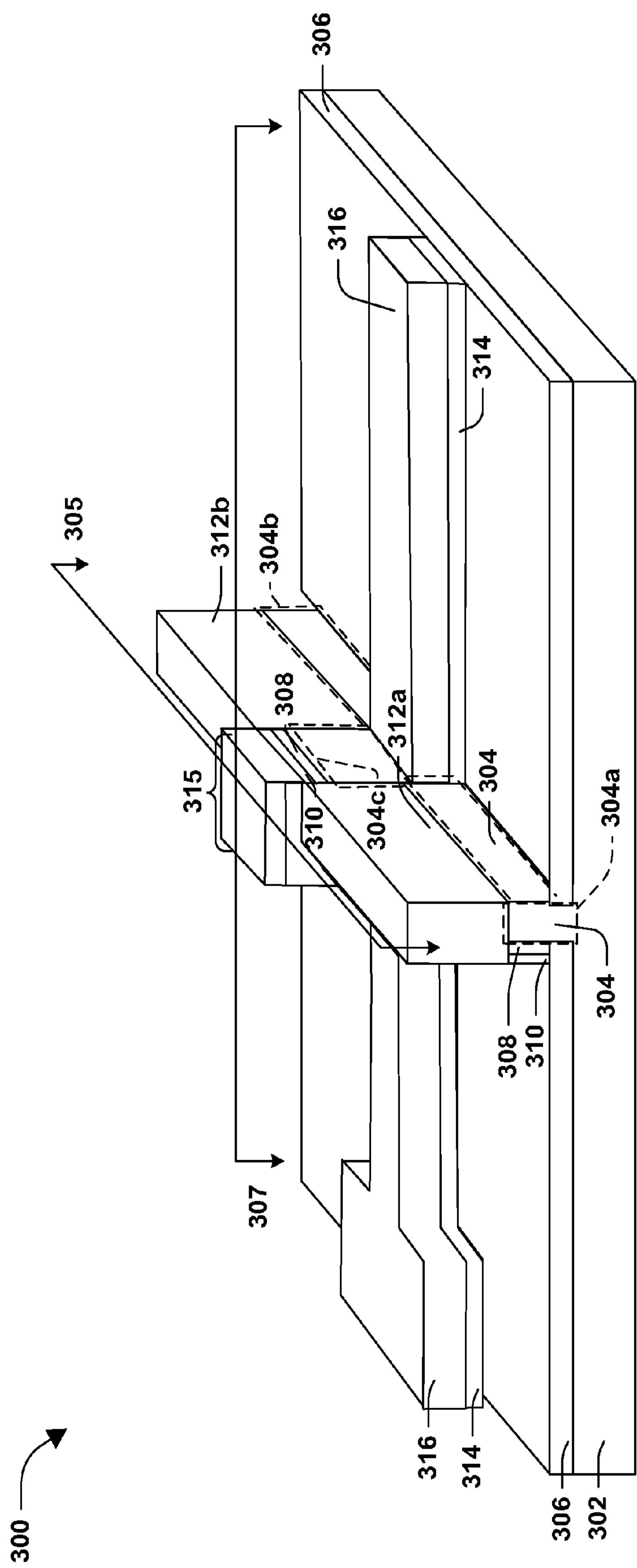


FIG. 19

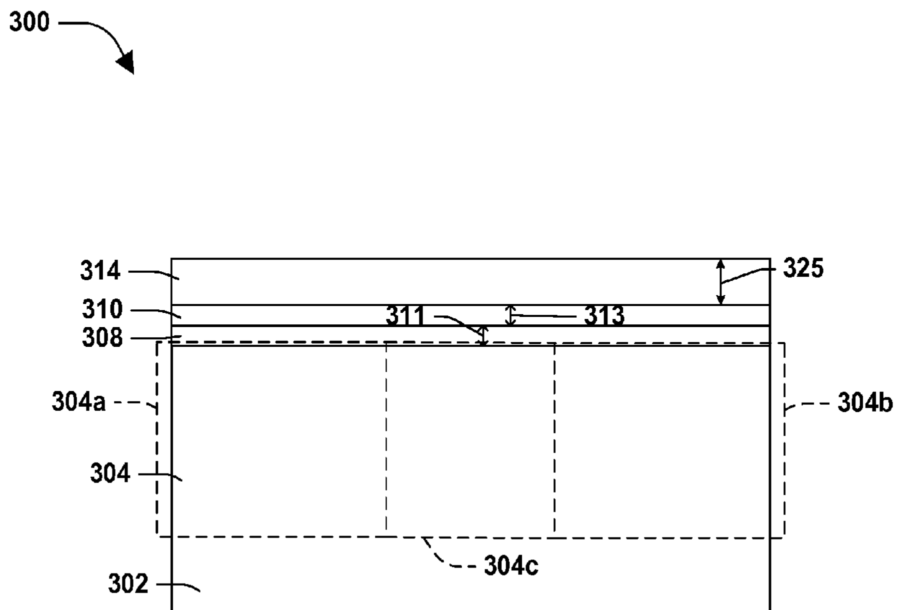


FIG. 20

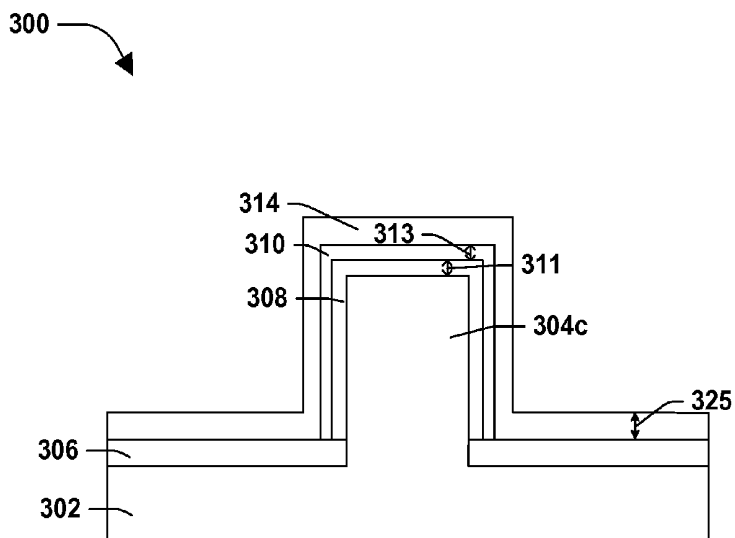


FIG. 21

FIG. 22

FIG. 23

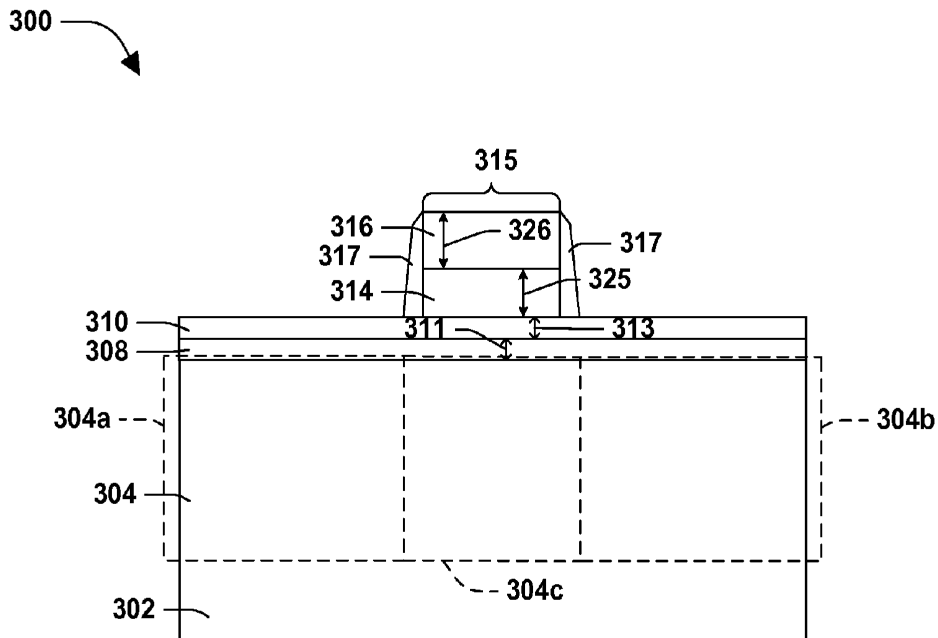


FIG. 24

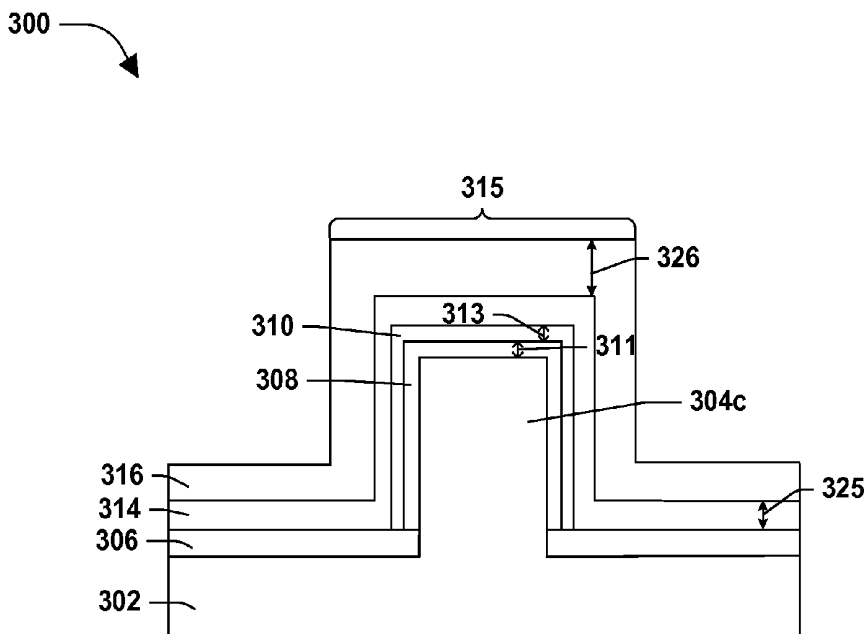


FIG. 25

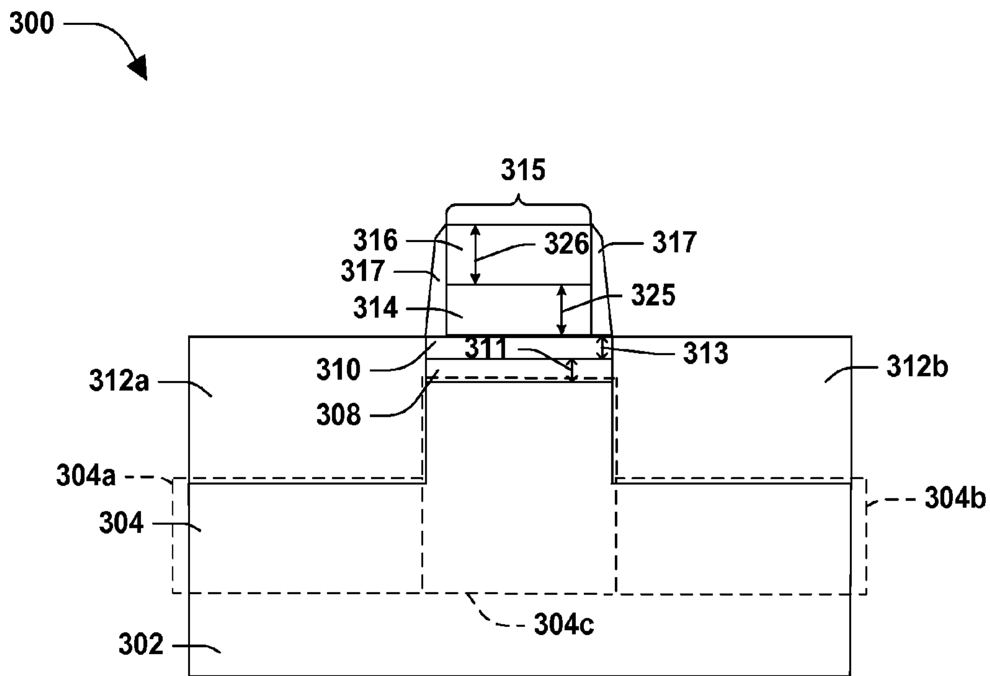


FIG. 26

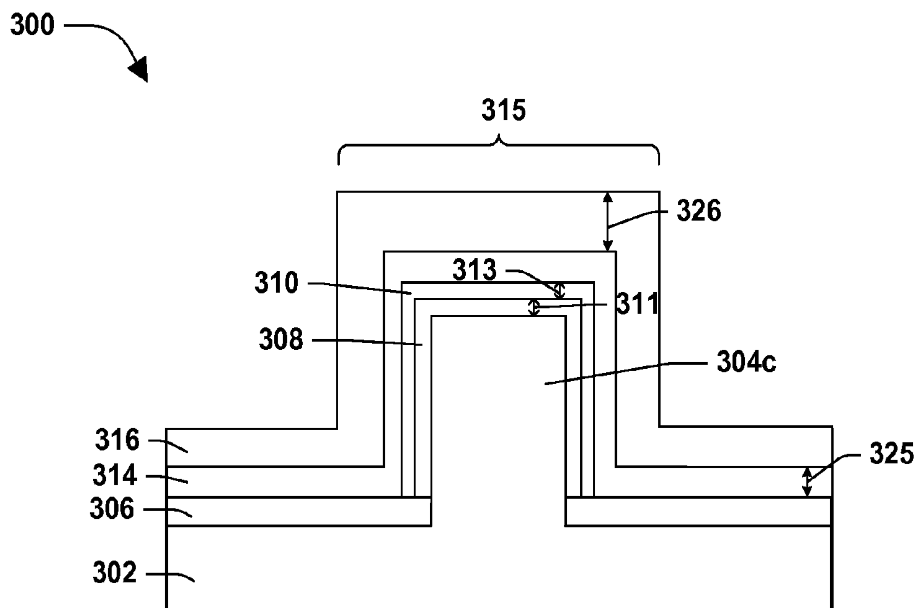


FIG. 27

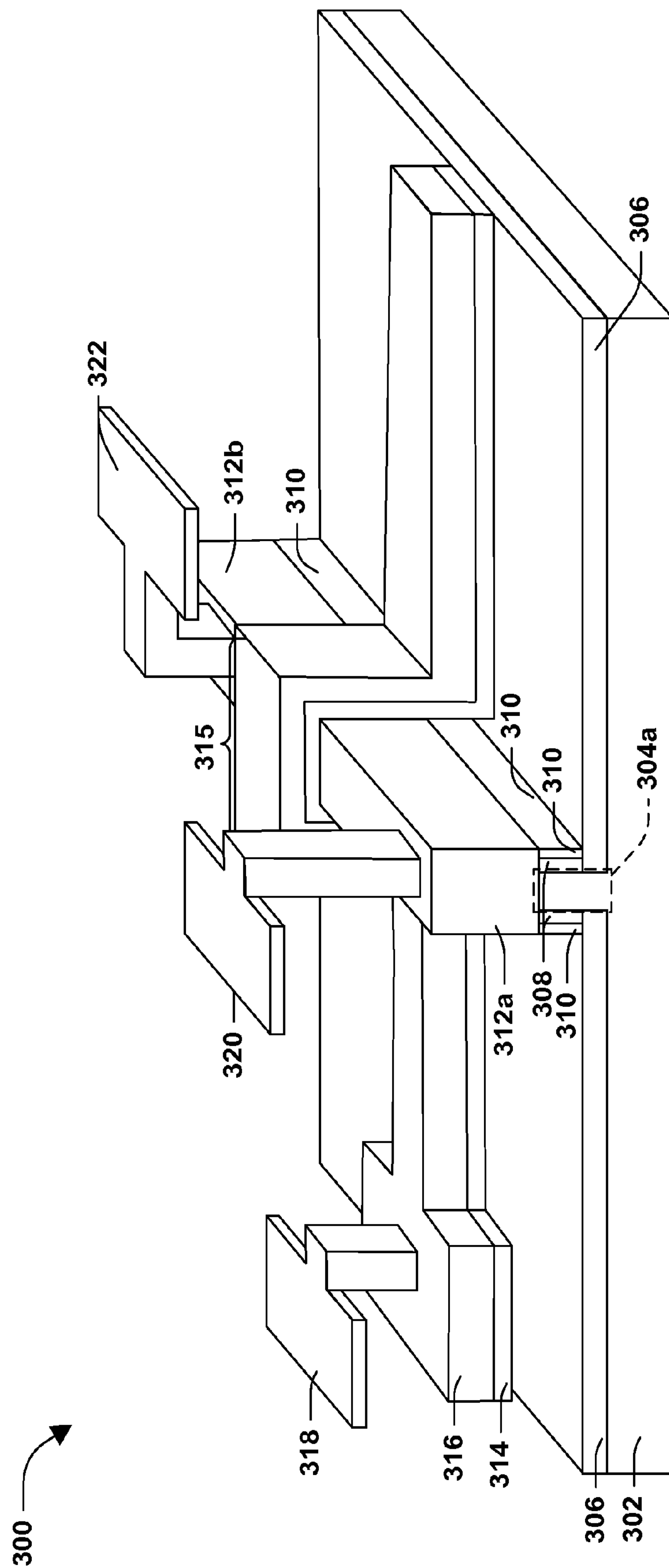


FIG. 28

SEMICONDUCTOR DEVICE AND FORMATION THEREOF

BACKGROUND

[0001] In a semiconductor device, such as a transistor, current flows through a channel region between a source region and a drain region upon application of a sufficient voltage or bias to a gate of the device. When current flows through the channel region, the transistor is generally regarded as being in an 'on' state, and when current is not flowing through the channel region, the transistor is generally regarded as being in an 'off' state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0003] FIG. **1** is a flow diagram illustrating a method of forming a semiconductor device, in accordance with some embodiments.

[0004] FIG. **2** is a flow diagram illustrating a method of forming a semiconductor device, in accordance with some embodiments.

[0005] FIG. **3** is an illustration of a semiconductor device, in accordance with some embodiments.

[0006] FIG. **4** is an illustration of a semiconductor device, in accordance with some embodiments.

[0007] FIG. **5** is an illustration of a semiconductor device, in accordance with some embodiments.

[0008] FIG. **6** is an illustration of a semiconductor device, in accordance with some embodiments.

[0009] FIG. **7** is an illustration of a semiconductor device, in accordance with some embodiments.

[0010] FIG. **8** is an illustration of a semiconductor device, in accordance with some embodiments.

[0011] FIG. **9** is an illustration of a semiconductor device, in accordance with some embodiments.

[0012] FIG. **10** is an illustration of a semiconductor device, in accordance with some embodiments.

[0013] FIG. **11** is an illustration of a semiconductor device, in accordance with some embodiments.

[0014] FIG. **12** is an illustration of a semiconductor device, in accordance with some embodiments.

[0015] FIG. **13** is an illustration of a semiconductor device, in accordance with some embodiments.

[0016] FIG. **14** is an illustration of a semiconductor device, in accordance with some embodiments.

[0017] FIG. **15** is an illustration of a semiconductor device, in accordance with some embodiments.

[0018] FIG. **16** is an illustration of a semiconductor device, in accordance with some embodiments.

[0019] FIG. **17** is an illustration of a semiconductor device, in accordance with some embodiments.

[0020] FIG. **18** is an illustration of a semiconductor device, in accordance with some embodiments.

[0021] FIG. **19** is an illustration of a semiconductor device, in accordance with some embodiments.

[0022] FIG. **20** is an illustration of a semiconductor device, in accordance with some embodiments.

[0023] FIG. **21** is an illustration of a semiconductor device, in accordance with some embodiments.

[0024] FIG. **22** is an illustration of a semiconductor device, in accordance with some embodiments.

[0025] FIG. **23** is an illustration of a semiconductor device, in accordance with some embodiments.

[0026] FIG. **24** is an illustration of a semiconductor device, in accordance with some embodiments.

[0027] FIG. **25** is an illustration of a semiconductor device, in accordance with some embodiments.

[0028] FIG. **26** is an illustration of a semiconductor device, in accordance with some embodiments.

[0029] FIG. **27** is an illustration of a semiconductor device, in accordance with some embodiments.

[0030] FIG. **28** is an illustration of a semiconductor device, in accordance with some embodiments.

DETAILED DESCRIPTION

[0031] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0032] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0033] One or more techniques for forming a semiconductor device and resulting structures formed thereby are provided herein.

[0034] A first method **100** of forming a semiconductor device **300** is illustrated in FIG. **1**, and one or more semiconductor devices formed by such methodology are illustrated in FIGS. **3-18**. Turning to FIG. **3**, a 3 dimensional (3D) view of the semiconductor device **300** is illustrated, where a portion of an insulating layer **314**, a semiconductive layer **310** and a conductive layer **308** illustrated in FIGS. **14-18** are not shown in FIG. **3** so that features underlying the insulating layer **314**, the semiconductive layer **310** and the conductive layer **308** are visible in FIG. **3**. In some embodiments, the semiconductor device **300** comprises a fin **304** over a substrate **302**. In some embodiments, the fin **304** comprises a first active region **304***a*, a channel region **304***c* and a second active region **304***b*. In some embodiments, a first dielectric layer **306** is over the substrate **302**, and the insulating layer **314** is over the first

dielectric layer **306** and the fin **304**. In some embodiments, the conductive layer **308** is on sidewalls of the fin **304** in the first active region **304***a* under a first metal alloy **312***a* and in the second active region **304***b* under a second metal alloy **312***b*. In some embodiments, the conductive layer **308** comprises germanium. In some embodiments, the conductive layer **308** is over and on the sidewalls of the fin **304** in the channel region **304***c*. In some embodiments, the semiconductive layer **310** is over the conductive layer **308** on the sidewalls of the fin **304** in the first active region **304***a* under the first metal alloy **312***a* and in the second active region **304***b* under the second metal alloy **312***b*. In some embodiments, the semiconductive layer **310** is over the conductive layer **308** in the channel region **304***c*. In some embodiments, the semiconductive layer **310** comprises silicon. In some embodiments, the conductive layer **308** has a conductive layer thickness **311**, depicted inter alia in FIG. **10**, between about 0.5 nm to about 5 nm. In some embodiments, the semiconductive layer **310** is over the conductive layer **308** over the fin **304** in the channel region **304***c*. In some embodiments, the semiconductive layer **310** has a semiconductive layer thickness **313**, depicted inter alia in FIG. **10**, between about 0.1 nm to about 3 nm. In some embodiments, at least one of the first metal alloy **312***a* or the second metal alloy **312***b* comprises at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon. In some embodiments, at least one of the first metal alloy **312***a* or the second metal alloy **312***b* comprises at least one of a source or a drain. In some embodiments, the conductive layer **308** having the conductive layer thickness **311** over the channel region **304***c* suppresses current leakage as compared to a conductive layer having a thickness different than the conductive layer thickness **311**. In some embodiments, the semiconductive layer **310** over the conductive layer **308** in the channel region **304***c* reduces electro flux from the source to the drain, as compared to a channel region that does not have a semiconductive layer over a conductive layer. In some embodiments, the semiconductor device **300** having the first metal alloy **312***a* as at least one of the source or drain and the second metal alloy **312***b* as at least one of the source or drain requires a lower activation temperature than a semiconductor device that does not have a metal alloy as at least one of a source or a drain.

[0035] In FIG. **3** two lines **301** and **303** are drawn to illustrate cross-sections that are depicted in other Figs. A first line **301** cuts through a metal layer **316**, the insulating layer **314**, the semiconductive layer **310**, the conductive layer **308**, the first metal alloy **312***a*, the second metal alloy **312***b*, the fin **304** and the substrate **302**, and. FIGS. **4**, **6**, **8**, **10**, **12**, **14** and **16** are cross sectional views of the semiconductor device **300** taken along the first line **301** at various stages of fabrication. A second line **303** cuts through the metal layer **316**, the insulating layer **314**, the semiconductive layer **310**, the conductive layer **308**, the first dielectric layer **306**, the fin **304** and the substrate **302**, FIGS. **5**, **7**, **9**, **11 13**, **15**, and **17** are cross sectional views of the semiconductor device **300** taken along the second line **303** at various stages of fabrication.

[0036] At **102** of the first method **100**, as illustrated in FIGS. **10** and **11**, the conductive layer **308** is formed over the fin **304** over the substrate **302**, according to some embodiments. Turning to FIGS. **4** and **5**, prior to FIGS. **10** and **11**, the fin **304** is formed from the substrate **302**, such as by etching, according to some embodiments. In some embodiments, the substrate **302** comprises at least one of silicon or germanium. According to some embodiments, the substrate **302** comprises at least one of an epitaxial layer, a silicon-on-insulator (SOI) structure, a wafer, or a die formed from a wafer. In some embodiments, the fin **304** has the first active region **304***a*, the channel region **304***c* and the second active region **304***b*. In some embodiments, the fin **304** has a fin height **323***a* between about 20 nm to about 70 nm and a fin width **323***b* between about 10 nm to about 30 nm. Turning to FIGS. **6** and **7**, the first dielectric layer **306** is formed over the substrate **302** and the fin **304**, according to some embodiments. In some embodiments, the first dielectric layer **306** comprises at least one of silicon or oxide. In some embodiments, the first dielectric layer **306** is formed by deposition. Turning to FIGS. **8** and **9**, the first dielectric layer **306** is etched such that the first dielectric layer **306** is removed from a top surface of the fin **304** and a portion of the sidewalls of the fin **304** and such that the first dielectric layer **306** remains over a top surface **319** of the substrate **302**, as illustrated in FIG. **5**. Turning to FIGS. **10** and **11**, the conductive layer **308** is formed over the fin **304**, according to some embodiments. In some embodiments, the conductive layer **308** comprises germanium. In some embodiments, the conductive layer **308** is grown, such as by epitaxial growth. In some embodiments, the conductive layer **308** is grown at a conductive temperature between about 400° C. to about 500° C. In some embodiments, the conductive layer **308** is grown at a conductive pressure between about 2 mTorr to about 15 mTorr. In some embodiments, the conductive layer **308** is grown in the presence of a conductive layer gas comprising GeH_4 introduced at a conductive layer flow rate between about 5 sccm to about 15 sccm. In some embodiments, the conductive layer **308** is formed at a conductive layer deposition rate between about 1 nm/min to about 4 nm/min. In some embodiments, the conductive layer **308** has the conductive layer thickness **311** between about 0.5 nm to about 5 nm.

[0037] At **104** of the first method of **100**, as illustrated in FIGS. **10** and **11**, the semiconductive layer **310** is formed over the conductive layer **308**, according to some embodiments. In some embodiments, the semiconductive layer **310** comprises silicon. In some embodiments, the semiconductive layer **310** is grown, such as by epitaxial growth. In some embodiments, the semiconductive layer **310** is grown at a semiconductive temperature between about 600° C. to about 700° C. In some embodiments, the semiconductive layer **310** is grown at a semiconductive pressure between about 0.2 mTorr to about 2 mTorr. In some embodiments, the semiconductive layer **310** is grown in the presence of a semiconductive layer gas comprising SiH_4 introduced at a semiconductive layer flow rate between about 0.2 sccm to about 2 sccm. In some embodiments, the semiconductive layer **310** is formed at a semiconductive layer deposition rate between about 0.5 nm/min to about 2 nm/min. In some embodiments, the semiconductive layer **310** has the semiconductive layer thickness **313** between about 0.1 nm to about 3 nm.

[0038] At **106** of the first method of **100**, as illustrated in FIGS. **10** and **11**, a photoresist **321** is formed on the semiconductive layer **310** over the channel region **304***c*, according to some embodiments.

[0039] At **108** of the first method of **100**, as illustrated in FIGS. **12** and **13**, the first metal alloy **312***a* is formed over the first active region **304***a* from the conductive layer **308** and the semiconductor layer **310** and the second metal alloy **312***b* is formed over the second active region **304***b* from the conductive layer **308** and the semiconductor layer **310**, according to some embodiments. In some embodiments, at least one of the

first metal alloy **312***a* or the second metal alloy **312***b* are formed by sputter deposition of at least one of platinum, gold, tantalum, gadolinium or titanium. In some embodiments, the photoresist **321** is removed after the formation of at least one of the first metal alloy **312***a* or the second metal alloy **312***b*. In some embodiments, at least one of the first metal alloy **312***a* or the second metal alloy **312***b* is formed by annealing at a temperature between about 250° C. to about 750° C. for a duration between about 5 s to about 70 s. In some embodiments, such as when at least one of the first metal alloy **312***a* or the second metal alloy **312***b* comprises at least one of nickel, platinum or gold, the semiconductor device **300** is annealed, such as by a rapid thermal anneal at a first anneal temperature between about 350° C. to about 650° C. for a first anneal duration between about 5 s to about 70 s. In some embodiments, such as when at least one of the first metal alloy **312***a* or the second metal alloy **312***b* comprises at least one of titanium, gadolinium or tantalum, the semiconductor device **300** is annealed, such as by a rapid thermal anneal at a second anneal temperature between about 450° C. to about 750° C. for a second anneal duration between about 5 s to about 70 s. In some embodiments, at least one of the first metal alloy **312***a* or the second metal alloy **312***b* comprises at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon. In some embodiments, after the formation of at least one of the first metal alloy **312***a* or the second metal alloy **312***b* the conductive layer **308** and the semiconductive layer **310** remain on sidewalls of the first active region **304***a* and on sidewalls of the second active region **304***b* of the fin **304**. Turning to FIGS. **14** and **15**, the insulating layer **314** is formed over the first dielectric layer **306**, the semiconductive layer **310**, the first metal alloy **312***a* and the second metal alloy **312***b*, according to some embodiments. In some embodiments, the insulating layer **314** comprises at least one of hafnium, zirconium or oxide. In some embodiments, the insulating layer **314** has an insulating thickness **325** between about 0.5 nm to about 1 nm. In some embodiments, the insulating layer **314** is formed by deposition. In some embodiments, the insulating layer **314** interacts with the semiconductive layer **310** over the channel region **304***c* to form a layer of hafnium silicon oxide (not shown). Turning to FIGS. **16** and **17**, the metal layer **316** is formed over the insulating layer **314** over the channel region **304***c*, according to some embodiments. In some embodiments, the metal layer **316** over the insulating layer **314** over the channel region **304***c* comprises a gate **315**. In some embodiments, the metal layer **316** comprises at least one of tantalum or nitride. In some embodiments, the metal layer **316** has a metal layer thickness **326** between about 50 nm to about 100 nm. In some embodiments, the metal layer **316** is formed by deposition. In some embodiments, such as illustrated in FIG. **18**, a gate contact **318** is formed over the metal layer **316** over the substrate **302**. In some embodiments, a first contact **320** is formed over the first active region **304***a*, such that the first contact **320** is in contact with the first metal alloy **312***a*. In some embodiments, a second contact **322** is formed over the second active region **304***b*, such that the second contact **322** is in contact with the second metal alloy **312***b*. In some embodiments, at least one of the gate contact **318**, the first contact **320** or the second contact **322** comprises a conductive material such as metal.

[0040] A second method **200** of forming the semiconductor device **300** is illustrated in FIG. **2**, and one or more semiconductor devices formed by such methodology are illustrated in FIGS. **19-28**. Turning to FIG. **19**, a 3D view of the semiconductor device **300** is illustrated where a portion of the insulating layer **314**, the semiconductive layer **310** and the conductive layer **308** illustrated in FIGS. **20-28** are not shown in FIG. **19** so that features underlying the insulating layer **314**, the semiconductive layer **310** and the conductive layer **308** are visible in FIG. **19**. In FIG. **19** two lines **305** and **307** are drawn to illustrate cross-sections that are depicted in other Figs. A third line **305** cuts through the metal layer **316**, the insulating layer **314**, the first metal alloy **312***a*, the second metal alloy **312***b*, the semiconductive layer **310**, the conductive layer **308**, the fin **304** and the substrate **302**. FIGS. **20**, **22**, **24** and **26** are a cross sectional view of the semiconductor device **300** taken along the third line **305** at various stages of fabrication. A fourth line **307** cuts through the metal layer **316**, the insulating layer **314**, the semiconductive layer **310**, the conductive layer **308**, the first dielectric layer **306**, the fin **304** and the substrate **302**, and FIGS. **21**, **23**, **25**, and **27** are cross sectional views of the semiconductor device **300** taken along the third line **307** at various stages of fabrication.

[0041] At **202** of the second method of **200**, as illustrated in FIGS. **20** and **21**, the conductive layer **308** is formed over the fin **304** over the substrate **302**, according to some embodiments. In some embodiments, the fin **304** is formed from the substrate **302** in the same manner as described above with regards to the fin **304** as illustrated in FIGS. **4** and **5**, according to some embodiments. In some embodiments, the first dielectric layer **306** is formed in the same manner as described above with regards to the first dielectric layer **306** as illustrated in FIGS. **6-9**. In some embodiments, the conductive layer **308** is formed in the same manner as described above with regards to the conductive layer **308**, as illustrated in FIGS. **10** and **11**.

[0042] At **204** of the second method **200**, as illustrated in FIGS. **20** and **21**, the semiconductive layer **310** is formed over the conductive layer **308**, according to some embodiments. In some embodiments, the semiconductive layer **310** is formed in the same manner as described above with regards to the conductive layer **308**, as illustrated in FIGS. **10** and **11**.

[0043] At **206** of the second method of **200**, as illustrated in FIGS. **24** and **25**, the gate **315** is formed on the semiconductive layer **310** over the channel region **304***c*, according to some embodiments. Turing to FIGS. **20** and **21**, prior to FIGS. **24** and **25**, the insulating layer **314** is formed over the first dielectric layer **306** and the semiconductive layer **310**, according to some embodiments. In some embodiments, the insulating layer **314** is formed in the same manner as described above with regards to the insulating layer **314**, as illustrated in FIGS. **14** and **15**. Turning to FIGS. **22** and **23**, the metal layer **316** is formed over the insulating layer **314**, according to some embodiments. In some embodiments, the metal layer **316** comprises at least one of tantalum or nitride. In some embodiments, the metal layer **316** has the metal layer thickness **326** between about 50 nm to about 100 nm. In some embodiments, the metal layer **316** is formed by deposition. In some embodiments, the metal layer **316** is formed over the substrate **302**, such that the metal layer **316** is connected to the gate **315**, as illustrated in FIG. **28**. Turning to FIGS. **24** and **25**, the metal layer **316** and the insulating layer **314** are patterned, such that the metal layer **316** and the insulating layer **314** are over the channel region **304***c* of the fin **304** to form the gate **315**, and over portions of the substrate **302**, according to some embodiments. In some embodiments, spacers **317** are formed adjacent the gate **315**. In some embodiments, the spacers **317** comprise nitride.

[0044] At **208** of the second method of **200**, as illustrated in FIGS. **26** and **27**, the first metal alloy **312***a* is formed over the first active region **304***a* from the conductive layer **308** and the semiconductor layer **310** and the second metal alloy **312***b* is formed over the second active region **304***b* from the conductive layer **308** and the semiconductor layer **310**, according to some embodiments. In some embodiments, the first metal alloy **312***a* and the second metal alloy **312***b* are formed in the same manner as described above with regards to the first metal alloy **312***a* and the second metal alloy **312***b*, as illustrated in FIGS. **12** and **13**, but where the gate **315** functions as the photoresist **321** to cover the channel region **304***c* of the fin **304**. Turning to FIG. **28**, the gate contact **318** is formed over the metal layer **316**, according to some embodiments. In some embodiments, the first contact **320** is formed over the first active region **304***a*, such that the first contact **320** is in contact with the first metal alloy **312***a*. In some embodiments, the second contact **322** is formed over the second active region **304***b*, such that the second contact **322** is in contact with the second metal alloy **312***b*. In some embodiments, at least one of the gate contact **318**, the first contact **320** or the second contact **322** comprises a conductive material such as metal. In some embodiments, the conductive layer **308** having the conductive layer thickness **311** over the channel region **304***c* suppresses current leakage as compared to a conductive layer having a thickness different than the conductive layer thickness **311**. In some embodiments, the semiconductive layer **310** over the conductive layer **308** in the channel region **304***c* reduces electro flux from the source to the drain, as compared to a channel region that does not have a semiconductive layer over a conductive layer. In some embodiments, the semiconductor device **300** having the first metal alloy **312***a* as at least one of the source or drain and the second metal alloy **312***b* as at least one of the source or drain requires a lower activation temperature than a semiconductor device that does not have a metal alloy as a source or a drain.

[0045] According to some embodiments, a semiconductor device comprises a first metal alloy over a first active region of a fin over a substrate and a second metal alloy over a second active region of the fin. In some embodiments, a conductive layer is over a channel region of the fin, between the first active region and the second active region; and a semiconductive layer is over the conductive layer.

[0046] According to some embodiments, a method of forming a semiconductor device comprises forming a conductive layer over a fin over a substrate, the fin having a first active region, a channel region and a second active region. According to some embodiments, the method of forming a semiconductor device comprises forming a semiconductive layer over the conductive layer, forming a first metal alloy over the first active region from the conductive layer and the semiconductive layer over the first active region and forming a second metal alloy over the second active region from the conductive layer and the semiconductive layer over the second active region.

[0047] According to some embodiments, a semiconductor device comprises a first metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon over a first active region of a fin over a substrate and a second metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon over a second active region of the fin. In some embodiments, a conductive layer having a conductive layer thickness between about 0.5 nm to about 5 nm is over a channel region of the fin, the channel region between the first active region and the second active region. In some embodiments, a semiconductive layer is over the conductive layer.

[0048] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

[0049] Various operations of embodiments are provided herein. The order in which some or all of the operations are described should not be construed to imply that these operations are necessarily order dependent. Alternative ordering will be appreciated having the benefit of this description. Further, it will be understood that not all operations are necessarily present in each embodiment provided herein. Also, it will be understood that not all operations are necessary in some embodiments.

[0050] It will be appreciated that layers, features, elements, etc. depicted herein are illustrated with particular dimensions relative to one another, such as structural dimensions or orientations, for example, for purposes of simplicity and ease of understanding and that actual dimensions of the same differ substantially from that illustrated herein, in some embodiments. Additionally, a variety of techniques exist for forming the layers features, elements, etc. mentioned herein, such as etching techniques, implanting techniques, doping techniques, spin-on techniques, sputtering techniques such as magnetron or ion beam sputtering, growth techniques, such as thermal growth or deposition techniques such as chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced chemical vapor deposition (PECVD), or atomic layer deposition (ALD), for example.

[0051] Moreover, "exemplary" is used herein to mean serving as an example, instance, illustration, etc., and not necessarily as advantageous. As used in this application, "or" is intended to mean an inclusive "or" rather than an exclusive "or". In addition, "a" and "an" as used in this application and the appended claims are generally be construed to mean "one or more" unless specified otherwise or clear from context to be directed to a singular form. Also, at least one of A and B and/or the like generally means A or B or both A and B. Furthermore, to the extent that "includes", "having", "has", "with", or variants thereof are used, such terms are intended to be inclusive in a manner similar to the term "comprising". Also, unless specified otherwise, "first," "second," or the like are not intended to imply a temporal aspect, a spatial aspect, an ordering, etc. Rather, such terms are merely used as identifiers, names, etc. for features, elements, items, etc. For example, a first element and a second element generally correspond to element A and element B or two different or two identical elements or the same element.

[0052] Also, although the disclosure has been shown and described with respect to one or more implementations, equivalent alterations and modifications will occur to others skilled in the art based upon a reading and understanding of this specification and the annexed drawings. The disclosure comprises all such modifications and alterations and is lim-

ited only by the scope of the following claims. In particular regard to the various functions performed by the above described components (e.g., elements, resources, etc.), the terms used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure. In addition, while a particular feature of the disclosure may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application.

What is claimed is:

1. A semiconductor device comprising:

a first metal alloy over a first active region of a fin over a substrate;

a second metal alloy over a second active region of the fin;

a conductive layer over a channel region of the fin, the channel region between the first active region and the second active region; and

a semiconductive layer over the conductive layer.

2. The semiconductor device of claim **1**, comprising a gate over the channel region comprising:

an insulating layer over the channel region; and

a metal layer over the insulting layer.

3. The semiconductor device of claim **2**, the insulating layer comprising at least one of hafnium, zirconium or oxide.

4. The semiconductor device of claim **2**, the metal layer comprising at least one of tantalum or nitride.

5. The semiconductor device of claim **1**, at least one of:

the first metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon; or

the second metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon.

6. The semiconductor device of claim **1**, comprising a first dielectric layer over a top surface of the substrate, between the conductive layer and the substrate and between the semiconductive layer and the substrate, the first dielectric layer comprising at least one of silicon or oxygen.

7. The semiconductor device of claim **6**, comprising an insulating layer over the first dielectric layer.

8. The semiconductor device of claim **1**, at least one of:

the conductive layer having a conductive layer thickness between about 0.5 nm to about 5 nm, or

the semiconductive layer having a semiconductive layer thickness between about 0.1 nm to about 3 nm.

9. The semiconductor device of claim **1**, at least one of:

the conductive layer comprising germanium, or

the semiconductive layer comprising silicon.

10. A method of forming a semiconductor device comprising:

forming a conductive layer over a fin over a substrate, the fin having a first active region, a channel region and a second active region;

forming a semiconductive layer over the conductive layer;

forming a first metal alloy over the first active region from the conductive layer and the semiconductive layer over the first active region; and

forming a second metal alloy over the second active region from the conductive layer and the semiconductive layer over the second active region.

11. The method of claim **10**, comprising forming a gate over the channel region of the fin and adjacent sidewalls of the fin.

12. The method of claim **11**, the forming a gate comprising:

forming an insulating layer over the channel region of the fin and adjacent the sidewalls of the fin; and

forming a metal layer over the insulting layer.

13. The method of claim **10**, at least one of:

the forming a first metal alloy comprising performing a sputter deposition comprising at least one of nickel, platinum, gold, tantalum, gadolinium or titanium; or

the forming a second metal alloy comprising performing a sputter deposition comprising at least one of nickel, platinum, gold, tantalum, gadolinium or titanium.

14. The method of claim **10**, the forming a conductive layer comprising epitaxially growing germanium over the fin.

15. The method of claim **10**, at least one of the forming a first metal alloy or the forming a second metal alloy comprising annealing at a temperature between about 250° C. to about 750° C. for a duration between about 5 s to about 70 s.

16. The method of claim **10**, comprising forming a first dielectric layer over a top surface of the substrate prior to the forming a conductive layer.

17. The method of claim **10**, the forming a semiconductive layer comprising epitaxially growing silicon over the conductive layer.

18. The method of claim **10**, comprising at least one of:

forming a gate contact connected to a gate that is over the channel region; or

forming a first contact connected to the first metal alloy.

19. A semiconductor device comprising:

a first metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon over a first active region of a fin over a substrate;

a second metal alloy comprising at least one of nickel, platinum, gold, tantalum, gadolinium, titanium, germanium or silicon over a second active region of the fin;

a conductive layer having a conductive layer thickness between about 0.5 nm to about 5 nm over a channel region of the fin, the channel region between the first active region and the second active region; and

a semiconductive layer over the conductive layer.

20. The semiconductor device of claim **19**, comprising a gate over the channel region comprising:

an insulating layer comprising at least one of hafnium, zirconium or oxide over the channel region; and

a metal layer comprising at least one of tantalum or nitride over the insulting layer.

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