Short-Channel Metal-Gate TFTs With Modified Schottky-Barrier Source/Drain

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***Abstract*—A thin active layer, a fully silicided source/drain (S/D), a modified Schottky-barrier, a high dielectric constant (high-κ) gate dielectric, and a metal gate are integrated to realize high-performance thin-film transistors (TFTs). Devices with 0.1-μm gate length were fabricated successfully. Low threshold voltage, low subthreshold swing, high transconductance, low S/D resistance, high on/off current ratio, and negligible threshold voltage rolloff are demonstrated. It is thus suggested for the first time that the short-channel modified Schottky-barrier TFT is a solution to carrier out three-dimension integrated circuits and system-on-panel.**

***Index Terms*—Thin-film transistor (TFT), Schottky-barrier (SB), silicide.**

I. Introduction

SILICON based thin-film transistors (TFTs) are widely used for the active-matrix liquid crystal display (AMLCD) as drivers of the liquid crystal. Furthermore, TFTs will help to carry out the three-dimensional integrated circuits (3D-ICs) or multilayer Si ICs for system-on-chip (SoC) applications and fully functional system-on-panels (SoPs) in the future [1]–[3]. In order to improve the performance of TFTs, lots of effort has been devoted to the thin-film crystallization technology [4]–[6]. Suppressing channel defects by a thinner gate dielectric is another approach [7]–[9]. On the other hand, gate length (L_g) scale down is a straightforward approach. However, serious short-channel effects and the performance nonuniformity of short-channel TFTs retard their applications [6], [7].

Recently, Schottky-barrier (SB) MOSFETs have been investigated for the nanoscale devices due to their simple processing, low temperature, low thermal budget, compatibility with conventional MOSFETs, and easy scaling [10]–[13]. The SB MOSFETs utilize metal–silicide or metal-like materials instead of heavily doped silicon to form source/drain (S/D). Metal silicides are formed at low temperature with low thermal budget so that the high temperature activation of source/drain dopant can be eliminated. For electrical aspect, a fixed potential barrier of source junction exists at the silicide/silicon Schottky contact and is insensitive to the electric field coming from the drain so that the drain-induced barrier lowering (DIBL) is suppressed and the roll-off of threshold voltage is alleviated [12].

In this letter, we combine the factors of the SB source/drain, metal gate, and thin effective gate oxide thickness (EOT) to fabricate deep-submicrometer TFTs. Low threshold voltage, low subthreshold swing, high transconductance, low S/D resistance, high on/off current ratio, and good control of threshold voltage down to 0.1-μm gate length are demonstrated.

II. Experiments

The starting material was a 6-in Si wafer. After standard RCA clean, 150-nm thermal oxide was grown as the bottom oxide layer (BOX) followed by an amorphous silicon (a-Si) layer of 50 nm deposition in a low-pressure chemical-vapor-deposition (LPCVD) system at 550 °C. The a-Si active layer was then recrystallized by a solid-phase crystallization (SPC) process at 600 °C in N_2 ambient for 24 h. The grain size is distributed in the range of 0.1 to 0.5 μm. The active layer was patterned by E-beam lithography and dry etching. The high-κ gate dielectric, HfO_2, film was deposited immediately after a diluted HF dip to a thickness of 10 nm at 500 °C in a metal–organic chemical vapor deposition (MOCVD) system. Ta/Pt alloy was selected as the metal gate electrode because of its thermal stability on HfO_2 dielectric and tunable work function [14]. The metal gate electrode was patterned by liftoff process. After gate patterning, HfO_2 layer on S/D region was removed by wet etching.

After a 50-nm-thick SiO_2 spacer formation, the active layer at the S/D region was fully converted to Ni silicide by a two-step annealing technique. A 22-nm Ni layer was deposited and wafers were annealed at 300 °C for 1 h in a vacuum to form Ni_2Si at first. At this temperature, Ni does not react with the TaPt gate. Then, the unreacted Ni was removed selectively by sulfuric acid. A second annealing at 600 °C for 30 s was performed in a rapid thermal annealing (RTA) system to transform Ni_2Si to NiSi. After the NiSi SB S/D formation, some wafers were implanted by BF_2^+ at 10 keV to a dose of 1×10^{15} cm^{-2} followed by an RTA at 600 °C for 90 s in N_2 ambient to form a modified SB (MSB) junction [10]. Finally, interlayer dielectric deposition and aluminum interconnect patterning completed the device fabrication. Before measurement, an NH_3 plasma treatment was performed at 300 °C for 1 h to passivate the crystalline defects.

III. Results and Discussions

Fig. 1(a) and (b) shows the schematic device structures of SB TFT and MSB TFT, respectively. The corresponding energy band diagrams are shown in Fig. 2(a) and (b). The present of

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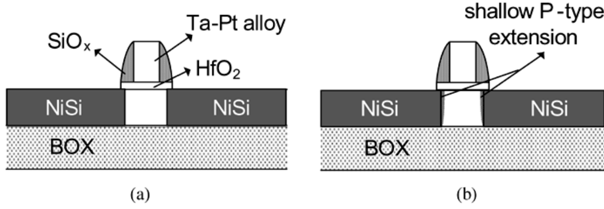

Fig. 1. Cross-sectional drawings of (a) the SB S/D TFT and (b) the MSB S/D TFT.

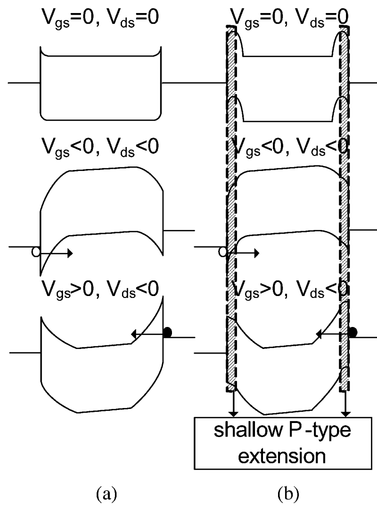

Fig. 2. Band diagrams of p-channel (a) SB TFT and (b) MSB TFT operated at various gate voltages. Replacing the p-type extension by n-type extension, n-channel devices can be obtained.

NiSi/Si SB junction at the source/body boundary offers a potential barrier for holes of about 0.5 eV. Under a sufficiently high gate bias which can plenty narrow the potential barrier width, carriers can tunnel through the SB. At the positive gate bias, the tunneling current will be electron dominant, while at negative gate bias it will be hole dominant. Since the NiSi has a work function slightly lower than the midgap of Si, hole tunneling is easier than electron tunneling. Therefore, the NiSi SB TFT tends to be p-type devices. Comparing with the energy bands of SB TFTs, the shallow p-type extension of MSB TFTs further modifies the width of NiSi/Si SB so that at negative gate bias the width of potential barrier is thinner for hole while at positive gate bias the width is thicker for electron. This means that the shallow p-type extension can increase the hole tunneling current and suppress the electron tunneling current. This mechanism is confirmed by the I_d–$V_{\rm gs}$ characteristics of SB TFT and p-type MSB TFT as shown in Fig. 3. This is the first time that the $I_{\rm on}/I_{\rm off}$ ratio of TFT with a gate length of 0.1 μm can be higher than 10^6 and the minimum $I_{\rm off}$ is lower than 10^{-11} A/μm at $V_{\rm ds} = -1$ V. The subthreshold swing is also improved to 0.28 V/dec by the MSB junction. The hole mobility is about 10 cm^2/V·s. This is the typical value that can be obtained by the SPC method.

To verify the effect of the SB junction, the maximum transconductance (G_m) at linear region is investigated at first. The linear region G_m is basically determined by the channel resistance and tunneling resistance of the SB junction [12]. As shown in Fig. 4(a), the G_m increases rapidly with the decrease

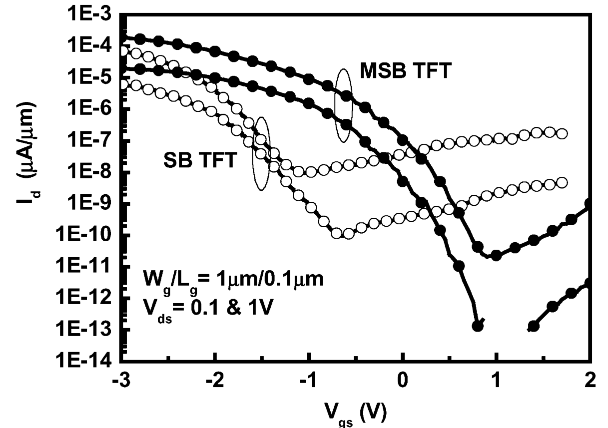

Fig. 3. Transfer characteristics $(I_d$–$V_{\rm gs})$ of SB TFT and p-channel MSB TFT. The gate length and channel width are 0.1 and 1 μm, respectively.

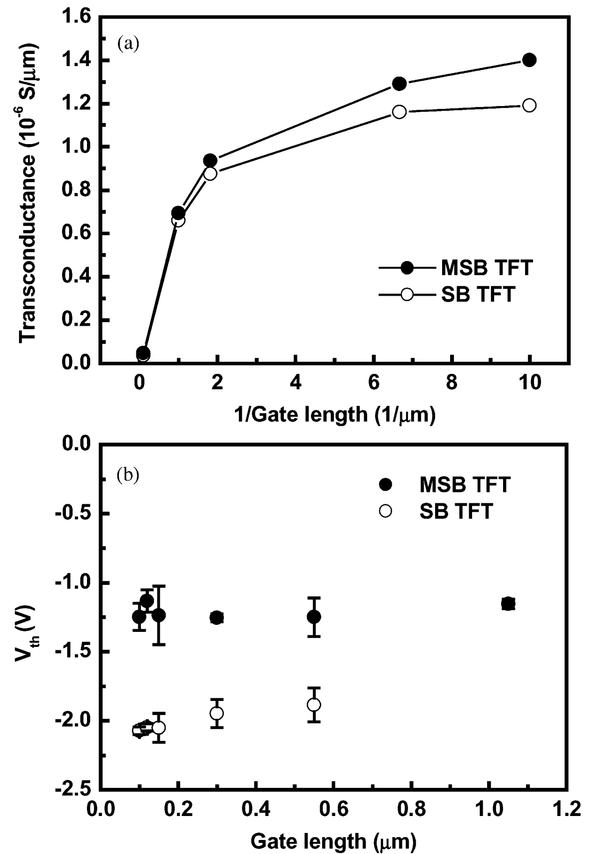

Fig. 4. (a) Maximum transconductance (G_m) and (b) threshold voltage $(V_{\rm th})$ of SB TFTs and MSB TFTs as a function of gate length measured at $V_{\rm ds} = -0.1$.

of gate length and then tends to be saturated. It is known that the channel resistance is linearly proportional to the gate length while the resistance of the SB junction is almost independent of the gate length. The measured G_m changes from linearly dependent to independent on the gate length. This implies that the G_m of long-channel SB TFTs ($L_g > 1$ μm) is mainly determined by the channel resistance and the G_m of short-channel SB TFTs is mainly determined by the SB junction. This observation is in agreement for both SB TFTs and MSB TFTs. For the long-channel devices, the G_m is determined by the channel

resistance so that the G_m of SB TFTs and MSB TFTs are almost the same. On the other hand, the G_m of short-channel TFTs is dependent upon the resistance of SB junction so that the MSB TFTs have higher G_m than that of the SB TFTs.

Similar effects are observed in the threshold voltage $(V_{\rm th})$ as shown in Fig. 4(b). The $V_{\rm th}$ is almost independent upon gate length. The low $V_{\rm th}$ of MSB TFTs is the result of the shallow p-type extension which causes thinner barrier width. As the gate length becomes close to or smaller than the grain size, the numbers of grain boundary in channel region becomes few. The magnitude of $V_{\rm th}$ deviation would increase with the decrease of gate length if the $V_{\rm th}$ is determined by the potential barrier of grain boundary. The fact of the $V_{\rm th}$ deviation does not degrade even if the gate length is reduced to 0.1 μm also supports the inference that the $V_{\rm th}$ is controlled by the SB.

Due to the low threshold voltage $(V_{\rm th})$, the $I_{\rm off}$ at $V_{\rm gs} = 0$ V and $V_{\rm ds} = -1$ V is about 1×10^{-8} A/μm. This value is higher than that of the conventional TFTs but is lower than the specification of high-performance circuits [15]. If lower $I_{\rm off}$ is required, thinner gate dielectric (better swing), higher channel concentration (higher $V_{\rm th}$), or a new gate electrode with lower work function (higher $V_{\rm th}$) may be adapted.

IV. Conclusion

Gate length scaling offers a notable benefit on device performance improvement. The issues of the threshold voltage rolloff and $I_{\rm off}$ increase of the short channel device are solved by the MSB S/D junction. The effects of channel defects are suppressed by the thin active layer and thin gate dielectric layer. By integrating these advanced features, a 0.1 μm gate length TFT is demonstrated with low threshold voltage, low subthreshold swing, high transconductance, low S/D resistance, high on/off current ratio, and negligible threshold voltage roll-off. These observations imply that the MSB TFTs fabricated with low temperature processes are a potential solution to carry out high performance TFTs for 3-D integrated circuit and SoP applications.

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