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A PARALLEL COUPLED-LINE FILTER USING VLSI BACKEND INTERCONNECT WITH HIGH RESISTIVITY SUBSTRATE

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Abstract

This paper reports our progress in developing parallel coupled-line filters based on Si-based VLSI backend interconnects for millimeter-wave applications. The resonant frequency of this coupled-line filter increases with increasing spacing-gap and with increasing IDM thickness. By using high resistivity substrate, the parallel coupled-line band-pass filter is extremely effective in reducing substrate loss, and also provides very low insertion loss, even at the millimeter-wave regime. In addition, the parallel coupled-line filter suitable for advanced system-on-a-chips at the millimeter wave application achieves high performance characteristics, which show low insertion loss, wide band, and compatibility with standard VLSI process.

Keywords: parallel coupled-line filter, VLSI, high resistivity substrate, millimeter-wave.

1. Introduction

The strong demand on advanced wireless communication services for advanced system-on-a-chips has attracted a great deal of attention. This is due

to their significant benefits such as overall chip size reduction, lower fabrication cost, as well as enhanced system performance. Meanwhile, significant progress in advanced VLSI technology [1] has made it possible to realize system-on-a-chip at millimeter-wave frequencies [2]. The concept of integrating parallel coupled-line filters with CMOS integrated circuit on silicon (Si) substrate is appealing because shorter coupling-line has shown on backend local or globe interconnects with CMOS scaling down [3]. This requirement becomes even more urgent as the operation frequency of Si communication integrated circuits (ICs) increases. However, the performance of microwave filters integrated on Si [4] suffers from the high frequency losses and crosstalk of the low resistivity Si substrate [5]. This is the fundamental limitation of Si-based RF circuits [6]. To improve the high-frequency performance of band-pass filter, in this paper, we present our recent progress in implementing the VLSI backend interconnects [7], a novel interconnect concept for millimeter-wave silicon MMIC's using high resistivity substrate technology, which can reduce losses from Si substrate [8]. The superior performance of the parallel coupled-line filter [9] in broadband and insertion loss denotes its applicability to advanced millimeter-wave wireless communication systems.

2. Design and fabrication

To imitate the interconnects, such as those shown schematically in Fig. 1, two long coupled lines were fabricated with lengths of 1 mm long and with different line-spacing of 10, 5, and 2.5 μm. Different inter-metal dielectric (IMD) thickness of 0.7 or 6 μm were used to simulate the local or global interconnects using metal-1 (M1) or metal-6 (M6) layers of the 1-Poly-6-Metal (1P6M) structures shown in Fig. 1.

Fig. 2 shows the die photo of fabricated 1 mm coupled lines with 10 μm spacing width, where additional co-planar waveguide (CPW) structure and 150 μm spacing GSG probing pads were used to study the parallel coupled-line filter. The CPW coupled lines were fabricated by 2 μm thick Al metal on

PECVD deposited IMD SiO_2 above the Si substrate. The S_{21} and S_{11} are the signal transmission from port 1 to port 2 and return loss of port 1, respectively. This approach was necessary due to non-ideal open and short in the RF regime. For comparison, we also investigated coupled lines on high-resistivity Si (HRS) substrates, which had a resistivity of 1.5×10^4 Ω-cm. The fabricated coupled lines were characterized by S-parameters measurements using an HP8510C network analyzer with standard RF calibration up to 50 GHz. The EM simulation results using IE3D (Zeland Software) were also demonstrated for comparison.

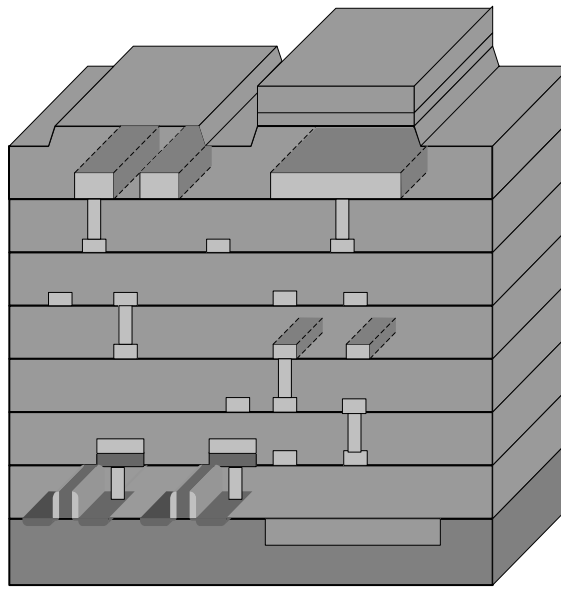


Fig. 1. The standard VLSI process on a Si-based technology showing multi-level parallel interconnects.

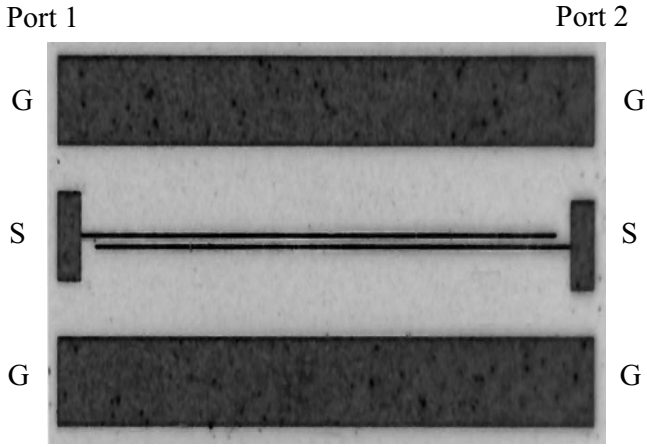


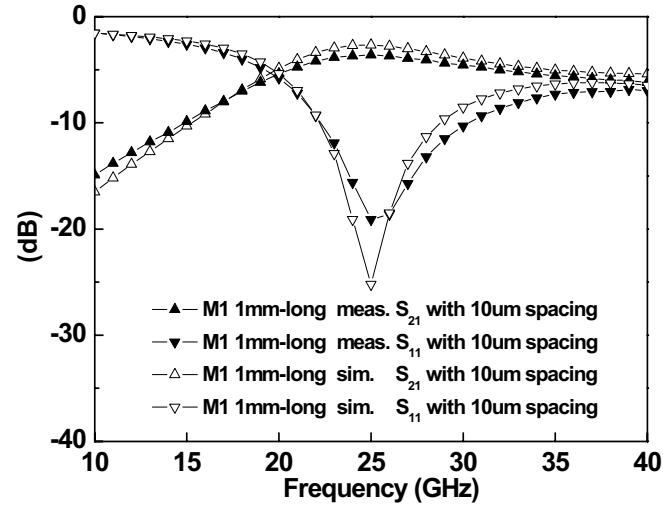
Fig. 2. The die photo of a fabricated 1 mm length parallel coupled-line filter with 10 μm gap-spacing width.

3. Experimetal results and discussion

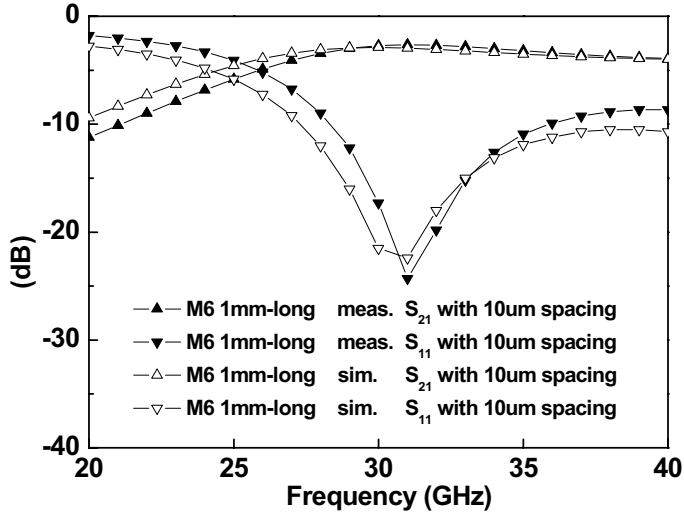
Fig. 3(a) shows the simulated and measured results for a 1 mm long interconnect parallel coupled-line filter with 10 μm spacing-gap on 0.7 μm SiO_2-isolated low-resistivity Si (LRS) substrates (M1). At the resonant frequency of 25 GHz, the poor RF characteristics of measured band-pass filter, such as the insertion loss of 3.6 dB, are unacceptable for filter use. However, this structure of parallel coupled-line filter based on VLSI backend interconnects has the advantage of integrating microwave and millimeter wave devices into the ICs. The measured result is in good agreement with the simulated result, which implies that the IE-3D simulator is reliable for verifying.

For comparison, the simulated and measured results for a 1 mm long interconnect parallel coupled-line filter with 10 μm spacing-gap on 6 μm SiO_2-isolated low-resistivity Si substrates (M6) are also plotted in Fig. 3(b). From the measured and simulated results, we can find that the resonant

frequency increases as the IMD thickness increases. In addition, it can be seen that the simulated and measured insertion losses are almost the same at the resonant frequency, which are 2.73 dB and 2.94 dB respectively. The slight reduction of insertion loss and the shifted resonant frequency in this coupled-line filter are apparently due to the increasing IMD thickness as compared with Fig. 3(a). However, the insertion loss and the bandwidth are still inadequate for advanced wireless communication application at high frequency range.



(a)



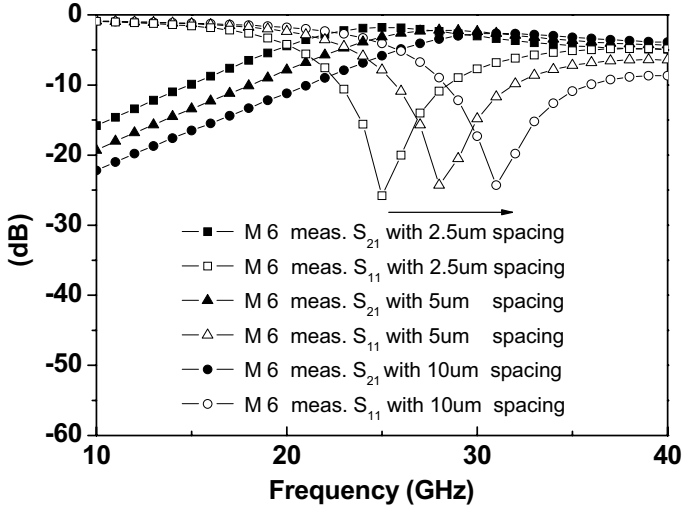
(b)

Fig. 3. The measured and simulated S_{21} and S_{11} responses for 1 mm long, 10 μm-spaced parallel lines filter on (a) 0.7 μm SiO_2-isolated Si LRS (b) 6 μm SiO_2-isolated Si LRS.

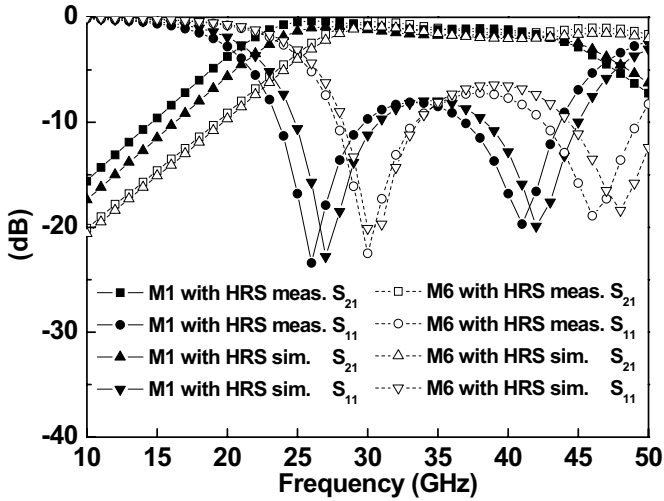
From the view of advanced VLSI backend process, we also made a study of a 1 mm long interconnect parallel coupled-line filter with different spacing-gap of 2.5 μm, 5 μm, and 10 μm on 6 μm SiO_2-isolated low-resistivity Si substrates (M6) in Fig. 4(a). It is seen that the resonant frequency increases from 25, 28, to 31 GHz with the increasing of the spacing-gap in 2.5 μm, 5 μm, and 10 μm. Meanwhile, the insertion losses of measured results are 3.1, 2.81 and 2.63 dB for each resonant frequency, respectively. From this result, it is more effective to enhance the resonant frequency of the parallel coupled line filters by increasing the spacing-gap between the two coupled-lines than increasing the IMD thickness. Taking the optimized geometry of spacing-gap between two coupled-lines, the expected resonant frequency of this parallel coupled line filters can be extracted. That will offer a good choice to design the filters.

By using high resistivity silicon substrate (HRS), the measured S_{21} and S_{11} responses of 1 mm long interconnect parallel coupled-line filter with 10 μm spacing-gap shown in Fig. 4(b). The simulation for ideal designed filters is included for comparison. From the figure, the S_{11} response of the measured parallel coupled-line filter on 0.7 μm SiO_2-isolated HRS shows good performance in enhancing its stop-band characteristics, which has two transmission zeros at 26 GHz and 41 GHz with an attenuation level of 23.4 dB and 19.7 dB, and the S_{21} response is as small as 1.1 dB at the central frequency of 33.5 GHz. The in-band insertion loss has a minimum of 0.3 dB at 26 GHz and increases smoothly with frequency. Besides, the simulated and measured S_{21} and S_{11} responses of 1 mm long interconnect parallel coupled-line filter with 10 μm spacing-gap on 6 μm SiO_2-isolated HRS also are plotted in Fig. 4(b). The central frequency of this measured parallel coupled-line filter is shifted to 38.5 GHz with the measured S_{21} of 1.4 dB, and the two rejection bands of that are centered at frequencies of 30 and 46 GHz, respectively. The flat insertion loss in the pass-band, with a minimum of 0.4 dB, is suitable for the band-pass filters using at the millimeter-wave range.

The great improvement in the insertion loss and bandwidth as compared with those shown in Fig. 3 is due to the high resistivity Si substrate that reduces the loss paths. The central frequency of this band-pass filter increases with the IMD thickness and the good characteristics of this band-pass filter, such as low insertion loss, broad bandwidth, integratable with VLSI technology, and extending its bandwidth at millimeter wave regime are all demonstrated by this parallel coupled-line filter basing on the HRS substrate.



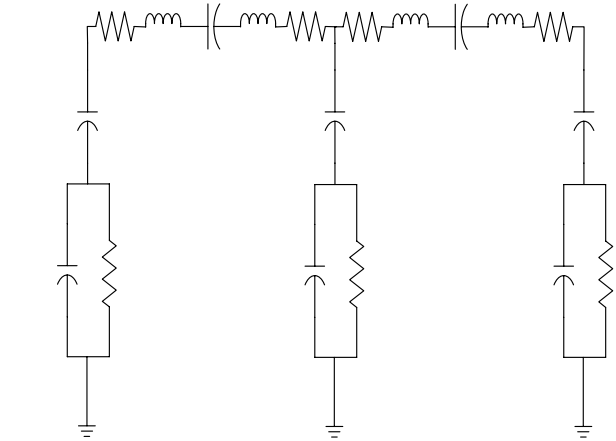
(a)



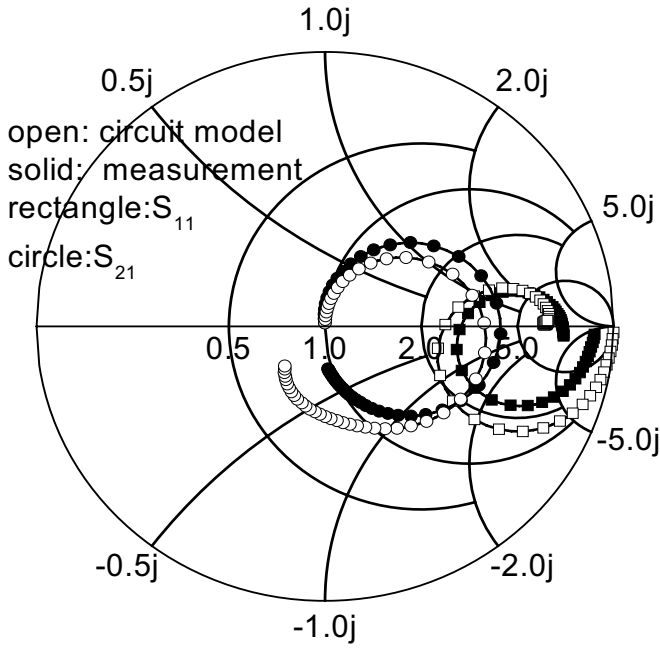
(b)

Fig. 4. (a) Comparison of S_{21} and S_{11} responses for 1 mm long parallel lines filter using with different spacing-gap of 2.5, 5, and 10 μm on 6 μm SiO_2-isolated Si LRS. (b) The measured and simulated S_{21} and S_{11} responses of 1 mm long, 10 μm-spaced parallel lines filter on 0.7 μm and 6 μm SiO_2-isolated Si HRS.

Fig. 5(a) shows the equivalent circuit model of the interconnect parallel coupled-line filter. The equivalent circuit of the substrate RC network includes the C_{ox}, which is the capacitance contributed by the IMD SiO_2, and the R_{sub} and the C_{sub}, which are the shunt resistance and capacitance modelling the effect of lossy silicon substrate. In the equivalent circuit of the two coupled line, L_1 and R_1 are the series inductance and parasitic resistance of the interconnect line body, L_2 and R_2 are the series inductance and parasitic resistance of the nearby interconnect line body, and the C_{couple} is the coupling capacitance between the two parallel coupled-lines. In order to verify this equivalent circuit, Fig. 5(b) shows the S-parameter result for a 1 mm long interconnect parallel coupled-line filter with 10 μm spacing-gap on 6 μm SiO_2-isolated LRS substrates. The consistency between the measured and modeling results from S-parameter proves that the equivalent circuit is suitable for modelling the parallel coupled line filter. Besides, the modelling results reveal that, using an HRS substrate, leakage losses from the substrate RC network can be significantly reduced, therefore improving high-frequency performances.



(a)



(b)

Fig. 5. (a) The equivalent circuit of two parallel coupled interconnect lines with substrate RC network (b) The S-parameter of measured and circuit model.

4. Conclusion

High performance millimeter-wave band-pass filters based on standard VLSI backend process are successfully demonstrated. By using the high resistivity Si substrate, the parallel coupled-line filters have good characteristics such as low insertion loss, broadband, and compact size. This novelty of using VLSI backend interconnect with high resistivity substrate provides an attractive solution for low-cost high-performance wireless application up to millimeter-wave frequency range.

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