materials

MDPI

Article

Microwave Annealing for NiSiGe Schottky Junction on SiGe P-Channel

Yu-Hsien Lin [1,*], Yi-He Tsai [1], Chung-Chun Hsu [2], Guang-Li Luo [3], Yao-Jen Lee [3] and Chao-Hsin Chien [2,3]

Received: 10 September 2015 ; Accepted: 5 November 2015 ; Published: 10 November 2015
Academic Editor: Jung Ho Je

1 Department of Electronic Engineering, National United University, Miaoli 36003, Taiwan; a246792001@yahoo.com.tw
2 Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 30010, Taiwan; arthur00403@hotmail.com (C.-C.H.); chchien@faculty.nctu.edu.tw (C.-H.C.)
3 National Nano Device Laboratories, Hsinchu 30010, Taiwan; glluo@narlabs.org.tw (G.-L.L.); yjlee@ndl.narl.org.tw (Y.-J.L.)
* Correspondence: yhlin@nuu.edu.tw; Tel.: +886-3-738-2533; Fax: +886-3-736-2809

Abstract: In this paper, we demonstrated the shallow NiSiGe Schottky junction on the SiGe P-channel by using low-temperature microwave annealing. The NiSiGe/n-Si Schottky junction was formed for the Si-capped/SiGe multi-layer structure on an n-Si substrate ($Si/Si_{0.57}Ge_{0.43}/Si$) through microwave annealing (MWA) ranging from 200 to 470 °C for 150 s in N_2 ambient. MWA has the advantage of being diffusion-less during activation, having a low-temperature process, have a lower junction leakage current, and having low sheet resistance (Rs) and contact resistivity. In our study, a 20 nm NiSiGe Schottky junction was formed by TEM and XRD analysis at MWA 390 °C. The NiSiGe/n-Si Schottky junction exhibits the highest forward/reverse current (I_{ON}/I_{OFF}) ratio of ~3×10^5. The low temperature MWA is a very promising thermal process technology for NiSiGe Schottky junction manufacturing.

Keywords: germanium; microwave annealing; NiSiGe; Schottky junction

1. Introduction

As the devices are being continuously scaled down for logic circuits, higher mobility channel materials such as Ge or SiGe have been considered to boost the driving current [1–5]. However, most high mobility materials have a significantly smaller bandgap as compared to Si, which will result in a higher band-to-band tunneling leakage. Therefore, S/D (Source/Drain) and channel engineering must play leading roles for boosting device performance. First, the parasitic series resistance should be reduced. The low dopant solid solubility in Ge results in the large S/D series resistance. A large S/D series resistance can be restrained by introducing metal germanide S/D. Second, the shallow junction is needed. The interface between the metal and the semiconductor is abrupt and can be easily governed by the reactant metal thickness and the process thermal budget, which indicates a high potential for scalability [6]. Third, simpler device fabrication could be achieved for the Schottky device without ion implantations and the high temperature annealing for dopant activation [7,8].

NiSiGe is the most promising candidate due to its low resistivity for the junction contact [9–12]. For reducing the thickness of the NiSiGe layer of the Schottky junction, the process temperature needs to be reduced. However, a lower process temperature results in a higher NiSiGe resistance due to the small crystallite size of the NiSiGe layer. These are the major challenges of scaling Ge CMOS (Complementary Metal-Oxide-Semiconductor) into nanoscale devices. Therefore, in order to avoid the dopant diffusion effect, which is dominant at high annealing temperatures,

low-temperature annealing with microwave excitation appears to offer a promising microwave annealing (MWA) process that may be an alternative to other rapid thermal processing methods in silicon processing [13–15]. Microwaves could repair the damage in the Schottky junction formation and provide the lower leakage current for the Schottky junction device.

In this paper, we propose a NiSiGe/n-Si Schottky junction formed by microwave annealing in the Si-capped SiGe Schottky junction devices ($Si/Si_xGe_{1-x}/Si$, x = 0~1). The shallow junction with a 20 nm depth has been fabricated with a high effective barrier height (ϕ_B^{eff}) and low leakage current in the devices.

2. Experimental Section

Figure 1 shows the schematic diagram and process flow of fabricating the NiSiGe/n-Si Schottky junction structure. The Schottky junction devices were fabricated on a four-inch silicon wafer. The multi-layer structure of $Si/Si_{0.57}Ge_{0.43}$ (1 nm/2 nm/n-Si) was grown by an ultra-high vacuum chemical vapor deposition system (UHVCVD, CANON ANELVA Corporation (Kanagawa, Japan)) on an n-type Si substrate. The channel was composed of a 1-nm-thick Si cap and a 2-nm-thick SiGe layer with biaxial compressive strain and was grown at 420–500 °C and 550 °C, respectively. The isolation film of 420 nm SiO_2 was deposited on the multi-layer architecture after series surface cleaning. Then, the definition of the junction active area was accomplished with lithography and wet-etching. Because of the bulk annealing characteristics of the microwave, the technique was utilized to form NiSiGe as a low-leakage Schottky junction ranging from 200 to 470 °C for 150 s in N_2 ambient. The un-reacted Ni film was removed, followed by Al deposition as the back contact.

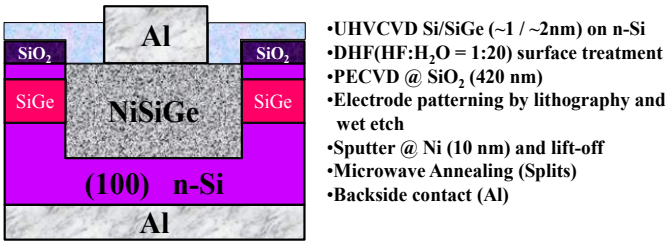

Figure 1. Schematic diagram and process flow of fabricating the NiSiGe/n-Si Schottky junction structure.

3. Results and Discussion

Figure 2 shows the high resolution TEM images of an approximately 1 nm/2 nm Si/SiGe film for the multi-layer $Si/Si_{0.57}Ge_{0.43}$/n-Si structure before MWA. The SiGe/Si lattice interface image shows the good polycrystalline structure. The inset figure shows the NiSiGe film after MWA at 390 °C. A 20-nm relative uniformity of the NiSiGe film and a distinct interface between the NiSiGe and Si could be observed.

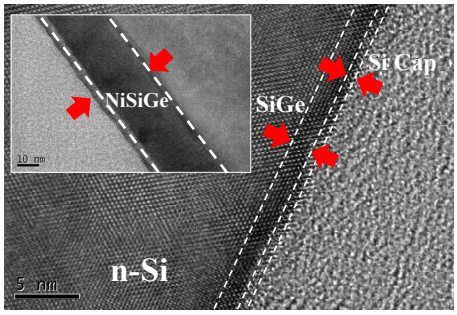

Figure 2. The cross-sectional TEM images show the polycrystalline structure in the Si/SiGe/n-Si lattice interface image. The inset figure shows the NiSiGe Schottky junction through MWA at 390 °C.

The result of the grazing incidence of X-ray diffraction (GIXRD) analysis was shown in Figure 3. From this figure, the descriptions of power 0.5, power 2, power 4 are 300 W, 1200 W, 2400 W, respectively. Moreover, the temperature measurements of the above power splits are 200 °C, 390 °C, and 470 °C, respectively. Many peaks are shown, which correspond to the crystalline nickel monogermanide; implementing 390 °C for 150 s MWA is sufficient to form polycrystalline NiGe and NiSiGe. The peaks corresponding to (011), (200), (112), (211), and (020) NiSi and (111) NiSiGe were clearly identified [16]. Performing the MWA at 390 °C for 150 s was sufficient to form the NiSi and NiSiGe phase for forming the Schottky junction.

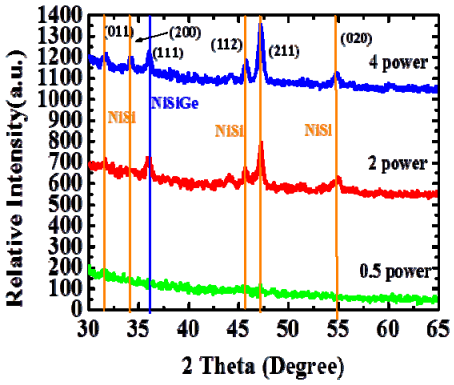

Figure 3. The GIXRD spectra for MWA with different power splits, confirming the NiSiGe formation.

Figure 4 shows the *I*–*V* characteristics of the fabricated NiSiGe/n-Si Schottky junction; the NiSiGe formation during MWA conditions was at 200 °C, 330 °C, 390 °C, 420 °C, and 470 °C for 150 s, respectively. After forming NiSiGe with MWA annealing, the forward currents and reverse leakage currents of all NiSiGe/n-Si contacts gradually decreased from 200 °C to 390 °C. However, increasing the annealing temperature from 200 °C to 470 °C, the forward currents and reverse leakage currents are degraded accordingly. The NiSiGe/n-Si Schottky junction exhibits the highest forward/reverse current ratio of ~2.5 × 10^5 at MWA 390 °C. This result also indicates that the series resistance can be significantly reduced after the SiNiGe formation at the condition of MWA 390 °C. Note that if using relatively high temperature MWA annealing at >470 °C, the crystallization became more significant and which was shown by the increased intensity of the GIXRD peak in Figure 3. This issue will potentially degrade the uniformity, cause more defects induce at the interface, and affect the leakage current of the junction increase.

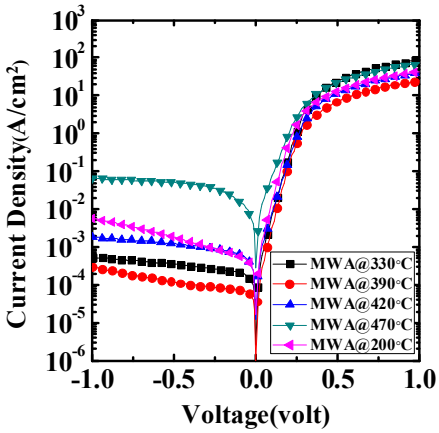

Figure 4. The *I*–*V* characteristics of the NiSiGe/n-Si Schottky junction annealed at different MWA temperatures.

Figure 5 shows the effective electron SBH (Schottky barrier height) and ideality factor of NiSiGe/n-Si Schottky junctions with different MWA temperatures. For a typical or moderate doped semiconductor, the *I–V* characteristics of the Schottky diode could be described by:

$$I = I_S \exp\left(\frac{qV_a}{nK_BT} - 1\right) \tag{1}$$

with

$$I_S = AA^*T^2 \exp\left(\frac{q\phi_B^{eff}}{K_BT}\right) \tag{2}$$

where I_s is the saturation current, A is the diode area, V_a is the applied voltage, A^* is the effective Richardson constant [17,18], ϕ_B^{eff} is the SBH, and n is the ideality factor. The ideality factor n and SBH ϕ_B^{eff} can be derived as:

$$n = \left(\frac{q}{K_BT}\right)\left(\frac{\partial V}{\partial[\ln I]}\right) \tag{3}$$

and

$$\phi_B^{eff} = \frac{K_BT}{q}\ln\left(\frac{A^*T^2}{J_S}\right) \tag{4}$$

By using Equation (3), we extract the ideal factor n and SBH ϕ_B^{eff} from each MWA sample of a different temperature in the I–V characteristics of Figure 4. From Figure 5, we can observe that the SBH and the ideality factor of the MWA 390 °C condition are 0.63 eV and 1.01, and it shows good electrical characteristics of Schottky junctions.

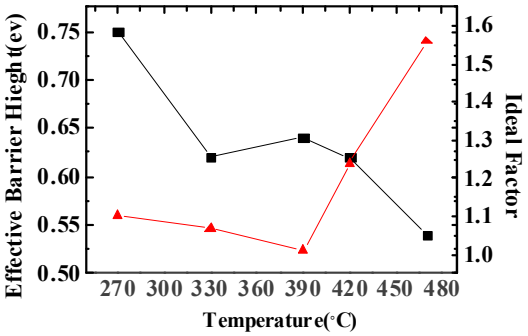

Figure 5. SBH and ideality factor of NiSiGe/n-Si Schottky contact with different MWA temperatures.

4. Conclusions

This paper realized the shallow NiSiGe Schottky junction on the SiGe P-channel by using low-temperature microwave annealing. The formation of junction defects could be suppressed and prevent the agglomeration due to the lower forming temperature. The microwave-annealed NiSiGe Schottky junction exhibited a superior I_{ON}/I_{OFF} ratio of about 3×10^5 formed at 390 °C as well as more stable off-current characteristics with an SBH of 0.63 eV and an ideality factor of 1.01. We believe our microwave annealing NiSiGe Schottky junction is promising for high performance logic circuits and will enable SiGe channel devices to be integrated on the Si substrate for the future applications.

Acknowledgments: The authors thank the National Science Council of the Republic of China, Taiwan, for supporting this research (104-2221-E-239-017). National Nano Device Laboratories (NDL), Taiwan, is highly appreciated for its technical support.

Author Contributions: Yu-Hsien Lin organized the research and wrote the manuscript; Yi-He Tsai and Chung-Chun Hsu performed the experiments and performed data analysis; Yu-Hsien Lin, Guang-Li Luo, Yao-Jen Lee, and Chao-Hsin Chien discussed the experiments and the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Datta, M.S.; Dewey, G.; Doczy, M.; Doyle, B.; Jin, B.; Kavalieros, J.; Kotlyar, R.; Metz, M.; Zelick, N.; Chau, R. High Mobility Si/SiGe Strained Channel MOS Transistors with HfO_2/TiN Gate Stack. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 8–10 December 2003; p. 23.
2. Goley, P.S.; Hudait, M.K. Germanium based field-effect transistors: Challenges and opportunities. *Materials* **2014**, *7*, 2301–2339. [CrossRef]
3. Claeys, C.; Simoen, E. *Germanium-Based Technologies: From Materials to Devices*, 1st ed.; Elsevier: Amsterdam, The Netherlands, 2007; pp. 1–480.
4. Delabie, A.; Bellenger, F.; Houssa, M.; Conard, T.; Elshocht, S.V.; Caymax, M.; Heyns, M.; Meuris, M. Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide. *Appl. Phys. Lett.* **2007**, *91*, 082904–082906. [CrossRef]
5. Gu, J.J.; Liu, Y.Q.; Xu, M.; Celler, G.K.; Gordon, R.G.; Ye, P.D. High performance atomic-layer-deposited LaLuO3 /Ge-on-insulator p-channel metal-oxide-semiconductor field-effect transistor with thermally grown GeO2 as interfacial passivation layer. *Appl. Phys. Lett.* **2010**, *97*, 012106–012108. [CrossRef]
6. Larson, J.M.; Snyder, J.P. Overview and status of metal s/d schottky-barrier mosfet technology. *IEEE Trans. Elec. Dev.* **2006**, *53*, 1048–1058. [CrossRef]
7. Calvet, L.E.; Luebben, H.; Reed, M.A.; Wang, C.; Snyder, J.P.; Tucker, J.R. Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect transistors. *J. Appl. Phys.* **2002**, *91*. [CrossRef]
8. Koike, M.; Kamimuta, Y.; Tezuka, T. Modulation of NiGe/Ge Schottky barrier height by S and P co-introduction. *Appl. Phys. Lett.* **2013**, *102*, 032108–032110. [CrossRef]
9. Iwai, H.; Ohguro, T.; Ohmi, S.I. NiSi salicide technology for scaled CMOS. *Mater. Adv. Met.* **2002**, *60*, 157–169. [CrossRef]
10. Roy, S.; Midya, K.; Duttagupta, S.P.; Ramakrishnan, D. Nano-scale NiSi and n-type silicon based Schottky barrier diode as a near infra-red detector for room temperature operation. *J. Appl. Phys.* **2014**, *116*. [CrossRef]
11. Zaima, S.; Nakatsuka, O.; Kondo, H.; Sakashita, M.; Sakai, A.; Ogawa, M. Silicide and germanide technology for contacts and metal gates in MOSFET applications. *ECS Trans.* **2007**, *11*, 197–205.
12. Hsu, S.L.; Chien, C.H.; Yang, M.J.; Huang, R.H.; Leu, C.C.; Shen, S.W.; Yang, T.H. Study of thermal stability of nickel monogermanide on single- and polycrystalline germanium substrates. *Appl. Phys. Lett.* **2005**, *86*, 251906–251908. [CrossRef]
13. Kappe, C.O. Controlled microwave heating in modern organic synthesis. *Angew. Chem. Int. Ed.* **2004**, *43*, 6250–6285. [CrossRef] [PubMed]
14. Lee, Y.J.; Hsueh, F.K.; Current, M.I.; Wu, C.Y.; Chao, T.S. Susceptor coupling for the uniformity and dopant activation efficiency in implanted Si under fixed-frequency microwave anneal. *IEEE Electron. Device Lett.* **2012**, *33*, 248–250. [CrossRef]
15. Alford, T.L.; Thompson, D.C.; Mayer, J.W.; Theodore, N.D. Dopant activation in ion implanted silicon by microwave annealing. *J. Appl. Phys.* **2009**, *106*. [CrossRef]
16. Sinha, M.; Lee, R.T.P.; Chor, E.F.; Yeo, Y.C. Schottky barrier height modulation of Nickel–dysprosium-alloy germanosilicide contacts for strained P-FinFETs. *IEEE Electron. Device Lett.* **2009**, *30*, 1278–1280. [CrossRef]
17. Sze, S.M. *Physics of Semiconductor Devices*, 2nd ed.; Wiley: New York, NY, USA, 1981; pp. 256–263.
18. Dimoulas, A.; Tsipas, P.; Sotiropoulos, A.; Evangelou, E.K. Fermi-level pinning and charge neutrality level in germanium. *Appl. Phys. Lett.* **2006**, *89*. [CrossRef]