



Polarity Asymmetry of Polyoxide Grown on Phosphorus In Situ Doped Polysilicon

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We show that polyoxides grown on phosphorus in situ doped polysilicon have larger polarity asymmetry than that on the POCl_3 -doped polysilicon. It may be not only the surface roughness between the polysilicon/polyoxide interfaces, but also the phosphorus distribution in the interfaces. For the phosphorus in situ doped poly film, the phosphorus piled up at the poly-1/polyoxide interface should result from the out-diffusion of the poly-1 doping during the tetraethyl orthosilicate oxide deposition process. However, the phosphorus concentration near the polyoxide/top poly-2 interface was lower than the bulk concentration of the polysilicon film, which may result from insufficient phosphorus concentration near the polyoxide/top poly-2 interface without subsequent annealing and dopant activation. Therefore, this may affect the polarity asymmetry of the electrical characteristics for the phosphorus in situ doped samples. Especially, the thermal polyoxide had the largest polarity asymmetry due to very high phosphorus concentration piled up in the bottom poly-1/polyoxide interface. We also show that the top poly-2 doping process affects the phosphorus distribution in the polysilicon/polyoxide interfaces, and further, affects the polyoxide performance.
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Thermal oxides grown on the n+ polycrystalline silicon, i.e., polyoxides, have been used as the interdielectric¹⁻⁴ for nonvolatile memory application. However, it is well known that the polyoxides have drawbacks of a lower dielectric strength and a higher leakage current than oxides grown on the single-crystal silicon due to non-uniformity polyoxide thickness and rough asperities (surface roughness). Also, the characteristics of polyoxides have been shown to depend on the structure and morphology of the predeposited polysilicon film, which in turn are affected by the deposition temperature, doping conditions, and the oxidation temperature.⁵⁻¹⁰

It was previously reported that the surface morphology could be improved by replacing the POCl_3 -doped polysilicon with the phosphorus in situ doped polysilicon deposited in the amorphous state. The polysilicon has more uniform small grains and thus a flatter and smoother interface¹¹⁻¹⁵ and the polyoxide grown on it has better electrical characteristics. It was also reported that more reliable dielectrics could be grown on polysilicon by using chemical vapor deposition (CVD) instead of thermal oxidation. For those CVD deposited dielectrics, the grain boundaries present in the bottom polysilicon are not incorporated in the deposited layer due to no polysilicon consumption and the surface of the polysilicon layer is not roughened, so the CVD oxide potentially has a defect density relatively independent of the bottom polysilicon.¹⁶⁻²²

In this paper, we present the CVD deposited polyoxide grown on the phosphorus in situ doped polysilicon, which has larger polarity asymmetry than that on the POCl_3 doped polysilicon. It may be not only the surface roughness between the polysilicon/polyoxide interfaces, but also the phosphorus distribution in the interfaces. We also discuss the effect of the poly-2 doping process for the phosphorus distribution.

Experimental

In this study, n+-polysilicon/polyoxide/n+-polysilicon capacitors were fabricated. At first, p-type wafers were thermally oxidized to have a field oxide of a thickness of 100 nm. The bottom polysilicon (poly-1) (~300 nm) was then deposited in a low-pressure chemical vapor deposition (LPCVD) system with phosphorus in situ doped at 580°C. The sheet resistance of the film was 60 Ω/sq . Then, inter-polyoxides of a thickness of about 130 Å were subsequently deposited onto the surface of the polysilicon films by pyrolysis of tetraethyl orthosilicate (TEOS) at 700°C in an LPCVD system, or thermally grown at 900°C in a diluted $\text{O}_2(\text{N}_2:\text{O}_2 = 5:1)$. A second polysilicon film (poly-2) was deposited by LPCVD and doped, also

in situ doped with phosphorus, and deposited at 580°C. For comparison, the TEOS oxide of 13 nm was deposited and the lower and upper polysilicon films were all doped with POCl_3 at 950°C. After poly-2 was patterned, all samples were grown with a 100 nm thick oxide as passivation layer. Contact holes were opened and metallized to form the capacitor structures. Finally, all devices were sintered at 350°C for 40 min in N_2 gas, which can improve the metallurgy between polysilicon and metal film, and reduce contact resistance.

Polyoxide thickness was determined by high frequency (1 MHz) Keithley capacitance-voltage (C-V) measurement. The morphology of the polyoxide/polysilicon interface was studied by AFM (atomic force microscope). For the AFM measurement of the surface to reveal the polyoxide/poly-1 interface, the TEOS oxide was removed by wet etching in the buffered HF acid. The true replica of the interface may be preserved by such a treatment because the poly-Si is not attacked by the HF-based solution. Finally, the current-voltage (I-V) characteristics were measured using an HP4145B semiconductor parameter analyzer.

Results and Discussion

Figure 1a and b shows the typical positive and negative current-field characteristics, respectively, of the polyoxides with TEOS de-

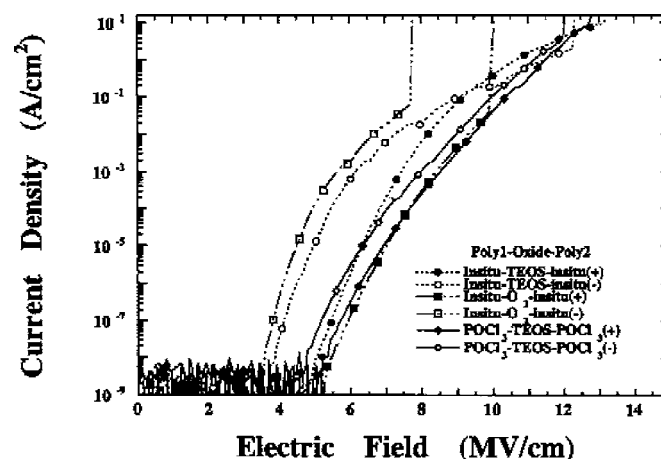
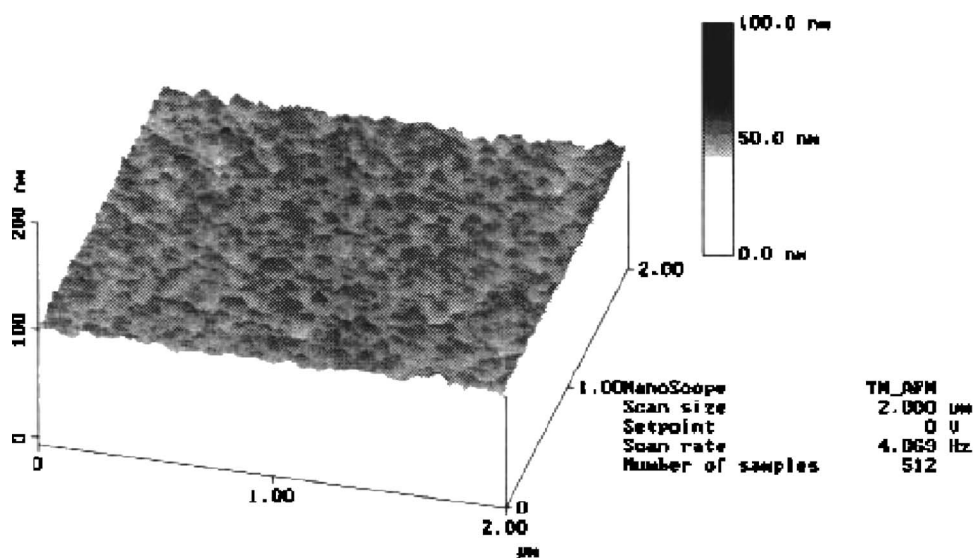


Figure 1. The positive and negative J - E characteristics of the polyoxides with TEOS deposited or thermally grown, where the top and bottom polysilicon films (poly-1 and poly-2) were phosphorus in situ doped or POCl_3 -doped films.

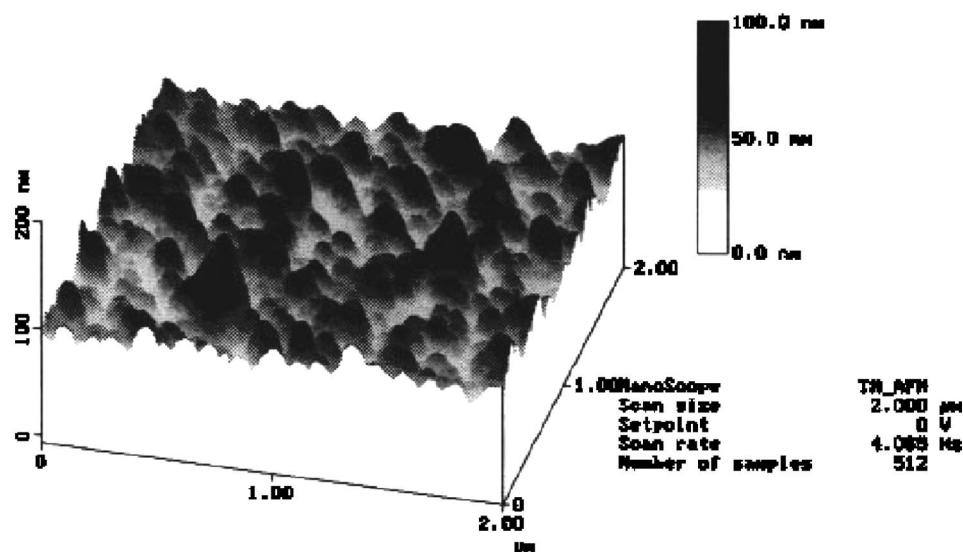
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pw16.001

(a)



pw1.000

(b)

Figure 2. The AFM images of (a) the poly-1 surface of the TEOS oxide deposited on the phosphorus in situ doped polysilicon; (b) the poly-1 surface of the TEOS oxide deposited on the POCl_3 -doped polysilicon.

posited or thermally grown, where the polysilicon films (bottom poly-1 and top poly-2) were phosphorus in situ doped and POCl_3 doped, respectively. In the figures, for the samples with deposited TEOS oxides, the in situ doped film had a higher breakdown but a higher leakage current density than those of the POCl_3 -doped film. It is also seen clearly that the polarity asymmetry of the former is larger than that of the latter. The samples with all in situ doping, the thermal oxide, had a lower E_{bd} and larger polarity asymmetry than the TEOS deposited oxide.

The polarity asymmetry may be explained by the different surface morphologies and phosphorus distribution in the bottom poly-1/polyoxide/top poly-2 interfaces. For the phosphorus in situ doped film, it had a more uniform and smooth polysilicon/polyoxide interface than that of the POCl_3 -doped film. Figure 2a and b shows the AFM images of the surfaces of the phosphorus in situ doped and

POCl_3 polysilicon films without deposited oxides, and the average roughness (R_a) values of AFM are 18 and 41 Å, respectively. The phosphorus in situ doped sample had a smaller average roughness value but with more and smaller protuberances and bumps, while the POCl_3 -doped sample had larger average roughness value but with larger protuberances and bumps at the surfaces. The more and smaller protuberances and bumps meant the in situ doped sample had a larger injection tunneling current but larger breakdown field than those of the POCl_3 -doped sample. Figure 3a and b shows the cross-section TEM images of the phosphorus in situ doped and POCl_3 -doped polysilicon films with TEOS deposited oxides, respectively. The phosphorus in situ doped polysilicon film was basically in an amorphous state which had a relatively smooth interface with the deposited TEOS oxide, but the POCl_3 -doped polysilicon film

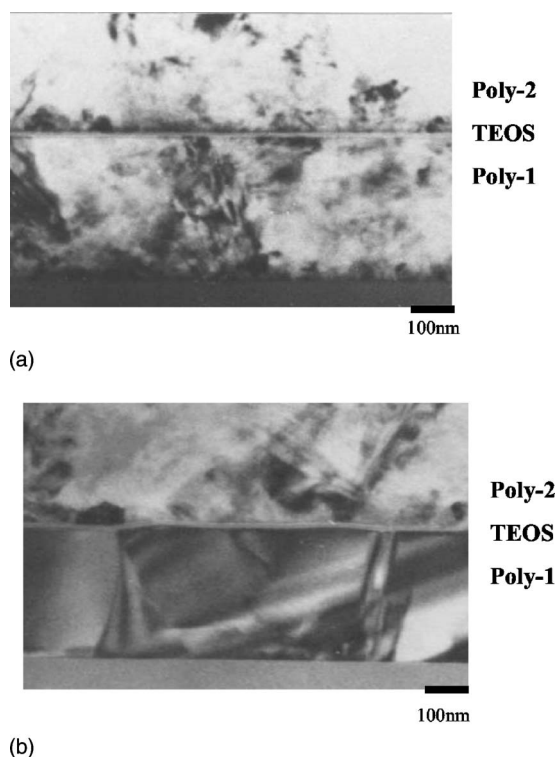


Figure 3. The TEM micrographs of (a) the TEOS oxide deposited on the phosphorus in situ doped polysilicon; (b) the TEOS oxide deposited on the POCl_3 -doped polysilicon.

was in the crystallization of the poly-grain state which had an irregular surface. Furthermore, for the sample with phosphorus in situ doped, it seems that both the top and bottom polysilicon layers remained in an amorphous state without the crystallization of polygrain.

Lee and Hu²³ reported that different polyoxides (dry oxidation, wet oxidation, and LPCVD deposition) grown on the phosphorus in situ doped polysilicon films had the same polarity dependence (i.e., the polyoxide conducts more current under $-V_g$ bias than that under $+V_g$ bias), and the polarity asymmetry of the phosphorus in situ doped polysilicon was opposite to those of the implanted and POCl_3 -doped polysilicons. Therefore, they suspect that the phosphorus in situ doped polysilicon consists of more uniform and small grains such that there is a high density of small bumps at the polysilicon/polyoxide interfaces, and the density of small bumps is higher at the top poly-2 interface than that at the bottom poly-1 interface. This seems to indicate that the top poly-2/polyoxide interface is rougher than the bottom one, where the polyoxide conducts more current under $-V_g$ negative bias (electrons injection from the top poly-2/polyoxide interface) than that under $+V_g$ positive bias (electron injection from the polyoxide/bottom poly-1 interface). The phosphorus in situ doped samples in our study also present the same polarity asymmetry.

The secondary-ion mass spectrometry (SIMS) profiles of the phosphorus concentration distribution of those samples are shown in Fig. 4. The phosphorus in situ doped sample had more of a nonuniform distribution of phosphorus concentration in the polysilicon/polyoxide interfaces than that of the POCl_3 -doped sample. For the phosphorus in situ doped poly film, the phosphorus piled up at the bottom poly-1 /polyoxide interface, but the phosphorus concentration near the polyoxide/top poly-2 interface was lower than the bulk concentration of the polysilicon film. Apparently, the phosphorus precipitated in the bulk of the polyoxide can be largely suppressed.

It is suspected that the phosphorus in situ doped polysilicon film under lower doping temperature with or without subsequent anneal-

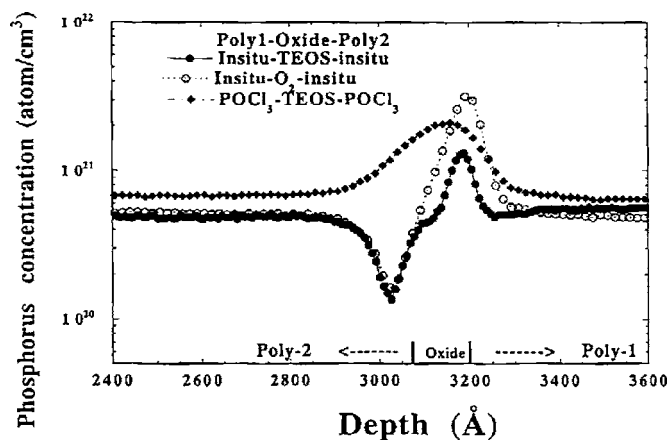


Figure 4. The phosphorus SIMS profiles of the deposited and thermally grown oxides on the phosphorus in situ doped or POCl_3 -doped polysilicon films.

ing process resulted in a less uniform distribution of the phosphorus concentration at the polysilicon/polyoxide interfaces.²⁴ For the bottom poly-1 film with phosphorus in situ doped, the phosphorus piled up at the bottom poly-1/polyoxide interface should result from the out-diffusion of the poly-1 doping during the TEOS oxide deposition process. However, for the top poly-2 film also with phosphorus in situ doped under lower doping temperature, the phosphorus concentration near the polyoxide/top poly-2 interface was lower than the bulk concentration of the polysilicon film, which may result from insufficient phosphorus concentration near the polyoxide/top poly-2 interface without subsequent annealing and dopant activation. Therefore, this may affect the polarity asymmetry of the electrical characteristics for the phosphorus in situ doped samples. Furthermore, the thermal oxide grown on the in situ doped film had the lowest E_{bd} and largest polarity asymmetry of those of the TEOS deposited oxides. Thermal oxidation not only increased polysilicon consumption to enhance interface roughness, but also resulted in the phosphorus out-diffusion to make a very high phosphorus concentration piled up at the poly-1/polyoxide interface to result in the largest nonuniformity distribution. This also shows the largest polarity asymmetry and poor polyoxide quality (low electric field breakdown).

The POCl_3 -doped poly film had higher phosphorus concentration distributed uniformly at the poly-1/polyoxide/poly-2 interfaces and bulk due to the phosphorus out-diffusion during the high-temperature POCl_3 process. Therefore, the sample with POCl_3 doped had the smallest polarity asymmetry of those samples with phosphorus in situ doped. So, except for interface roughness, the phosphorus distribution in the polyoxide interfaces may be another reason for the polarity asymmetry.

Figure 5 shows the curves of gate voltage shift (ΔV_g) vs time of the oxides on both types of doped polysilicon films under a constant $\pm 10 \mu\text{A}/\text{cm}^2$ current stressing. The area of the test capacitor was $5 \times 10^{-4} \text{cm}^2$. All the increases in gate voltage were seen to be due to electron trappings. For the deposited oxides samples, the in situ doped devices exhibited lower electron trapping rates than those of the POCl_3 -doped devices in the positive and negative stresses. This is because the sample with phosphorus in situ doped had more smooth interface and less phosphorus concentration in the oxide. However, the thermal oxide grown on the phosphorus in situ doped poly film, had higher trapping rates in the positive stress than that of deposited samples due to the largest phosphorus piled up in the poly-1/polyoxide interface during high-temperature oxidation process. The lower trapping rate under the negative stress is due to the centroid of thermally grown oxide being farther away from the poly-2/polyoxide interface than that of deposited polyoxides from the below discussion.

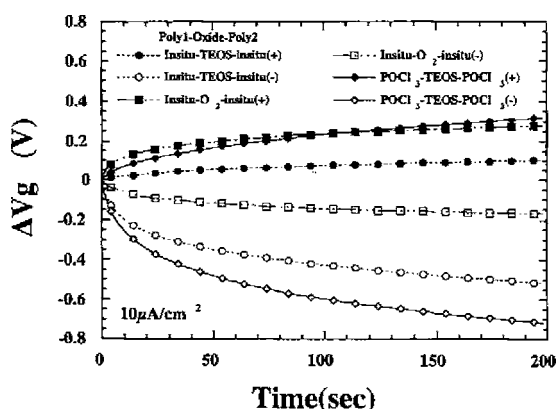


Figure 5. The curves of gate voltage shifts (ΔV_g) vs time of the deposited and thermally grown oxides on both types of doped poly films under $\pm 10 \mu\text{A}/\text{cm}^2$ stress.

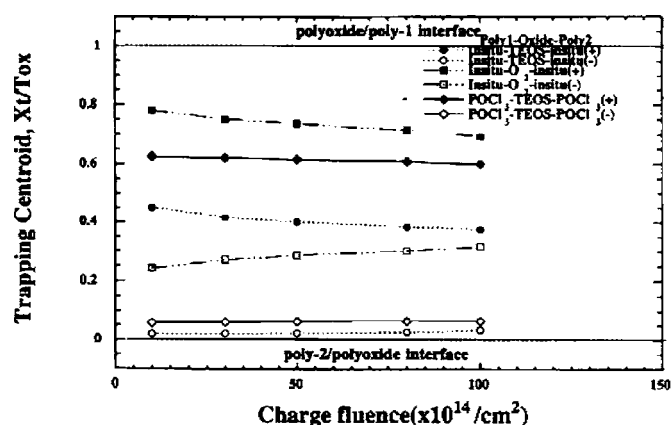
The centroids of trapped charges (X_t) and the trapped charge as a function of injected charges Q_t in the polyoxides were measured by the bidirectional I - V method.^{25,26} By comparing the deviations of Fowler-Nordheim I - V characteristics before and after stresses for both polarities, we calculate the average location of trapped charges from the following equations

$$X_t = \Delta V_{g+} / (\Delta V_{g+} + \Delta V_{g-}) * T_{ox}$$

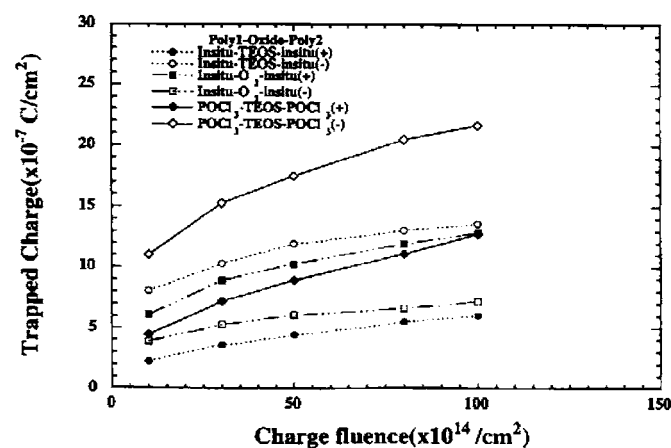
$$Q_t = (\Delta V_{g+} + \Delta V_{g-}) * \epsilon_{ox} / T_{ox}$$

where X_t is measured from the top poly-2/polyoxide interface; ΔV_{g+} denotes the voltage shift when the poly-2 is positively biased; ΔV_{g-} denotes the voltage shift when the poly-2 is negatively biased; T_{ox} and ϵ_{ox} are thickness and permittivity of the polyoxide, respectively. Figure 6a and b presents the centroids of trapped charges (X_t) and the trapped charge (Q_t) of these oxides for the positive and negative constant current injections. In Fig. 6a, one can find that the X_t of the deposited oxide on the sample with phosphorus in situ doped was further away from the polyoxide/poly-1 interface than that of the sample with POCl_3 doped. This may be because the sample with phosphorus in situ doped had more smooth interfaces and less phosphorus concentration in the polyoxide, which also induce smaller trapped charges than that of the sample with POCl_3 doped in Fig. 6b. The X_t of the thermal oxide grown on the phosphorus in situ doped poly film was near the polyoxide/poly-1 interface under $+V_g$ stress, but far away from the polyoxide/poly-2 interface under $-V_g$ stress than those of the deposited oxide. It means that the thermal oxide had higher trapping rates in the positive stress but lower trapping rate in the negative stress. This effect may be because thermal oxidation could enhance the polyoxide/poly-1 interface roughness and large amount of phosphorus to make higher trapping rates in the positive stress. But, the thermal process could obtain good bonding in the polyoxide/poly-2 interface to reduce these nonbridging and dangling bonds of the low-temperature deposited oxide in the negative stress, which also induces the smallest trapped charge for the thermal oxide under $-V_g$ stress in Fig. 6b.

In order to investigate the phosphorus concentration variance in the polyoxide interfaces, two samples were prepared by depositing TEOS oxide all on the phosphorus in situ doped poly-1 film at first and then deposited with the phosphorus in situ doped and POCl_3 -doped poly-2 films, respectively. Figure 7 shows the SIMS data for the two samples. It is seen clearly that the top poly-2 film of the sample with POCl_3 doped had larger phosphorus concentration in the polyoxide than that with phosphorus in situ doped, even though their bottom poly-1 films were all phosphorus in situ doped. This is because the high-temperature POCl_3 doping (950°C) process caused larger phosphorus out-diffusion into the polyoxide and also



(a)



(b)

Figure 6. The trapped (a) centroids and (b) charges of the deposited and thermally grown oxides on both types of doped poly films under $\pm 10 \mu\text{A}/\text{cm}^2$ stress.

induced higher V_g shift under the constant $\pm 10 \mu\text{A}/\text{cm}^2$ current stressing in Figure 8. Figure 9a and b shows the effect of the phosphorus in the trapped charges and centroids. It can be seen that the top poly-2 film of the sample with POCl_3 doped had larger trapped

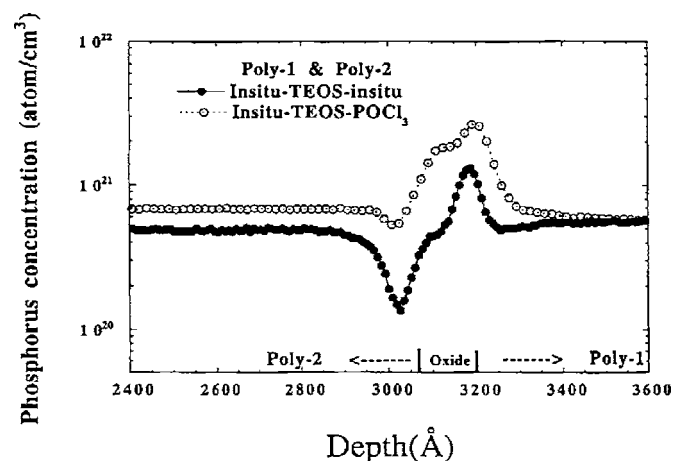


Figure 7. The phosphorus SIMS profiles of the oxide deposited on the phosphorus in situ doped poly(poly-1), but the poly-2 doping were phosphorus in situ doped and POCl_3 doped.

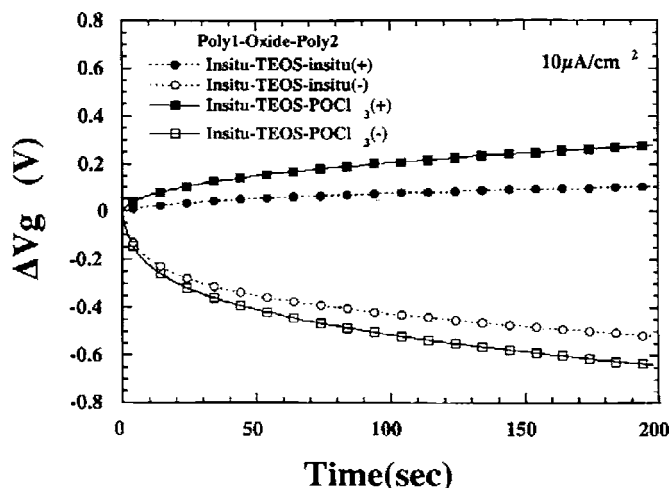
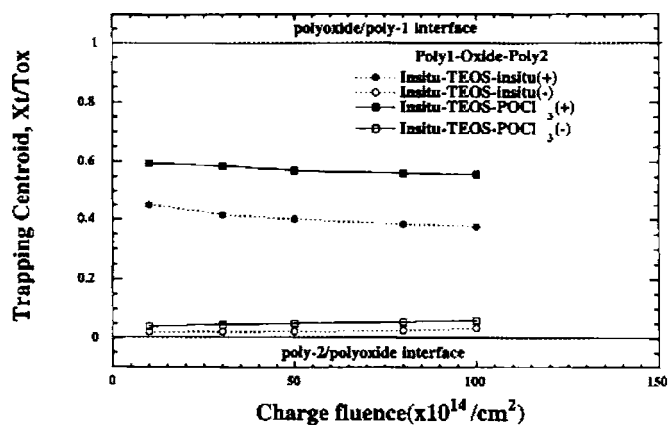
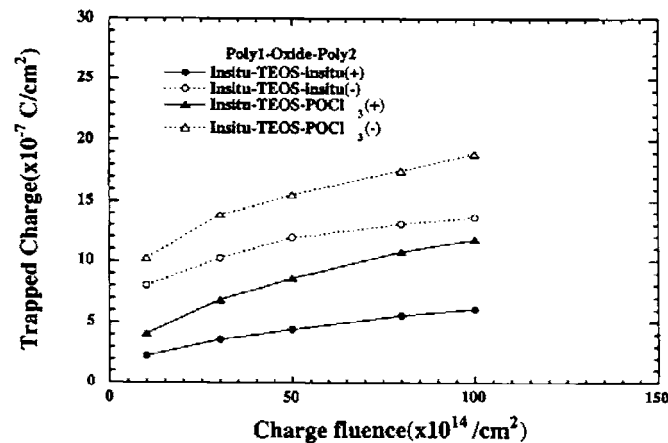


Figure 8. The curves of gate voltage shifts (ΔV_g) vs time for the deposited oxides with both types of doped poly-2 films under $\pm 10 \mu\text{A}/\text{cm}^2$ stress.

charges than that with phosphorus in situ doped and made the centroids closer to the polyoxide/poly-1 interface. We suspect that not only poly-1 doping but also poly-2 doping processes all vary phosphorus distribution in the polysilicon/polyoxide interfaces, further affecting the polyoxide quality.



(a)



(b)

Figure 9. The trapped (a) centroids and (b) charges of the deposited oxides with both types of doped poly-2 films under $\pm 10 \mu\text{A}/\text{cm}^2$ stress.

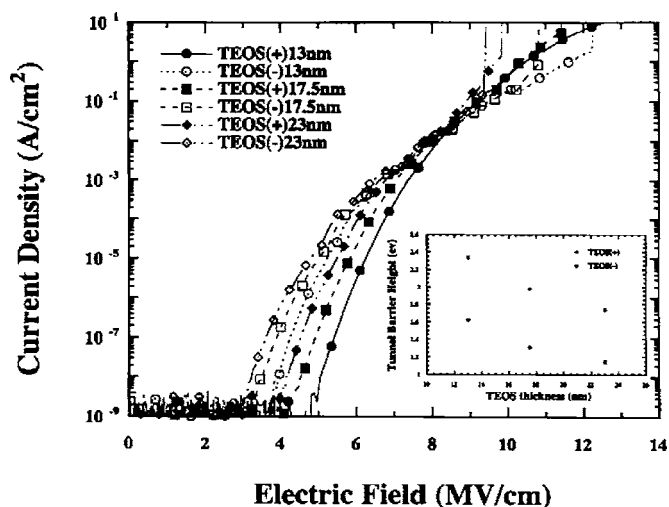


Figure 10. The positive and the negative J - E characteristics of the TEOS oxides deposited on the phosphorus in situ doped poly films at thickness of 130, 175, and 230 Å, respectively.

Figure 10 shows the positive and the negative J - E characteristics of the TEOS oxides deposited on the phosphorus in situ doped poly films at thickness of 130, 175, and 230 Å, respectively. Upon increasing the oxide thickness both J - E characteristics decreased, i.e., the E_{db} decreased and the leakage current increased. The thicker deposited oxides had more defect densities and dangling bonds, which also results in the inferior characteristics. Figure 11 shows the Weibull charge-to-breakdown (Q_{bd}) plots for these different deposited polyoxide thicknesses. This exhibits also the same trend as the J - E characteristics; the thicker the oxide is, the lower the Q_{bd} is. The thinnest oxide (130 Å) exhibits the largest Q_{bd} ($+V_g$: 10 coul/cm², $-V_g$: 2 coul/cm²).

Conclusion

The polyoxide on the phosphorus in situ doped polysilicon had larger polarity asymmetry than that on the POCl_3 -doped polysilicon. This may be not only the surface roughness between the polysilicon/polyoxide interfaces, but also the phosphorus distribution in the interfaces. The phosphorus in situ doped polysilicon film under lower

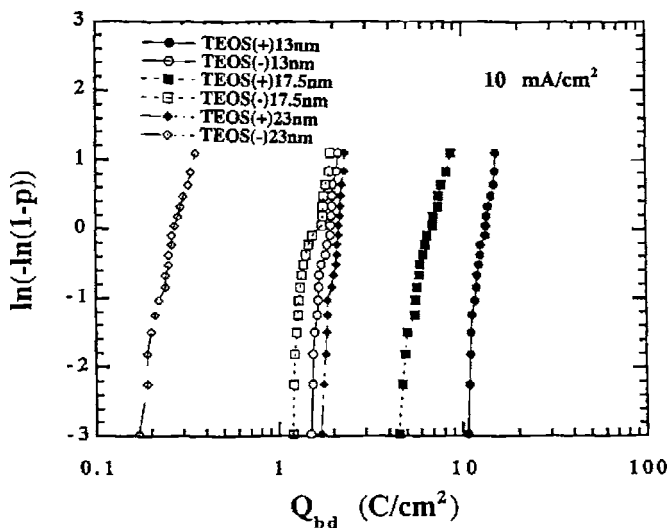


Figure 11. The Weibull charge-to-breakdown (Q_{bd}) plots for these different deposited polyoxide thicknesses under $\pm 10 \text{ mA}/\text{cm}^2$ stress.

doping temperature with or without subsequent annealing process resulted in a less uniform distribution of the phosphorus concentration at the polysilicon/polyoxide interfaces. For the film with phosphorus in situ doped, the phosphorus piled up at the bottom poly-1/polyoxide interface should result from the out-diffusion of the bottom poly-1 doping during the TEOS oxide deposition process. However, the phosphorus concentration near the polyoxide/top poly-2 interface was lower than the bulk concentration of the polysilicon film, which may result from insufficient phosphorus concentration near the polyoxide/top poly-2 interface without subsequent annealing and dopant activation. Therefore, this may affect the polarity asymmetry of the electrical characteristics for the phosphorus in situ doped samples. Furthermore, the thermal oxide grown on the in situ doped film had the lowest E_{bd} and largest polarity asymmetry due to very high phosphorus concentration piled up at the bottom poly-1/polyoxide interface. Otherwise, the top poly-2 film of the sample with $POCl_3$ doped had larger phosphorus concentration in the polyoxide than that with phosphorus in situ doped, even though their bottom poly-1 films were all phosphorus in situ doped. Therefore, not only poly-1 doping but also poly-2 doping processes all vary phosphorus distribution in the polysilicon/polyoxide interfaces, further affecting the polyoxide quality.

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References

1. T. Hamada, Y. Saito, M. Hirayama, H. Aharoni, and T. Ohmi, *IEEE Electron Device Lett.*, **22**, 423 (2001).
2. S. Mori, N. Arai, Y. Kaneko, and K. Yoshikawa, *IEEE Trans. Electron Devices*, **ED-38**, 270 (1991).
3. S. Mori, Y. Y. Araki, M. Sato, H. Meguro, H. Tsunoda, E. Kamiya, K. Yoshikawa, N. Arai, and E. Sakagami, *IEEE Trans. Electron Devices*, **43**, 47 (1996).
4. T. S. Chao, W. L. Yang, C. M. Cheng, T. M. Pan, T. F. Lei, "High quality interpoly dielectrics deposited on the nitrided-polysilicon for nonvolatile memory devices," *VLSI Technology, Systems, and Applications*, 2001 International Symposium, April 18–20, 2001, p. 142–145.
5. L. Faraone, R. Vibronck, and J. Mc Ginn, *IEEE Trans. Electron Devices*, **ED-32**, 577 (1985).
6. L. Faraone, *IEEE Trans. Electron Devices*, **ED-33**, 1785 (1986).
7. P. A. Heimann, S. P. Murarka, and T. T. Sheng, *J. Appl. Phys.*, **53**, 6240 (1982).
8. C. Cobianu, O. Popa, and D. Dascalu, *IEEE Electron Device Lett.*, **14**, 213 (1993).
9. K. Shinada, S. Mori, and Y. Mikata, *J. Electrochem. Soc.*, **132**, 2185 (1985).
10. S. L. Wu, C. Y. Chen, T. Y. Lin, C. L. Lee, T. F. Lei, and M. S. Liang, *IEEE Trans. Electron Devices*, **ED-44**, 153 (1997).
11. M. Sterheim, E. Kinsbron, J. Alspector, and P. Heimann, *J. Electrochem. Soc.*, **130**, 1735 (1983).
12. M. Hendriks and C. Mavero, *J. Electrochem. Soc.*, **138**, 1466 (1991).
13. C. Cobianu, O. Popa, and D. Dascolu, *IEEE Electron Device Lett.*, **14** (1993).
14. C. H. Kao, C. S. Lai and C. L. Lee, *IEEE Electron Device Lett.*, **18**, 526 (1997).
15. C. H. Kao, C. S. Lai, and C. L. Lee, *J. Electrochem. Soc.*, **153**, G128 (2006).
16. J. H. Klootwijk, M. H. H. Weusthof, H. Van Kranenburg, P. H. Woerlee, and H. Wallinga, *IEEE Electron Device Lett.*, **17**, 358 (1996).
17. J. H. Klootwijk, M. H. H. Weusthof, H. Van Kranenburg, P. H. Woerlee, and H. Wallinga, *IEEE Trans. Electron Devices*, **46**, 1435 (1999).
18. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Trans. Electron Devices*, **45**, 1927 (1998).
19. J. W. Lee, C. L. Lee, T. F. Lei, and C. S. Lai, *IEEE Trans. Electron Devices*, **48**, 743 (2001).
20. T. F. Lei, J. Y. Cheng, S. Y. Shiau, T. S. Chiao, and C. S. Lai, *IEEE Trans. Electron Devices*, **45**, 912 (1998).
21. P. Candelier, F. Mondon, B. Guillaumont, G. Reibold, and F. Martin, *IEEE Electron Device Lett.*, **18**, 306 (1997).
22. T. F. Lei, J. H. Chen, M. F. Wang, T. S. Chao, *IEEE Trans. Electron Devices*, **47**, 1545 (2000).
23. J. C. Lee and C. Hu, *IEEE Trans. Electron Devices*, **35**, 163 (1988).
24. J. V. Grahn, J. Pejnefors, M. S. Sanden, S.-L. Zhang, and M. Osiling, *J. Electrochem. Soc.*, **144**, 3952 (1997).
25. M. S. Liang, N. Radjy, W. Cox, and S. Cagnina, *J. Electrochem. Soc.*, **136**, 3786 (1989).
26. Z. H. Liu, P. T. Lai, and Y. C. Cheng, *IEEE Trans. Electron Devices*, **38**, 344 (1991).