Electromigration Lifetime Improvement of Copper Interconnect by Cap/Dielectric Interface Treatment and Geometrical Design

M. H. Lin, Y. L. Lin, J. M. Chen, M.-S. Yeh, K. P. Chang, K. C. Su, and Tahui Wang, *Senior Member, IEEE*

***Abstract*—A significant improvement of electromigration (EM) lifetime is achieved by modification of the preclean step before cap-layer deposition and by changing Cu cap/dielectric materials. A possible mechanism for EM lifetime enhancement was proposed. Cu-silicide formation prior to cap-layer deposition and adhesion of Cu/cap interface were found to be the critical factors in controlling Cu electromigration reliability. The adhesion of the Cu/cap interface can be directly correlated to electromigration median-time-to-failure and activation energy. Effects of layout geometrical variation and stress current direction were also investigated.**

***Index Terms*—Copper electromigration (EM), Cu/cap interface, Cu-silicide, preclean treatment.**

I. Introduction

THE back-end-of-line (BEOL) *RC* delay has gradually become a major limiting factor of circuit performance as a result of the rapid shrinkage of critical dimensions. With the reduced resistivity and dielectric constant, copper and low-*k* dielectric materials have attracted increasingly attention for future interconnect technology. The reliability of Cu/low-*k* interconnects has become an important concern for the 0.13 μm technology node and beyond. Cu electromigration is the key issue that limits the lifetime of advanced interconnect systems. The rapid shrinkage of Cu conductor dimensions while maintaining high current capability and reliability emerges to be a serious challenge.

The Cu/cap dielectric interface is the dominant diffusion path in Cu damascene interconnects. Different surface treatments can significantly affect EM result. Various approaches including special process steps and cap layer materials have been used to increase the current capability of Cu lines. Lloyd *et al.* [1] found that the adhesion between Cu and the upper surface cap material can be directly correlated to electromigration lifetime. Hatano *et al.* [2] reported electomigration lifetime improvement using a P-SiC cap layer as compared with P-SiN. Hu *et al.* [3] reported improved electromigration lifetime of Cu interconnection with a selective electroless metal coating of CoWP, CoSnP, or Pd, on the top surface of Cu damascene lines. Fisher and Glasow [4], [5] discussed the influences of the preclean process after via-etch and SiN cap deposition for different preclean intensity. However, few studies have been done on the effect of cap-layer preclean on median-time-to-failure (MTF) of EM. Therefore, the present study focuses on the correlation between electromigration lifetime and Cu surface cap-layer process. An especially suitable EM test structure to evaluate the properties of Cu cap-layer interface was well designed. The three level damascene Cu interconnect line was produced to do a series of experiments. This paper illustrates the interface between the Cu line and the dielectric capping layer, and shows the dependence of EM on current direction, capping layer materials, preclean treatment before dielectric layer deposition, and includes geometry design. The results of this study indicate that the Cu cap-layer preclean treatment and the adhesion of the Cu/cap interface can be directly correlated to the electromigration lifetime of Cu interconnects.

II. Experimental Detail

The EM tests were carried out at the package level. Sample was fabricated using Cu dual damascene process. The TaN/Ta liner and Cu seed layers were deposited sequentially by using plasma vapor deposition method. In addition, resputtering TaN/Ta layers leads to excellent side wall coverage, and void-free vias. The sample size per EM test was more than 20. Stress temperatures were in the range of 250 °C $\sim$ 350 °C (typically 300 °C). The current density used was reduced to the range of 0.6 $\sim$ 1.6 $\times$ 10^6 A/cm^2 (defined with respect to the cross section of metal line) in order to control temperature raise due to Joule heating to less than 5 °C even for low-*k* materials with low thermal conductivity. Testing was conducted typically at 300 °C with a current density of 1.6 $\times$ 10^6 A/cm^2. The EM failure criterion was defined as a 20% increase in resistance or when extrusion monitor current exceeds 1 μA. The EM structure used in the tests described below is shown in Fig. 1(a). Two stress current directions were investigated naming "downstream" and "upstream." The "downstream" case is defined according to the electrons flowing from the upper wide metal line over the via into the narrow metal line below and "upstream" is defined for

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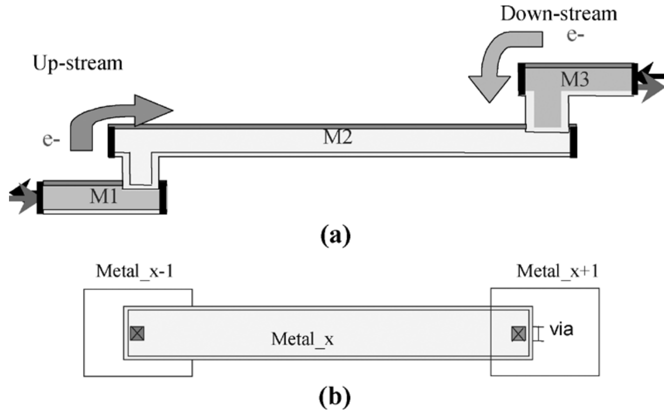


Fig. 1. (a) Via terminated line structure used in the present work. Stress direction is defined by electron current flow direction. (b) Top view of wide line with single via. The width of Metal $= 0.42\ \mu$m equals approximation $3\times$ via diameter $(0.14 \times 0.14\ \mu\text{m}^2)$.

TABLE I
PROCESS SPLIT STUDIED IS SUMMARIZED. THE PRE-CLEAN A AND PRE-CLEAN B REPRESENTED VARIOUS GAS SPECIES AND THE GAS FLOW USED. THE CAP-LAYER SiCN IS A NITRIDED FORM OF SiC

Process split	Pre-treatment parameter	Cap-layer Materials
1	pre-clean-A	PE-SiN
2	pre-clean-B	PE-SiN
3	pre-clean-A	SiCN
4	pre-clean-B	SiCN

the electrons flowing from lower wide metal line through via into the upper narrow metal line. The wide trench line with single via was used to eliminate the liner redundancy effect and to characterize the mass transport at the Cu/Cap dielectric interface [Fig. 1(b)]. It consists of a 0.42 μm wide; 400 μm long dual damascene Cu M2 line connected with a single via diameter $0.14 \times 0.14\ \mu\text{m}^2$. The test structure with a fully landed via was particularly suitable for verifying the character of the Cu/cap interface. In this work, the electromigration behavior of dual damascene Copper interconnects was evaluated using low-*k* materials $(k = 2.65 \sim 3.6)$ for the 0.13 μm node and advanced BEOL technology. A chemical vapor deposited SiOC $(k = 2.65)$ and fluorosilicate glass (FSG, $k = 3.6$) was used as intermetal dielectrics (IMD) materials, SiOC was used to evaluate the effect of pretreatment and cap-layer materials. Fluorosilicate glass (FSG) was used to examine the geometrical effect. The EM test samples were processed with different cap layer pretreatments and cap-layer materials. The process split studied is summarized in Table I. The preclean A and preclean B represented different gas species and the gas flow used. The cap-layer SiCN was a nitrided form of SiC. Quantitative adhesion data were obtained from modified edge liftoff test (m-ELT) [6] and four-point bending measurement [7]. The film stack of samples was Si/PEOX/Liner/Cu/PE-SiN or SiCN. The reported adhesion results were averaged from ten samples.

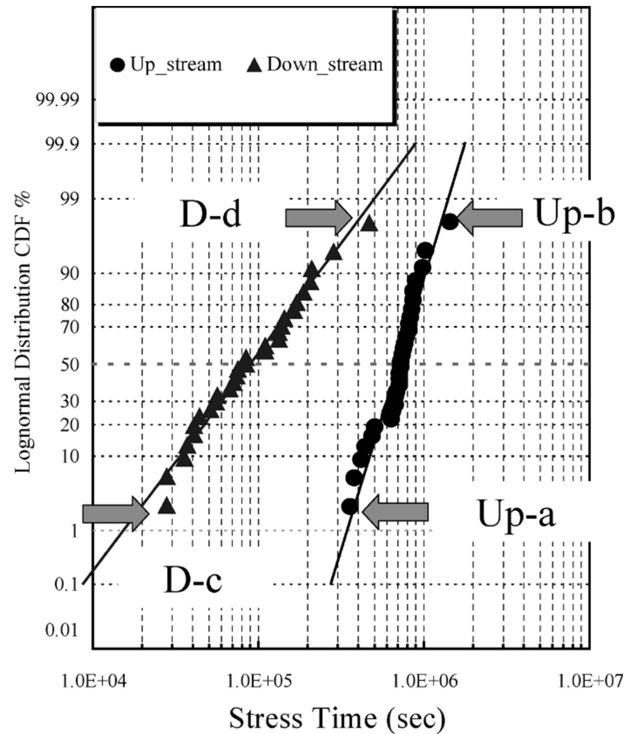


Fig. 2. Lognormal time-to-failure distribution plots for upstream and downstream case. The cumulative density function describes the accumulated percentage of failed devices. Up-stream case shows much better EM performance than downstream case. The sample size is 30/29 for upstream/downstream case. MTF $=$ 193.8 h, $\sigma = 0.3$ for upstream, MTF $=$ 24.6 h, $\sigma = 0.74$ for downstream. The samples chosen for physical failure analysis were indicated.

III. RESULTS AND DISCUSSION

A. Stress Current Direction and Failure Mode

The current direction of EM test was found to have a strong effect on EM result. In addition, different dual-damascene process approach and EM structure will lead to different EM behavior. In our study, the wide-line structure with single via was used to eliminate the liner redundancy effect and to characterize the mass transport at the Cu/cap dielectric interface. Using this structure to evaluate the EM performance is the first time in the literature. The upstream stress showed much better EM lifetime than the downstream case in Fig. 2. Extensive failure analysis was carried out to explain the failure mechanism. Scanning electrom microscope (SEM) images at the different failure time points are shown in Fig. 3(a) and (b). Trench depletion failure mode was found in the upstream case, where a small volume of Cu depletion was observed for a short time-to-failure (TTF) point while a large volume of Cu depletion was correlated to a long TTF point. Unlike the previous work report [8], two failure modes were found in the upstream case. Assuming that a tapered via profile and good liner coverage were obtained, a large volume compared with the vertical via of Cu must be depleted. In this case, a good liner coverage suppresses Cu diffusion and the via depletion is alleviated for the upstream case. However, for the downstream case in Fig. 3(b), two failure modes corresponding to voiding in the via/metal interface and trench depletion were found.

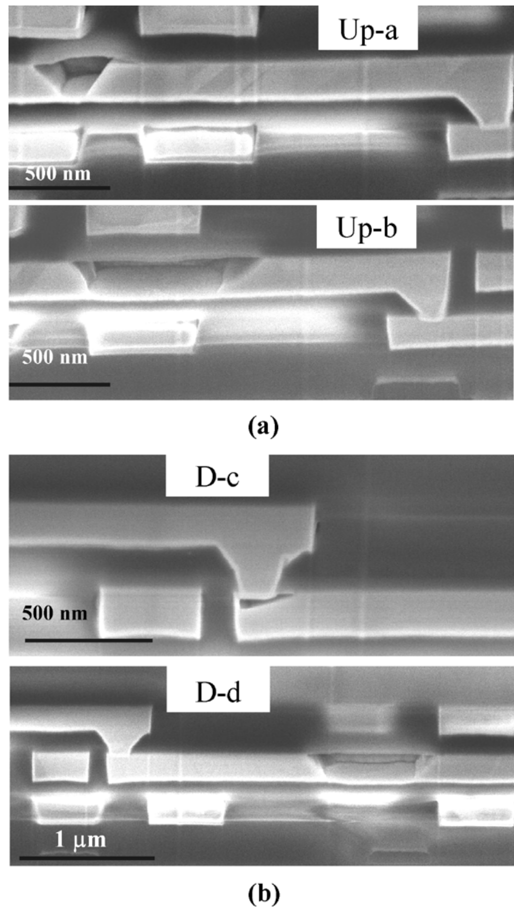
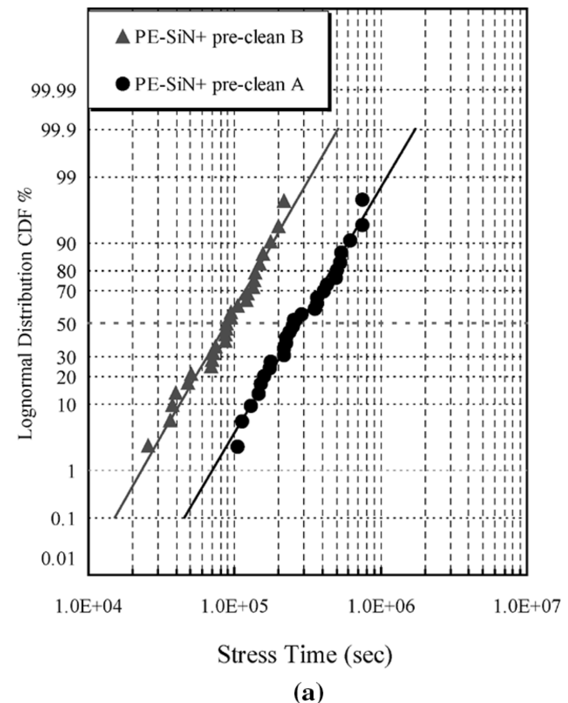


Fig. 3. (a) In upstream stress case. SEM images show trench depletion. Up-a and Up-b are different TTF indicated in Fig. 2. (b) In downstream stress case. SEM images show void in via/metal interface and trench depletion. D-c and D-d are different TTF indicated in Fig. 2.

Via depletion was related to a short TTF and even much shorter compared with the upstream case. A small volume of Cu depletion around the via/metal interface can cause a large resistance change, and it requires much shorter time to form via depletion than trench depletion. For the trench depletion mode in the down stream case, the TTF and the volume of Cu depletion were very close to the upstream case. Both stress directions indicated that Cu diffusion velocity was almost the same for identical trench depletion condition. Another failure mode of via depletion was noticed in the downstream stress. The downstream case with a wide line structure is a good approach to study, not only for evaluation of the worst case of Cu cap-layer interface but also for evaluation of process integration of via bottom interface.

B. Effect of Pretreatment on MTF

The Cu/cap dielectric interface is the dominant diffusion path in Cu damascene interconnects. The critical process leading to this specific interface property is known to be the preclean treatment prior to cap dielectric film deposition and cap layer materials. In this paper, two preclean recipes with different H content were used. Preclean A and reference process preclean B have different recipes according to the gas species



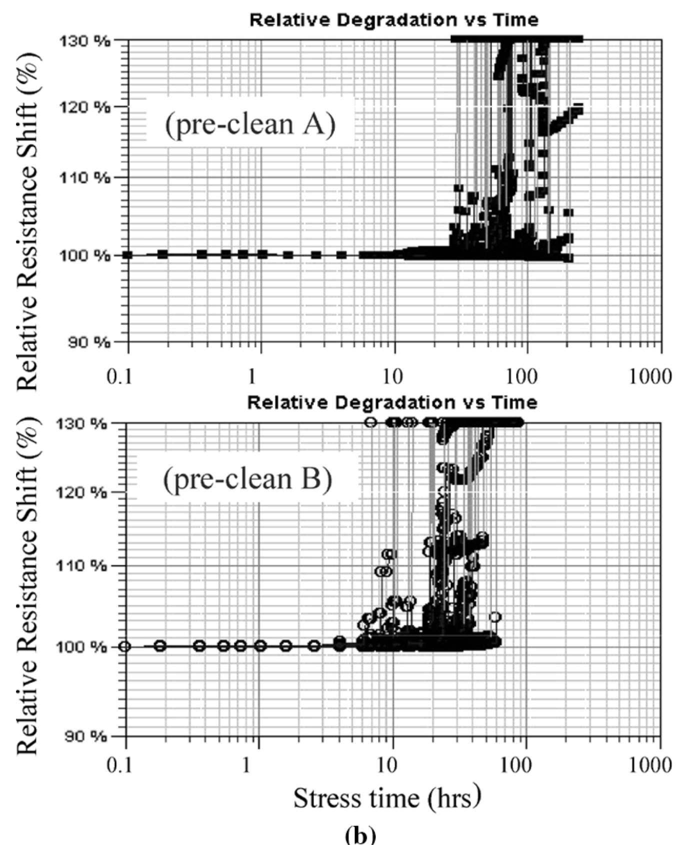


Fig. 4. (a) Lognormal time-to-failure distribution plots for PE-SiN+preclean A and PE-SiN+preclean B. The sample size is 27/28 for PE-SiN+preclean A/PE-SiN+preclean B. MTF = 77.8 h, σ = 0.58 for PE-SiN+preclean A, MTF = 24.4 h, σ = 0.56 for PE-SiN+preclean B. (b) Relative resistance degradation versus time plot for (upper) PE-SiN+preclean A. (down) PE-SiN+preclean B. The failure mode is almost same for both preclean recipes but the MTF is four times improvement for preclean A. Stress conditions are the same for both splits.

and gas flow. Fig. 4(a) shows the time-to-fail distribution of PE-SiN cap layer with preclean A and preclean B. By using

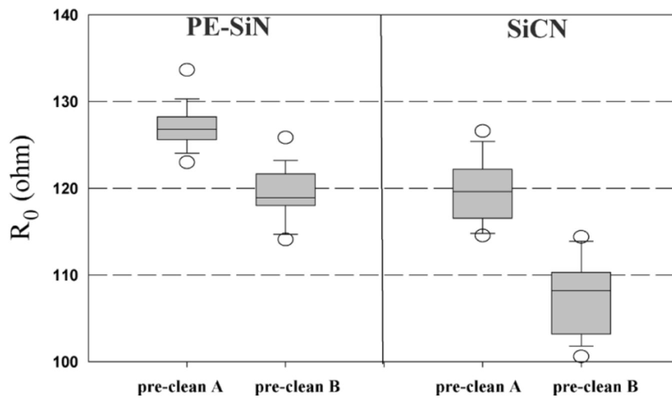


Fig. 5. Cu-wire initial resistance of PE-SiN and SiCN with preclean A or preclean B. The resistance of the Cu wire with the preclean A treatment is higher than that with the preclean B for both cap-layer materials. The sample size is 30 for initial resistance extraction. The circles are max and min points. The rectangular box is bounded by 75% and 25% points. The mean ± standard deviation of resistance (percent) is 127.1 ± 2.1%, 119.4 ± 2.6%, 119.6 ± 3.1%, and 107.5 ± 3.9% for PE-SiN+preclean A, PE-SiN+preclean B, SiCN+preclean A, and SiCN+preclean B, respectively.

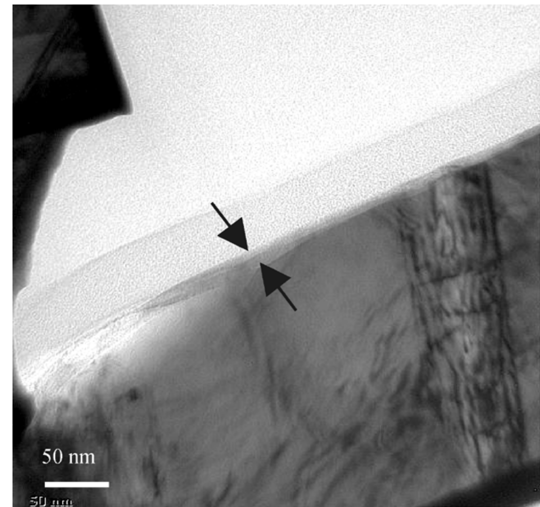


Fig. 6. High-magnification TEM image on Cu/Cap interface. Cu-siliside (Cu_xSi_y) formation between Cap/Cu interface is proposed to be an EM enhancement mechanism.

preclean A, we obtained significant improvement in EM lifetime and around four times increase of MTF. This result indicates that the Cu atom migration velocity at the interface after pretreatment H-rich preclean A is obviously slower than that of N-contained preclean B. In comparison to relative resistance degradation in Fig. 4(b), both cases display similar EM failure behavior. The distinct increase in MTF suggests that there should be an essential change taking place at the Cu/cap layer interface. Different initial resistances of Cu-wire for both pretreatment recipes were shown in Fig. 5. H-rich preclean A shows about 8% higher of initial resistance than that of N-contained preclean B with various cap-layer materials. High-magnification transmission electron microscope (TEM) analysis was carried out to reveal the interface image, as shown in Fig. 6. A very clear interlayer with darker contrast between Cu and cap dielectric layer is observed and its thickness is about 80 A. It demonstrates that the interlayer is a high-resistant compound formed on the H-rich treatment Cu surface as SiN deposition. The physical and electrical evidence is consistent with the previous study [9], suggesting that the interlayer should be Cu_xSi_y. The Cu-silicide (Cu_xSi_y) acts as the metallic cap layer [3], which will reduce the mass transport at Cu/cap interface. The intermetallic compound capped on the top surface of Cu wires provides a more cohesive interface between cap-layer, and it reduces the Cu migration effectively. The reason is thought to be the changes of interface bond strength, and reduction of mobility of Cu atoms is caused by pinning. Therefore, a reasonable mechanism for EM lifetime enhancement was proposed. After, Cu-oxide on the post-CMP surface is removed efficiently by the H-rich preclean A treatment, and then a "fresh" Cu surface is exposed. Consequently, Si-contained precursor gas reacts with the fresh Cu surface and forms a Cu_xSi_y thin-layer before the cap dielectric film deposition. The Cu-silicide formation schematic flow is summarized in Fig. 7(a). A Cu-silicide layer can provide a new interface with lower Cu migration rate than SiN/Cu interface and improve the Cu interconnect EM resistance. Moreover, it

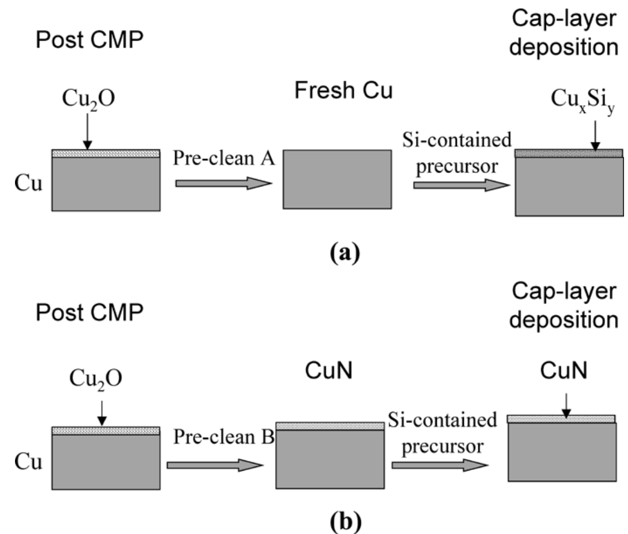


Fig. 7. (a) Schematic process flow of the Cu-silicide formation. (b) Schematic process flow of the Cu-nitridation reaction.

is proposed that N-rich preclean B will form a very thin nitrided layer [9]. The Cu-nitridation reaction flow is shown in Fig. 7(b). This nitridation layer will block the Si-contained precursor gas to form Cu-silicide and suppress the increase of Cu wire resistance, which is supported in Fig. 5. The velocity of Cu atoms diffusion along the surface under the preclean B treatment is speculated to be faster than that of preclean A due to the lack of a Cu-silicide layer. The MTF of preclean B is consequently shorter than that of preclean A.

C. *Effect of Cap-Layer Material on MTF*

Various cap-layer materials were used to examine the interface property. The EM lifetime performance of SiCN and PE-SiN with the same N-rich preclean B were compared in Fig. 8. The MTF of SiCN is two times longer than the PE-SiN cap dielectric layer, but the distribution of TTF is broader than PE-SiN. The activation energy extraction and adhesion of

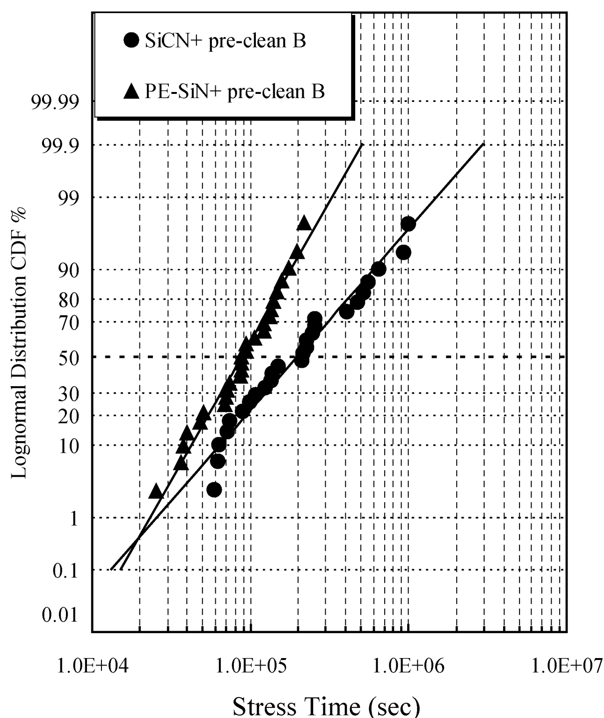


Fig. 8. Lognormal time-to-failure distribution plots for PE-SiN+preclean B and SiCN+preclean B. The sample size is 27/28 for PE-SiN+preclean B/SiCN+preclean B. MTF = 24.4 h, σ = 0.56 for PE-SiN+preclean B, MTF = 54.7 h, σ = 0.87 for SiCN+preclean B. Stress conditions are the same for both splits.

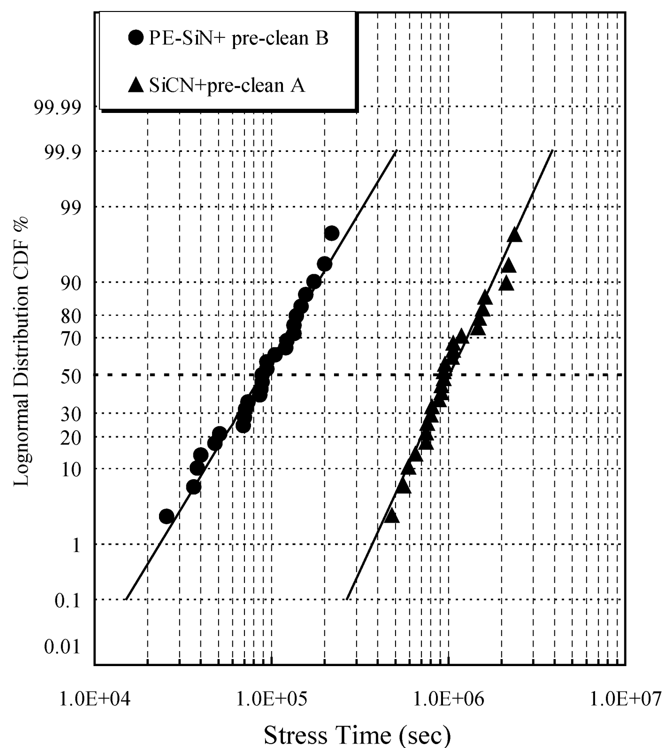


Fig. 9. Lognormal time-to-failure distribution plots for PE-SiN+preclean B and SiCN+preclean A, the sample size is 27/26 for PE-SiN+preclean B/SiCN+preclean A. MTF = 24.4 h, σ = 0.56 for PE-SiN+preclean B, MTF = 281.6 h, σ = 0.47 for SiCN+preclean A. Significant improvement of EM lifetime performance is achieved. Stress conditions are the same for both splits.

TABLE II
COMPARISON OF ADHESION AND ELECTROMIGRATION ACTIVATION ENERGY ON DIFFERENT CAP DIELECTRIC LAYERS. SiCN SHOWS BETTER ADHESION THAN PE-SiN FOR BOTH MEASUREMENT METHODS. SAMPLE SIZE IS 8 × 40 mm^2 FOR 4PB, 10 × 10 mm^2 FOR m-ELT, RESPECTIVELY

Cap-Material	PE-SiN	SiCN
m-ELT(MPa-m$^{1/2}$)*	**0.35 ± 0.03**	**0.41 ± 0.05**
4PB(J/m^2)*	**37.6 ± 3.6**	**44.9 ± 5.2**
Electromigration activation energy (eV)§	**0.79 ±0.14**	**1.13 ± 0.2**

*Standard deviation.

§Uncertainties to 90% CL by Maximum Likelihood estimation method.

cap-layer measurement were used to investigate the different interface property. Higher activation energy (Ea ~ 1.1 ± 0.2 eV) of samples with SiCN was obtained comparing to PE-SiN (Ea ~ 0.79 ± 0.14 eV). The uncertainties to 90% confidence levels were attained by a maximum-likelihood estimation method. The adhesion between the cap-layer and Cu was obtained through m-ELT and a four-point bending method. The result of the adhesion between SiCN and PE-SiN is shown in Table II. According to the result of both measurement methods, the strength of adhesion of SiCN is stronger than PE-SiN. The enhancement of the EM lifetime can be explained below. The adhesion of the Cu/cap interface can be directly correlated to electromigration MTF and activation energy [1]. The strength of adhesion would affect the void nucleation and growth rate induced by EM effect. Therefore, better adhesion between the cap-layer and Cu will suppress the Cu mass transporting through the cap interface. Higher activation energy also indicates that Cu atoms diffuse along the interface between Cu and SiCN is slow. The EM of SiCN is thus reduced due to better adhesion and higher activation energy than PE-SiN. In conclusion, preclean A shows longer MTF than preclean B under the same cap dielectric layer condition. In addition, SiCN shows better EM performance than PE-SiN on the same pretreatment. Finally, the SiCN with H-rich preclean A treatment, a ten times longer MTF and tight failure time distribution were attained. Fig. 9 shows the discrepancy between SiCN with H-rich preclean A and PE-SiN N-rich preclean B. A significant improvement of EM performance is achieved.

D. *Effect of Geometrical-Layout on MTF*

Geometrical layout design is a simple approach to increase the resistance of EM. The wide lines were designed as single or dual via where the line end extension is optional. Wide line with dual via is expected to get longer EM lifetime than single via. The relative resistance versus time plot shows instantaneous change for single via, but two modes found (i.e., most samples are long-lasting but few are of instantaneous change) for dual via shown in Fig. 10(a). The failure analysis shows via bottom depletion will induce instantaneous change. Dual via structure with a redundancy via can support the current when

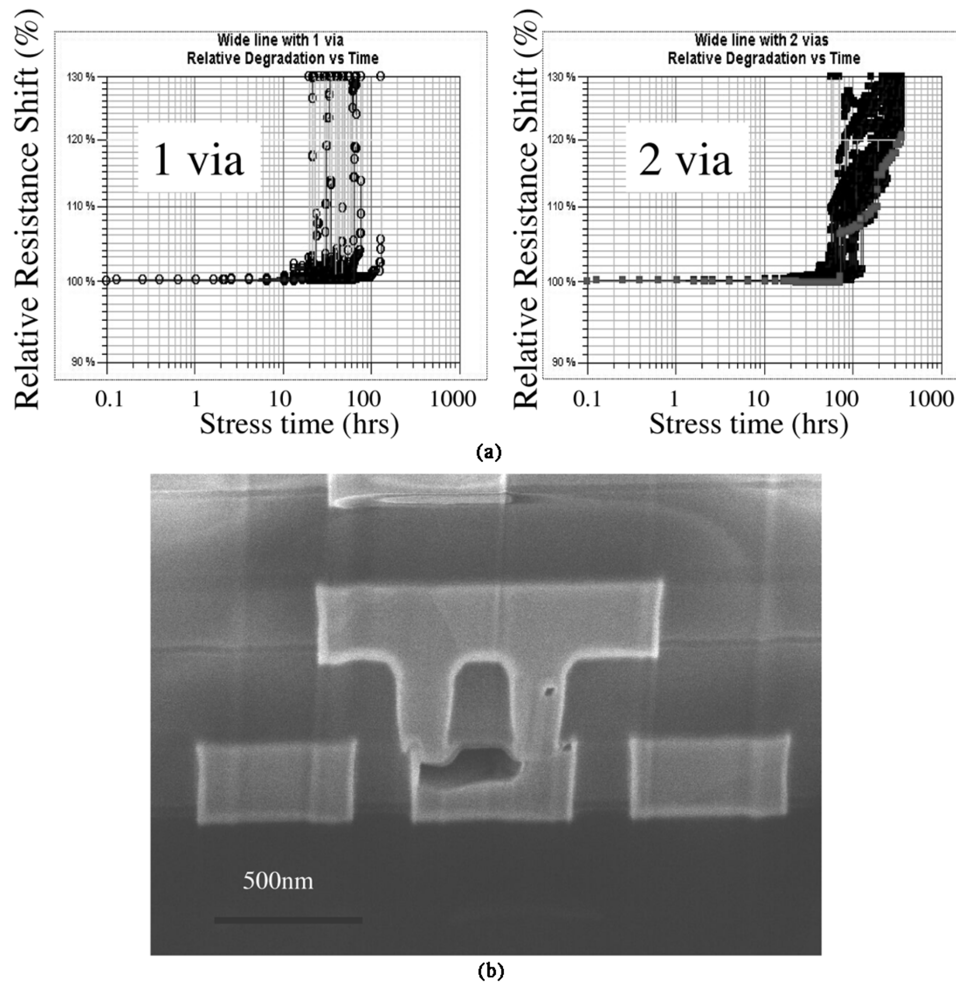


Fig. 10. Relative resistance degradation versus time plot for (a) wide line with single via (left) and wide line with dual vias (right). (b) SEM image for dual vias wide line structure. Void was found in one via bottom. The other serves a current path.

Cu under one via bottom was depleted in Fig. 10(b). It causes long-lasting resistance change. In comparison with one via the dual via structure not only extends MTF around three times but also reduces half value of deviation in time-to-fail. More than ten times EM lifetime enhancement was obtained. Furthermore, the major failure mechanism was found to change from instantaneous to long-lasting mode. The line-end extension will cause different trends on narrow or wide lines [10]. For line width equal to via diameter, line end extension may not change the redundancy effect since via liner always connects both sides of the line's wall liners. The line end extension will increase the EM lifetime since extra Cu in line end is like reservoir and could provide more Cu to diffuse away. But for wide line with single via without line end extension, via liner will connect trench liner, which serves as a current path when the void is in nucleation and growth under via bottom. It is expected that zero line end extension will get a better EM lifetime performance; however, no obvious improvement in EM lifetime was observed in Fig. 11. From two aspects we can explain it, one is that the interface diffusion is dominant factor than liner connection; the other is that some early fail samples were found in structure without line end extension due to the process variation.

IV. Conclusion

In conclusion, current direction of EM test has a strong effect on EM result. Trench depletion was a major failure mode for upstream case. However, for the downstream case, two failure modes corresponding to voiding in the via/metal interface and trench depletion were found. The effects of preclean and cap-layer material on MTF are significant. The SiCN+preclean A can improve lifetime by 10× relative to a PESiN+preclean B process. The adhesion of the Cu/cap interface can be directly correlated to electromigration MTF and activation energy. The Cu-silicide formation mechanism before cap-layer deposition was proposed to explain the enhancement of the EM lifetime. The critical process that leads to this specific interface property is known to be the preclean treatment prior to cap dielectric film deposition and cap layer materials deposition. Therefore, researchers have primarily chosen to optimize the EM performance in Cu interconnect systems through the modification of Cu/dielectric interfaces. Besides, geometrical layout design is a simple way to increase the resistance of EM. The dual via structure not only extends the EM lifetime but also changes the major failure mechanism from instantaneous to long-lasting mode.

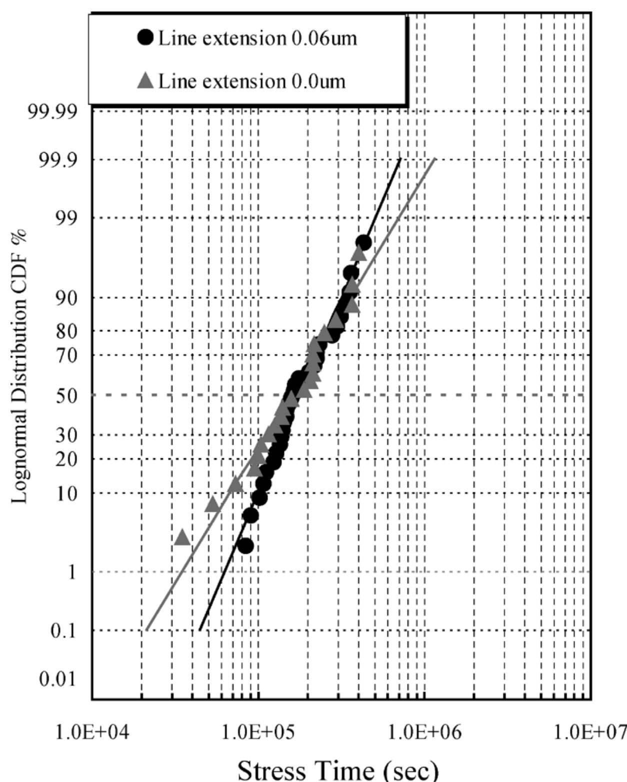


Fig. 11. Lognormal time-to-failure distribution plots for single via fully landed on wide-line with line end extension 0.06 μm versus 0.0 μm. Stress conditions are the same for both cases.

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