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Pentacene-based thin film transistors used to drive a twist-nematic liquid crystal display

Yu-Wu Wang [a,b,*], Horng-Long Cheng [b,1], Yi-Kai Wang [b], Tang-Hsiang Hu [b], Jia-Chong Ho [b], Cheng-Chung Lee [b], Tan-Fu Lei [a], Ching-Fa Yeh [a]

[a] *Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan 310, ROC*
[b] *Electronics Research and Service Organization, Industrial Technology Research Institute, Hsinchu, Taiwan 310, ROC*

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Abstract

The study addresses the factors of influence on the active matrix display that is driven by pentacene-based organic thin-film transistors (TFTs). The atmosphere and humidity conditions were found to seriously affect the performance of organic TFTs. An appropriate encapsulation layer was added to protect the organic TFTs from external damage. Organic TFTs reliability, the illumination effect and device uniformity, were also considered in the context of display application. Finally, a monochrome 3 inch 64×128 active-matrix twist-nematic liquid crystal display (LCD) was fabricated. The display is capable of showing video images with a refresh rate of 20 Hz. Obtained results reveal the potential of organic TFTs for active-matrix LCD technology.

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Keywords: Organic semiconductors; Electronic devices; Electrical properties and measurements

1. Introduction

Organic thin film transistors (OTFTs) have attracted much attention over the last decade. They can be used in a wide range of electronic devices such as displays, radio frequency identification tags [1], smart cards, microelectronics [2–6] or sensors [7]. Among various organic semiconductors, pentacene, a fused ring polycyclic aromatic hydrocarbon, has exhibited a high field-effect mobility of above 1.0 cm^2/Vs and is considered to be the preferred candidate for replacing amorphous silicon thin film transistors (TFTs) [8–11]. Pentacene, a small-molecule organic compound, can be processed by thermal evaporation or vapor deposition. Other organic semiconductors, the long chain polymers, such as regioregular poly(3-hexylthiophene) [12–14] and poly(9,9′-dioctyfluorene-*co*-2,2′-bi-thiophene) [15,16], have less favorable characteristics as compared to pentacene. However, the latter can be fabricated in solution processes, such as spin coating, ink-jet printing [17] or contact printing. Consequently, long chain polymers can be fabricated at lower cost by utilizing a roll-to-roll process — resulting in expenditures equal to 10% of the cost of fabricating traditional TFTs. OTFTs can be fabricated at low temperature and are highly compatible with a flexible/plastic substrate. Inherent features of OTFTs make the technology a promising candidate for the next generation of TFTs.

In active-matrix liquid crystal displays (AMLCDs), for instance, OTFTs allow the use of inexpensive, lightweight mechanically rugged plastic substrates as an alternative to glass. Prototype AMLCDs with all pixels driven by pentacene transistors [18] have recently been demonstrated. A polymer pixel engine has also been developed [19,20],

* Corresponding author. Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan 310, ROC. Tel.: +886 3 5914348; fax: +886 3 5826842.
E-mail address: newman@itri.org.tw (Y.-W. Wang).
[1] Present address: Institute of Electro-Optical Science and Engineering, National Cheng Kung University, Tainan 701, Taiwan.

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indicating the potential for application of organic transistor technology in displays. However, high operating voltage and photosensitivity of OTFTs restrict their use in regular display types. Thus, research on the application of OTFTs to drive AMLCDs, focuses on reflective displays, such as the polymer dispersed liquid crystal or electronic-ink displays [21]. These types of displays are suitable for operation at a high voltage.

This work studies the factors affecting the driving of a twist-nematic liquid crystal (TNLC) with a backlight system by pentacene transistors. Electronic stability of pentacene transistors is always a significant factor of consideration, regardless of application. The study of environmental factors, including moisture and illumination sensitivity of pentacene transistors is presented below. An extra passivation layer was added on to the pentacene transistors to isolate them from the atmosphere and prevent damage from the subsequent TNLC process. The gate bias stress and device uniformity were also studied. A 3 inch transparent active matrix TNLC display with 64×128 pixels was fabricated. The display is capable of displaying a black and white image with a contrast ratio similar to that of a paper. Furthermore, it can easily be fabricated into a color display through application of color filters.

2. Experimental details

This study employs the standard inverted-coplanar thin-film transistor structure with a bottom-contact configuration: the organic semiconductor is deposited onto the gate insulator, the prefabricated source and the drain electrodes. A finger-shaped source/drain electrode structure was adapted for testing devices. Following is the description of the process. First, an indium tin oxide (ITO) layer of thickness 1500 Å was sputtered and patterned by photolithography as the gate electrode on a glass substrate. Then, a silicon dioxide layer of thickness 3000 Å was prepared by plasma-enhanced chemical vapor deposition at 106.6 Pa and 380 °C. The gases He, O_2 and tetraethylorthosilicate (TEOS) were used with the following respective breakdown of gas quantity: 100, 3500, and 175 sccm. The silicon dioxide layer served as the gate dielectric and the breakdown electrical field was near 4 MV/cm. Then, the source/drain electrodes, also associated with a sputtered ITO layer of thickness 1500 Å, were deposited and patterned. Finally, pentacene, purchased from FULKA Chemical (97^{+}%), was thermally evaporated and transformed into a 1500 Å thickness layer through a shadow mask, to form the active region. The evaporation rate was maintained at 0.5 Å/s and the substrate temperature was fixed at 70 °C at a pressure of 5×10^{-5} Pa.

Throughout the TNLC process, the OTFTs array (backplane) was processed according to the technological process described above. Then, a water-based encapsulation poly (vinyl alcohol) (PVA) layer of thickness 6000 Å was spin coated on it. A spin-coated and rubbed polyimide (PI) layer of thickness 1000 Å was formed to align the TNLC. The two layers also serve as the passivation layer comprising the bottom plate. The top plate was formed by fabricating a sputtered ITO layer of thickness 1500 Å as the common electrodes with the addition of a spin-coated, rubbed polyimide alignment layer of thickness 1000 Å on a glass substrate. Finally, the two plates were assembled by a full sealing of the TNLC at 150 °C.

All the electrical characteristics were measured using a Hewlett-Packard 4155A Semiconductor Parameters Analyzer and a Keithley Model 237 High-Voltage Source-Measure Unit. The basic electrical characteristics and direct current (dc) stress were measured in normal air, in dry air and in a high vacuum.

3. Results and discussion

3.1. Sensitivity to humidity

Fig. 1 plots the influence of the measuring environment on the device performance of pentacene transistors with the bottom-contact configuration. In this bottom-contact device, the pentacene was deposited onto the gate insulator, the prefabricated ITO source/drain electrodes. In ambient air, the device performed poorly with a field-effect mobility (μ) of only 0.018 cm^2/Vs, a threshold voltage (V_t) of -3.3 V, an on/off ratio of order 10^4 and a subthreshold slope (SS) of 5.4 V/decade. The electrical parameters were extracted by applying standard metal-oxide-semiconductor field-effect transistor (MOSFET) equations, which are described in an earlier work [22]. As a next step, the characteristics of the device were measured after it had been stored in dry air for 25 h. The device exhibited better performance with a μ of 0.026 cm^2/Vs, a V_t of -3.3 V, an on/off ratio of 10^6 and an SS of 3.9 V/decade. The performance indicators were

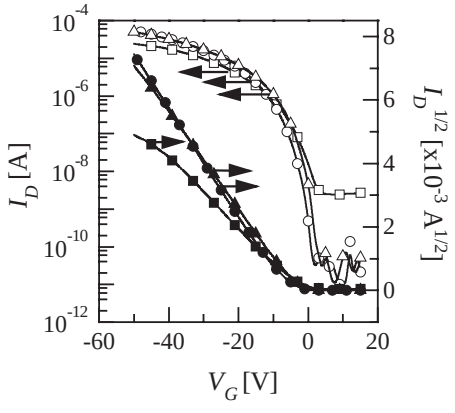

Fig. 1. Log $(I_D) - V_G$ (left axis, open symbols) and $(I_D)^{1/2} - V_G$ (right axis, closed symbols) characteristics of a pentacene transistor measured in air (squares), in vacuum (circles), and in dry air after 25 h of pre-test storage (triangles) with a V_{DS} of -50 V. The channel width and length are 20000 and 57 μm, respectively.

similar to those of the device measured under vacuum conditions, to be more specific a μ of 0.030 cm^2/Vs, a V_t of −6.4 V, an on/off ratio of 10^6 and an SS of 3.2 V/decade. Clearly, we can conclude that the pentacene transistors suffered from humidity/H_2O and consequently exhibited inferior performance due to the moisture that diffuses into the pentacene grain boundaries acting like a trap center and limiting carrier transport. Similar phenomena were observed in another investigation in which a top-contact configuration with Au source/drain electrodes was used [22,23].

3.2. Effect of passivation layer

In the standard manufacturing of AMLCDs, the liquid crystal is built on top of the TFTs. The practical experience showed that pentacene transistors failed when the liquid crystal solution was deposited onto it. Moreover, the pentacene molecule could not dissolve in common organic solvent. However, the solvent may change the pentacene grain state and grain boundaries state, modifying the device characteristics. Accordingly, when pentacene transistors were integrated into an AMLCD panel, an appropriate passivation layer was required to prevent damage caused by the subsequent liquid crystal process and the humidity of the ambient air. A passivation layer was deposited onto the device to ensure that the pentacene transistors work properly under liquid crystal; see the "Experimental" section for detailed description of the process. Fig. 2 plots the output curves of the pentacene transistors with and without a passivation layer, measured in ambient air. Obviously, the PVA/PI passivation layer prevent the device from moisture in air, thus the device shows the larger output current. After liquid crystal process, the protected pentacene transistors still

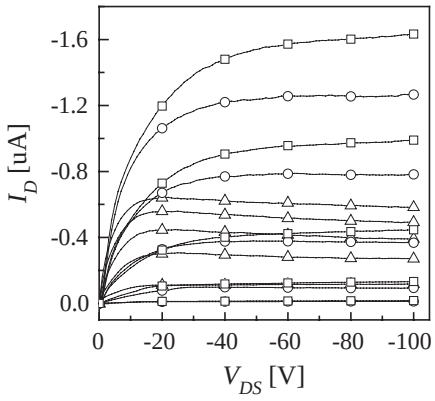

Fig. 2. Measured output characteristics of a pentacene transistor. The triangle symbols indicate the bare device without any passivation layer. The circles indicate the same device with the PVA/PI passivation layer upon it. The square symbols show the same device with the PVA/PI passivation layer after the full cycle of liquid crystal processing. The curves correspond to five different gate-source biases, from −20 to −100 V, in increments of −20 V. The measurements were performed in ambient air condition. The featured device had a channel width and length of 500 and 50 μm, respectively.

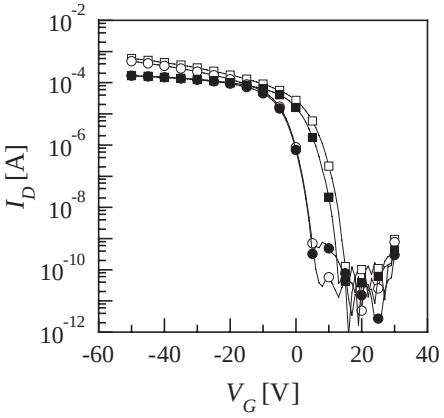

Fig. 3. Transfer characteristics of a pentacene transistor under illumination (squares) and without illumination (circles). The curves correspond to two different V_{DS} of −10 V (closed symbols) and −50 V (open symbols), respectively. The measurements were performed in vacuum. The featured device had a channel width and length of 20 000 and 57 μm, respectively.

worked fine and performed more output on-current. The relatively high on-current may be explained by the better moisture resistance of liquid crystal layer upon the PVA/PI passivation layer. However, these points need more detail studies in the future. The results clearly revealed that the passivation layer prevented the diffusion of moisture/H_2O, and the damage of liquid crystal solution.

3.3. Effect of illumination

Most organic semiconductor molecules are very photosensitive, resulting in marked leakage current in AMLCDs due to high backlight intensity. Therefore, electrical characteristics of pentacene transistors were measured in the dark and under illumination in a vacuum chamber, as plotted in Fig. 3. The device was operated in the linear region and in the saturation region with drain-to-source voltages (V_{DS}) of −10 and −50 V, respectively. Under illumination, the extracted field-effect mobility and the modulated on/off ratio were very close to the values obtained in the dark. However, the threshold voltage of −3 V obtained in the dark shifted to a positive 14 V under illumination. Such a shift in the threshold voltage under illumination was also observed in other OTFTs [24,25]. An almost unchanged on/off ratio of TFT was very important to the operation of active-matrix TNLC displays with backlight illumination, guaranteeing that the turn on/off states of each single pixel were clearly defined without disturbance or error. However, the shift of threshold voltage due to illumination had to be compensated by modulating the gate scan signal voltage, increasing the complexity of the driving system.

3.4. Gate bias stress

Fig. 4 plots the drain current (I_D) as a function of time under gate bias stress in ambient air and in vacuum. The

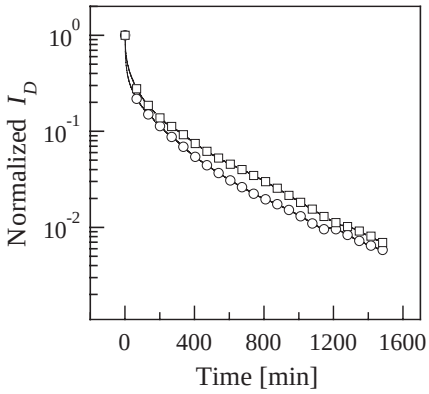

Fig. 4. The normalized drain current as a function of time of pentacene transistors stressed at V_G of −50 V and V_{DS} of −50 V in vacuum (squares) and in ambient air (circles).

gate voltage and drain voltage were set to the same value of −50 V. The dependence of the drain current in ambient air on time is similar to that in vacuum but displays more rapid decay. Other studies [26,27] revealed that the decay of the on-current could be attributed to the trapping of charges in the gate oxide and the oxide/pentacene interface. The trapped charges generate a built-in voltage that would result in negative inclination of threshold voltage of OTFTs. Hence, for a given dc stress, the actual bias, $(V_G - V_t)$, which forms the conducting channel gradually becomes smaller, leading to on-current decay. This procedure was found to be reversible. By supporting a suitable positive gate voltage for a short period or by supporting an unbiased state for a long period, trapped carriers can be neutralized or self-recombined. Thus, pentacene transistors are able to recover their initial state. The on-current decay is strongly correlated with the number of initial possible traps and defect states in the pentacene layer. The trap density in vacuum was lower than that measured in ambient air, thus explaining longer lifetime [22].

In some cases, after going through a dc stress, the pentacene transistors never recovered. The dc stress bias may be too intense to cause the gate insulator to undergo hard breakdown. Another well-known cause of the drop in lifetime, the hot carrier effect, which is evident in most MOSFETs, did not occur in OTFTs, because of low field effect mobility and small electron momentum.

3.5. Uniformity test

The uniformity of OTFTs is important for display applications. Fig. 5 shows the pentacene transistors uniformly distributed in a 3 inch OTFTs array substrate. The on-current of the pentacene transistors was in the order of 10^{-6} A at a V_G and a V_{DS} of −25 and −20 V, respectively. The leakage current was in the order of 10^{-11} A at a V_G and a V_{DS} of −5 and −20 V, respectively. Hence, the modulated on/off ratio of each device was approximately of the order of 10^5. The threshold voltage was around −4 V, with a variation of ±1 V. This variation of threshold voltage and the modulated on/off ratio appears as the result of the distribution of non-uniform pentacene grains and unintentional doping [28]. The OTFTs act as a switch to ensure that the external signal passes directly to the liquid crystal terminal to drive the TNLC display. Accordingly, the variation in the threshold voltage insignificantly influences the operation of the display and can be easily compensated by modulating the driving signal.

3.6. Application of active-matrix TNLC display

Fig. 6(a) presents an equivalent pixel structure, including an OTFT with an equivalent capacitance of C_{Pixel} (which combines an additional assistance storage capacitance C_S and a liquid crystal parasitic capacitance C_{LC}). Fig. 6(b) presents a microscopic image of the layout of a single pixel and Fig. 6(c) presents a cross-section view of the AMLCD. Each pixel was addressed once and its written state is retained for the interval of a frame. The driving scheme is briefly described below. The rows were triggered consecutively by applying high negative pulse voltage that maintained a scan line selection period (screen refresh time (T_{frame})/number of horizontal scan lines (N_{row})). The given scan signal turned on the switch OTFTs in the pixels of the same row, at the same time the data signals were simultaneously written into individual pixels. The data signal was stored in the storage capacitor to modulate the TNLC state for one frame interval until the next writing.

The most important OTFT criterion for the operation of the display was to ensure that the proposed on-current (I_{on}) could charge up the pixel capacitor in a limited selection row time. Another condition was that the data signal stored in the capacitor would not decay via the OTFT leakage path in the remaining frame interval. The criteria are specified in terms of the display resolution, the frame rate, the operating

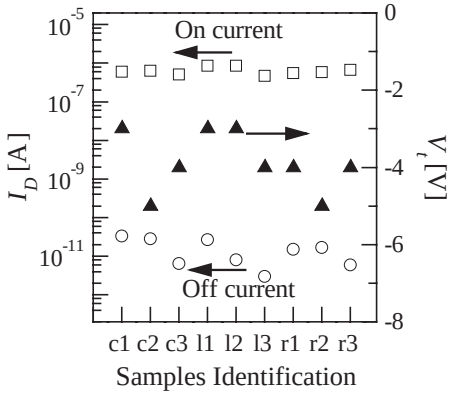

Fig. 5. On current, off current, and threshold voltage of nine pentacene transistors distributed in a 3 inch OTFTs array.

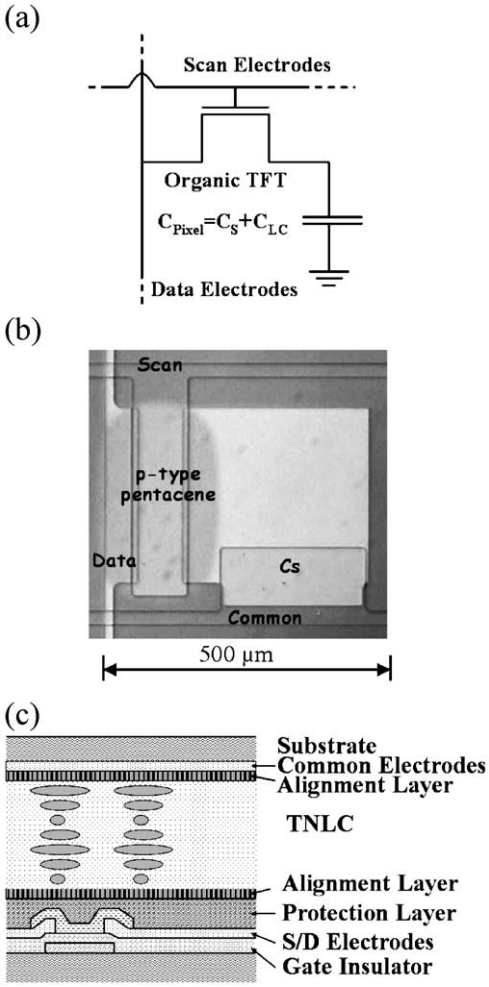

Fig. 6. (a) Equivalent pixel structure, including one transistor, one storage capacitor C_S and an additional assisting liquid crystal parasitic capacitor C_{LC}. The reference is made to the C_s on common pixel structure. (b) Microscopic view. (c) Cross section of pixel.

voltage and the storage capacitance, according to the following equation.

$$I_{on} \geq \frac{6C_{pixel}V_{on}N_{row}}{T_{frame}} \quad (1)$$

$$I_{off} \leq \frac{C_{pixel}V_{on}}{N_{gray}MT_{frame}} \quad (2)$$

$$\frac{I_{on}}{I_{off}} \geq 6MN_{row}N_{gray} \quad (3)$$

where I_{on} is the required minimum on-current; I_{off} is the required maximum leakage current; N_{gray} is the number of gray levels; M is the empirical safety margin coefficient, and V_{on} is the maximum data signal voltage [29]. Eqs. (1) and (2) yield the required minimum on-current and the maximum off-current of OTFTs, respectively. Accordingly, Eq. (3) specifies the required modulated on/off ratio of OTFTs.

A 3 inch active-matrix TNLC display with a 64×128 resolution, and a pixel size of 500×500 μm was fabricated. In the display, the total pixel capacitance was set to 1.4 pF; T_{frame} was equal to 16 ms (frame rate 60 Hz); the scan signal pulse swing ranged between 0 V to −40 V; the data signal rang fell between 5 and −20 V, the safety margin coefficient M was 3; N_{gray} was 16 steps; the required minimum on-current should have exceeded 0.68 μA, and the required maximum leakage current had to be less than 36.7 pA. If N_{gray} was increased to 256 steps, then the leakage current of each pentacene transistor should be less than 2.29 pA for a given pixel structure. Based on the above calculations, the process design rule and the obtained device mobility of 0.014 cm^2/Vs, the driving pentacene transistors in this display were designed with a channel length and a channel width of 70 and 320 μm, respectively. The storage capacitance was designed to be 1.4 pF, and the parasitic C_{LC} was calculated to be less than 0.01 pF, to meet the requirements. The final aperture ratio of this display was equal to 38.4%.

Fig. 7 plots the voltage–transmittance curve of a single TNLC cell. The transmittance ranged from 35% at 1.5 V to almost 0% at 3 V. Falling out of the range, the TNLC was either in the transparent state (<1.5 V) or in the dark state (>3 V). The two states determined the contrast ratio of the display. In fact, the pentacene transistors in the pixels were over-designed with a high width/length ratio. The given data signal (5 to −20 V) was also magnified out of the TNLC display modulation range. The two preventive measurements were made to suppress the signal loss caused by the parasitic effect to ensure that the on-current sufficient enough to charge up the storage capacitor. The display demonstrated a black and white video image with a refresh rate of 20 Hz. It performed with a contrast ratio characteristic for normal paper and a brightness of 30 nits.

Numerous factors influenced the final performance of the display. For example, the TNLC display cell gap strongly affected the display uniformity. The contrast ratio

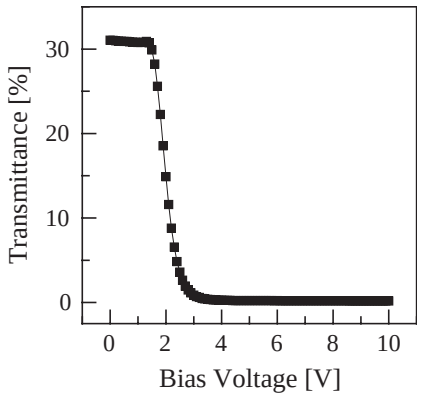

Fig. 7. Voltage-transmitting curve of TNLC.

was determined by the pixel aperture ratio, the black matrix area, the TNLC transmittance, the polarizer absorption as well as other factors. The OTFTs variation seemed to not affect the display considerably. However, the OTFTs variation needed to be further suppressed to improve the display performance. For instance, the OTFTs threshold voltage variation of ±1 V yields an almost 5% difference in the charging on-current. Perhaps in response to the charging of the storage capacitor, leading to the variation of TNLC transmittance, the error would be enlarged if the display has a high resolution and small gray level step. Although the display performance still has much room for improvement, the OTFTs driving TNLC display was successfully produced.

4. Conclusion

A 3 inch 64×128 active-matrix TNLC display with pentacene transistors was fabricated and demonstrated. The electronic stability of pentacene transistors was studied in various environments. It was noted that the pentacene transistors were sensitive to humidity/H_2O and easily failed in organic solvent during the subsequent liquid crystal process. A passivation bilayer consisting of PVA and PI needs to be deposited on the top of the device to overcome issues related to the integration of a pentacene device into an active-matrix TNLC display. The photosensitivity characteristics of pentacene transistors were also investigated. The findings revealed that the pentacene transistors can drive a normal active-matrix TNLC display with a backlight system. However, application of an additional light shield layer is recommended. The gate bias stress proved to accelerate the on-current decay of the pentacene transistors. Fortunately, the decay is reversible. The reliability and uniformity of pentacene transistors was investigated in relation to display applications. Although the display required adjustment, a high-resolution transparent AMLCD application was made possible. In this process, a rigid 0.7 mm glass substrate was adopted. It can later be easily transferred to flexible plastic substrates. In the future, color filters will be integrated with the display to render color images. Therefore the OTFT has the potential to play an important role in the future of display technology.

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