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Electrical properties of amorphous silicon films with different thicknesses in metal/insulator/semiconductor structures

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Abstract

The density of states (DOS) of hydrogenated amorphous silicon (a-Si:H) is an important issue in the study of the physics of amorphous semiconductors. In many earlier reports concerning the analysis of the field-effect conductance metal/insulator/a-Si:H structures, namely, thin-film transistors (TFTs), the potential at the semiconductor surface apart from the gate insulator/a-Si:H interface, i.e., the rear interface, was assumed to be zero. However, in principle, as the thickness of the semiconductor film is smaller than the theoretically expected width of the space charge region, this assumption no longer holds. Hence, it is necessary to reconsider the band-bending phenomena of the a-Si:H active layers. It was found that the DOS, which was extracted previously from the field-effect conductance of the TFTs based on the assumption of the zero-potential rear interface, was appropriate only for the thick a-Si:H films. As for the thin semiconductor films, the accurate DOS can be obtained by fitting the calculated field-effect conductance, with a surmised possible DOS, to the experimentally measured data via the method developed.

Keywords: Density of states (DOS); Field-effect conductance; Hydrogenated amorphous silicon (a-Si:H); Thin-film transistors (TFT)

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been widely studied because of their practical applications in liquid crystal displays (LCDs) [1]. The field-effect conductance measurement is the main technique used to analyze the electrical characteristics of the TFTs. In many earlier reports [2–9] concerning the analysis of the field-effect conductance of the TFTs, the potential at the semiconductor surface apart from the gate insulator/a-Si:H interface, i.e., the rear interface, was assumed to be zero as a boundary condition for the Poisson equation. Based on this assumption, it was derived that the electrical potential distribution in the a-Si:H shifts rigidly along the distance from the gate insulator/a-Si:H interface (the front interface) as the gate voltage varies. Then the effect of the density of states (DOS) on the conductance at a given gate voltage can be attributed to the DOS at the potential at the front interface with respect to the gate voltage. Thereby, the energy dependent DOS of the a-Si:H can be extracted from the experimentally measured field-effect conductance. However, if the width of the space charge region corresponding to the gate voltage is larger than the thickness of the semiconductor film of the TFTs, the assumption of the zero-potential rear interface and the rigidly shifting potential distribution along the distance become invalid.

A method to calculate the electrical potential distributions in the active layer, namely, the band-bending profiles, at different gate voltages is proposed to study

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the effects of the a-Si:H film thickness of the TFTs. The DOS in the a-Si:H is assumed to be spatially uniform and the same for films with different thicknesses, and the effects of the interface states and fixed charges are neglected in this paper. The results show that as the active layer of the TFTs is thinner than the required width of the space charge region, the band-bending profiles are greatly affected by the thickness of the semiconductor.

2. Model calculations

For the one-dimensional gate electrode/insulator/a-Si:H structure, the Poisson equation in the a-Si:H active layer can be written as

$$\frac{\mathrm{d}\phi(x)}{\mathrm{d}x} = -\xi(x) \tag{1}$$

$$\frac{\mathrm{d}\xi(x)}{\mathrm{d}x} = \frac{1}{\varepsilon_{\mathrm{Si}}}\left\{-q\left[\int_{E_v}^{E_c} N(E)(f(E-q\phi)-f(E))\,\mathrm{d}E + n_b(\exp(-q\phi/kT)-1) - p_b(\exp(-q\phi/kT)-1)\right]\right\} \tag{2}$$

where ϕ and ξ are the electrical potential and field in the semiconductor, respectively, x is the distance from the gate insulator/a-Si:H interface, q is the electron charge magnitude, $\varepsilon_{\mathrm{Si}}$ is the permittivity of the a-Si:H, E_c and E_v are the conduction and valence band mobility edges, respectively, $N(E)$ is the energy-dependent DOS and is assumed to be spatially uniform, f is the Fermi–Dirac occupation function, n_b and p_b are the densities of the mobile electrons and holes, respectively, k is Boltzmann's constant, and T is the absolute temperature. To determine the band-bending profile in the active layer, the a-Si:H film is divided into many super-thin slabs with a thickness of Δx. In each super-thin film, the electrical potential ϕ can be taken as a constant and the conductivity σ of the film is thus given by

$$\begin{aligned}\sigma &= q\mu_e\left\{\int_{E_c}^{\infty} N_C f(E)\,\mathrm{d}E\right\}\exp(-q\phi/kT) + q\mu_h\left\{\int_{-\infty}^{E_v} N_V[1-f(E)]\,\mathrm{d}E\right\}\exp(q\phi/kT)\\ &\cong q\mu_e N_C\{\exp[-(E_c-E_f+q\phi)/kT]\}kT + q\mu_h N_V\{\exp[(E_f-E_v+q\phi)/kT]\}kT\end{aligned} \tag{3}$$

where μ_e and μ_h are the electron and hole mobilities, respectively, N_C and N_V are the DOS at E_c and E_v, accordingly, and E_f is the Fermi energy.

Once the DOS distribution $N(E)$ is given, the static field-effect conductance-gate voltage characteristics of the TFTs can be obtained by the following procedure.

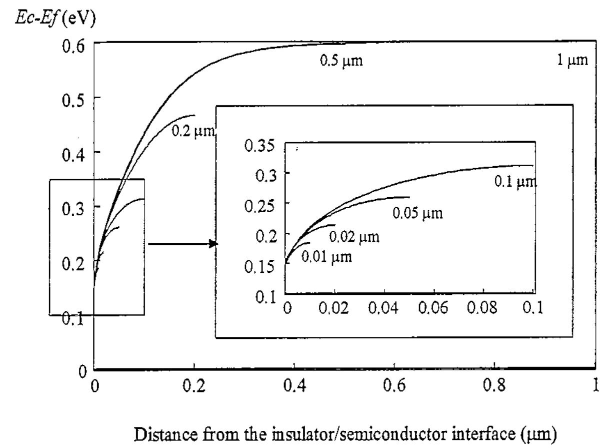

Fig. 1. Band-bending potential profiles for several semiconductor thicknesses in TFTs.

Assuming a zero electrical field and a potential ϕ' for the super-thin slab at the semiconductor surface apart from the gate insulator/a-Si:H interface, the sheet conductance of this film is $\sigma\Delta x$ and the potential in the super thin-slab next to this one is $\phi' - \xi\Delta x$, where the electrical field ξ is given by Eq. (2). By repeating the computation, the potentials of all the super-thin films, i.e., the band-bending profile along the active layer, can be determined. corresponding to this potential profile, the gate voltage V_G can be written as

$$V_G = -\frac{\varepsilon_{\mathrm{Si}}}{C_{\mathrm{ins}}}\xi_S + \phi_S \tag{4}$$

where C_{ins} is the gate insulator capacitance per unit area and η_S and ϕ_S are the electrical field and potential at the insulator/a-Si:H interface, respectively. Moreover, the conductance of the whole active layer is obtained by summing up the conductance of each super-thin film. Therefore, the gate voltage and the associating field effect conductance of the semiconductor can be obtained by assuming a potential ϕ'. Then, the field-effect mobility and the threshold voltage can be obtained from the slope and the intercept, respectively, of the curve of the gate voltage against field-effect conductance for various potentials ϕ'.

To verify the validity of the simulation, a-Si:H TFTs with inverted-staggered structures fabricated by successive plasma-enhanced chemical vapor deposition (PECVD) and necessary etching of the silicon nitride, a-Si:H, and n^+ a-Si:H on the chromium gate electrode were also tested to compare with the simulation results. The gate insulator capacitance per unit area, C_{ins}, of the a-Si:H TFTs is 30 nF cm^{-2} and the thickness of the active layer is 200 nm. In the simulation study, the energy gap is assumed to be 1.8 eV and E_f is chosen to be 1.2 eV above the valence band, according to Ref. [10]. $N(E)$ is assumed to have a linear tail states distribution near the conduction and valence bands with

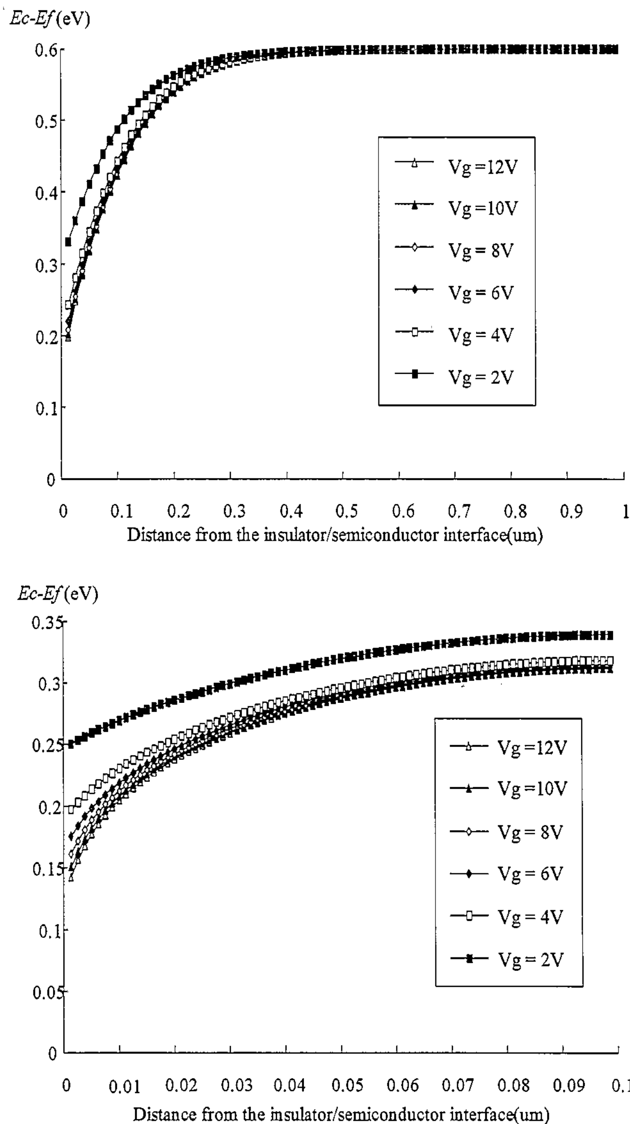

Fig. 2. Potential distributions under various gate bias voltages in the a-Si:H films with thicknesses of (a) 1 μm and (b) 0.1 μm.

widths of 0.07 and 0.05 eV, respectively, as well as a deep state density of 10^{17} cm^{-3} eV^{-1}. N_C and N_V are both set at 10^{21} cm^{-3} eV^{-1}. The band mobility of the electrons needed for the calculation of Eq. (3) is 10 cm^2 V s^{-1} [11], while the hole mobility is zero, since the n$^+$ source/drain regions will block the conduction of the holes. The surface DOS and the fixed charges at the interfaces of the passivation layer/active layer and the active layer/gate insulator are excluded in this study. By modifying the distribution of the DOS, the calculated curve of the field-effect conductance versus the gate voltage is altered to fit the experimental results. Furthermore, the activation energy of the field-effect conductance was also measured with respect to the gate voltage. It was in good agreement with the calculated separation of the Fermi level from the conduction band edge at the gate insulator/a-Si:H interface [10,12]. Therefore, the validity of this model is confirmed.

3. Results and discussion

The simulated band-bending profiles of the TFTs with various thicknesses of the semiconductor layer, biased at the same front interface potential of $E_C - E_f = 0.15$ eV, are shown in Fig. 1. It can be seen that the potential distributions in the active layers with thicknesses of 1 and 0.5 μm are indistinguishable and approaching the flat band condition near the rear interfaces. However, as illustrated in the inset of Fig. 1, for the TFTs with the a-Si:H films thinner than 0.5 μm, the potential profiles split near the rear interfaces and the potentials are no longer close to the Fermi level at the flat band where $E_c - E_f = 0.6$ eV. With the same gate bias, the departure of the rear interface potential from its flat band position increases as the thickness of the semiconductor film shrinks down.

These phenomena are attributed to the space charges which must be induced in the semiconductor layer by the gate bias. In a metal/insulator/semiconductor structure, the space charge region is formed as the gate voltage is applied. Assuming the thickness of the semiconductor film is infinite, the theoretical width of the space charge region corresponding to the surface potential is determined by the charges in the semiconductor and the states at the front interface. For the intrinsic a-Si:H film without interface states in this simulation, these space charges consist of the charges trapped by the states in the energy gap and the free carriers. If the thickness of the semiconductor is larger than the principal width of the space charge layer, the potential distributes as it does in the infinitely thick a-Si:H film, and the region near the rear interface will not be affected by the gate voltage, as shown in Fig. 2(a). The theoretical width of the space charge region, calculated with the $N(E)$ of the semiconductor in this study, is about 0.5 μm. As illustrated in Fig. 2(b), for the 0.1-μm-thick active layer, the Fermi level in the whole film is forced to move toward the conduction band. This thin layer cannot afford the required charges according to the applied positive gate voltage if the potential at the rear interface is to stay at its flat band position. Moreover, for an even thinner a-Si:H film, the Fermi level will be closer to the conduction band, because almost the same amount of charges, corresponding to the positive gate voltage, must be generated in less volume. This is an important feature of thin-film transistors. In the following context, 'thin' film and 'thick' film are used to describe the thicknesses of the films that are less and greater than the principal width of the space charge region, respectively.

In thick silicon films, the potential at the rear interface is never affected by the gate bias in the range of the applied voltages, and the potential profile shifts rigidly along the distance from the insulator/semiconductor interface as the potential at the front interface varies, as

shown in Fig. 1(a). Therefore, the variation of the conductance of the active layer can be attributed wholly to the change in the potential profile near the front interface. This is the basis of a commonly used technique to extract the DOS of the semiconductor from the field-effect conductance of thin-film transistors. However, the results of this study reveal that the assumption of the zero-potential rear interface is improper for thin semiconductor films. Therefore, the rigidly shifting behavior of the band bending is not observed in Fig. 2(b), for which the a-Si:H film is thinner than 0.5 μm. In Refs. [2–9], this analysis was applied to TFTs with thick semiconductor films. Thus, the increment of the field-effect conductance can be exclusively correlated to the states near the front interface at that particular energy, and the DOS can be extracted. However, for TFTs with thin semiconductor films, the change in the field-effect conductance results from the difference in the band-bending profiles, which cannot be ascribed to a sole energy. Consequently, using the methods presented in Refs. [2–9] to analyze the DOS might lead to incorrect conclusions. The accurate DOS in the thin active layer can be obtained by fitting the calculated field-effect conductance with a guessed possible DOS to the experimentally measured data via the proposed procedure.

The thickness effects of the semiconductor films discussed above can also happen in polycrystalline silicon and silicon-on-insulator (SOI) TFTs if the doping concentration and the DOS of the semiconductor are very low or the active layer is very thin.

4. Conclusions

The band-bending profiles of semiconductor films with different thicknesses in TFTs are calculated. It is found that there is a theoretical width of the space charge region for the metal/insulator/a-Si:H structure. If the thicknesses of the a-Si:H films are larger than this width, the potential distributes as it would in a film that is infinitely thick. On the other hand, if the semiconductor films are thinner than this width, the potential profiles are greatly affected by the gate bias. The effects of the amorphous-silicon film thickness must be considered in the analysis of the field-effect conductance of TFTs, especially when the active layer is very thin.

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