Process and Characteristics of Modified Schottky Barrier (MSB) p-Channel FinFETs

Bing-Yue Tsui, *Senior Member, IEEE,* and Chia-Pin Lin, *Student Member, IEEE*

***Abstract*—A novel modified Schottky barrier p-channel FinFET (MSB FinFET) has been successfully demonstrated previously. In this paper, the detailed process conditions, especially the formation of MSB junctions, has been presented. Device characteristics as well as the geometry effect are also discussed extensively. In the MSB FinFETs fabricated by the two-step silicidation and implant-to-silicide techniques (ITS), an ultrashort and defect-free source/drain extension (SDE) could be formed at a temperature as low as 600 °C, resulting in excellent electrical characteristics. The ultrashort SDE could effectively thin out the SB width between source/channel during on-state or broaden and elevate it between drain/channel during off-state. A leakage mechanism of MSB FinFETs similar to the conventional ones was identified by the activation energy analysis. Strong fin width dependence of the electrical characteristics was also found in the proposed devices. When the fin width becomes larger than the silicide grain size, the multigrain structure results in a rough front edge of the MSB junction, which in turn degrades the short-channel device performance. This result indicates that the MSB device is suitable for use as FinFET. The low thermal budget of the MSB FinFET relaxes the thermal stability issue for metal gate/high-κ dielectric integration. It is considered that the proposed MSB FinFET is a very promising nanodevice.**

***Index Terms*—FinFET, implant-to-silicide (ITS), Schottky barrier (SB), silicon-on-insulator (SOI).**

I. Introduction

THE first Schottky barrier MOSFET (SB-MOSFET) utilizing metal silicide to replace the heavily doped silicon within the source/drain (S/D) regions was proposed in 1968 [1]. Compared with conventional MOSFETs, SB MOSFETs had several advantages including easy processing, ultrashallow junction, low S/D series resistance, low thermal budget, and excellent short channel effect immunity. In 1983, the SB pMOS was proposed to eliminate the latch-up effect [2], [3]. However, the drawbacks of high drain leakage current attributed to the thermionic emission current and low driving capability due to the abnormally high SB height made it impractical [4], [5]. Subsequently, asymmetric Schottky MOSFET with SB source junction and p-n drain junction was shown to solve the leakage current issue [6]. However, the problem of low driving current was left unsolved. Furthermore, the asymmetric device is difficult to be scaled down.

Recently, nanoscaled SB-MOSFETs were proposed so that the driving capability could be improved by the gate-fringing field due to the short spacer length [7]. Nevertheless, previous problems still existed for those nanoscaled SB-MOSFETs. For example, the gate fringing field could not suppress the SB effectively, so that the on-state current (I_{on}) of SB-MOSFET was still lower than that of the conventional MOSFET. A method of reducing this barrier by using complementary silicide (PtSi for pMOS and ErSi for NMOS) on bulk or silicon-on-insulator (SOI) substrate has been suggested [7], [8]. However, the process to form complimentary silicide was more complex than that to form single silicide, and the abnormally high off-state leakage current (I_{off}) due to the thermionic injection and gate-induced drain leakage (GIDL)-like effect was still a problem [9]. Adding a metal fieldplate over the MOSFET was shown to be effective in reducing the off-state leakage current by suppressing the thermionic injection from the drain contact; nevertheless, it required an additional voltage supply and it sacrificed device density [10]. The SOI structure with fully silicided S/D and doped S/D extension (SDE) fabricated by a conventional process was also reported to have proper electrical characteristics [11]. It was basically a conventional MOSFET with identical thermal budget.

Recently, to overcome the drawbacks of SB-MOSFETs while keeping the advantages of low S/D external resistance and low temperature process, a new MSB p-channel FinFET with ultrashort SDE using an implant-to-silicide (ITS) process was proposed [12]. In the MSB FinFET structure, the gate wraps around the rectangular silicon fin from three sides, so that a significantly high driving current and excellent short channel effect could be achieved at the same feature size [13]. Furthermore, the proposed MSB device also showed significantly lower I_{off} than the conventional SB device because of the thick SB at the drain/body junction during off-state.

The key process developed in this work is a two-step annealing technique under 600 °C to control the silicidation process for the MSB FinFET. We also carried out a detailed study on the current–voltage (*I–V*) characteristics of the MSB FinFET with various fin thicknesses. Based on these results, the conduction mechanisms for on-state and off-state were proposed. The temperature effect was studied and the leakage current mechanism was analyzed. Finally, the uniformity dependence of SDE region related to the electrical characteristics, including drain-induced barrier lowing (DIBL) and subthreshold swing (SS) were also investigated. The advantage

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B.-Y. Tsui is with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C., and also with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. (e-mail: bytsui@mail.nctu.edu.tw).

C.-P. Lin is with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: cplin.ee90g@nctu.edu.tw).

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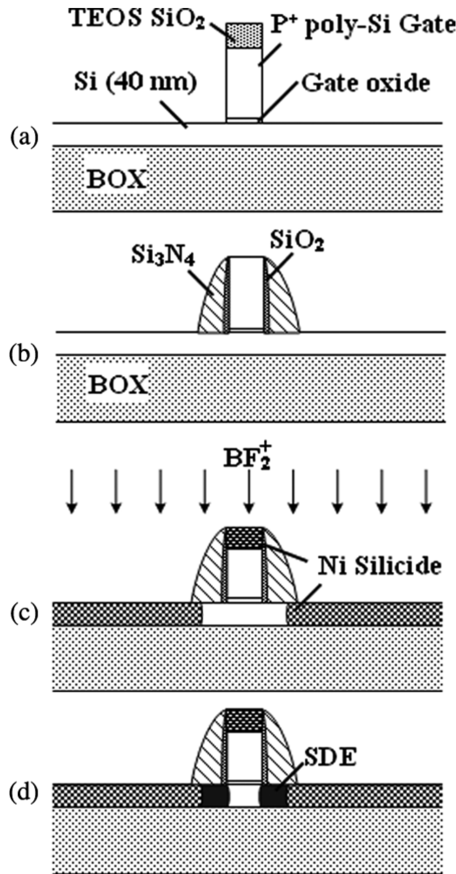

Fig. 1. Main process flow of the modified SB FinFET.

of low thermal budget to relax the thermal stability issue for metal gate/high-κ dielectric integration has been demonstrated.

II. Device Fabrication

Fig. 1 shows the main process steps of the MSB FinFET fabrication. The starting material was a boron-doped 6-in SOI wafer with a low doping concentration of around 1×10^{15} cm^{-3}. The nominal Si layer and buried oxide layer thicknesses were 50 and 150 nm, respectively. The Si layer was thinned down to 40 nm by thermal oxidation. The device islands (including S/D region and Si fins) were defined by electron-beam (e-beam) lithography and plasma etching. A 4-nm-thick SiO_2 was thermally grown as the gate dielectric. Since the gate oxide thickness on the top and sidewall of the Si fin are similar, the final device is a tri-gate FinFET. Poly-Si film of a 150-nm thickness was deposited and doped by BF_2^+ ion implantation at 40 KeV to a dose of 5×10^{15} cm^{-2}. After rapid thermal activation at 1025 °C for 10 s, a 50-nm-thick TEOS oxide was deposited in a low-pressure chemical vapor deposition system as hardmask. As shown in Fig. 1(a), e-beam lithography was employed again to define the gate pattern. Following a gate patterning, a SiO_2 (10 nm)/Si_3N_4 (30 nm) composite spacer was formed, as shown in Fig. 1(b). The hardmask on poly-Si was etched away during spacer etching. Self-aligned Nickel silicide (Ni-Salicide) process was then performed and the resulting structure is shown in Fig. 1(c). The sheet resistance of the silicide layer is about 10 $\Omega/\square$ as measured by a Van der Pauw structure. This silicidation process is the key process step for the MSB FinFET and is discussed extensively in the next section.

To modify the characteristics of the SB, BF_2^+ ions were implanted to silicide at 30 KeV to a dose of 3×10^{15} cm^{-2}, followed by a furnace annealing at 600 °C for 30 min. The silicide layer acts as a stop layer for the implanted ions and as a solid diffusion source for the lateral diffusion of ions into the silicon region to form an ultrashort SDE. Monte Carlo simulation shows that the straggling distribution of ions is only 8 nm, which is shorter than the lateral growth of silicide [14]. Hence, all of the implanted ions were confined in the silicide region and the channel region was not damaged. It has been reported that the ITS process forms a modified Schottky junction with characteristics between a pn junction and a pure Schottky junction [15]–[17]. Since the ion implantation does not directly damage the Si layer, the junction would be free of crystalline defects and low junction leakage current could be expected. During the postimplantation annealing, boron atoms were diffused out of the silicide and piled up at the Si/silicide interface to form an ultrashort SDE uniformly as indicated in Fig. 1(d). In this ITS technique, since the annealing temperature is not determined by the annihilation of ion implantation induced damages, the thermal budget is greatly reduced.

Typical interlayer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. For comparison, a simple SB FinFET without the ITS process step and conventional (CN) FinFET without S/D silicidation were also fabricated. The post S/D implantation annealing was performed at 1025 °C for 20 s in a N_2 ambient for the CN FinFET.

III. Results and Discussion

A. Ni-Salicide Process

Ni reacts with Si to form Ni-rich silicide at temperatures as low as 200 °C, so the Ni-silicide is typically formed by one-step rapid thermal annealing at 400 °C–600 °C for 30–60 s. The unreacted Ni can be selectively removed using a $H_2SO_4 + H_2O_2$ mixture. Since the dominant diffuser during silicide formation is Ni, the Ni-silicide is confined at the Si region and the gate to S/D isolation can be controlled easily. However, as the Si region becomes small, a large number of Ni atoms can be supplied from the Ni film deposited on the isolation region. It has been reported that excess silicidation occurs in the conventional one-step rapid thermal annealing at 500 °C $\sim$ 600 °C due to the fast diffusion of Ni atoms from regions surrounding the small silicon region [18]. In bulk CMOS, the failure modes are poly-Si gate depletion and S/D junction leakage current. In the fully depleted SOI devices, excess silicidation may result in different failure modes.

According to the volume ratio of Ni silicidation, a 22-nm —thick Ni film was deposited by a dc sputtering system to completely convert the 40-nm-thick Si to silicide. Fig. 2 shows the cross-sectional transmission electron micrograph (TEM) of an MSB device after one-step rapid thermal silicidation at 600 °C for 30 s. As expected, no silicide was observed on the sidewall spacer. However, it is surprising that the poly-Si gate was fully

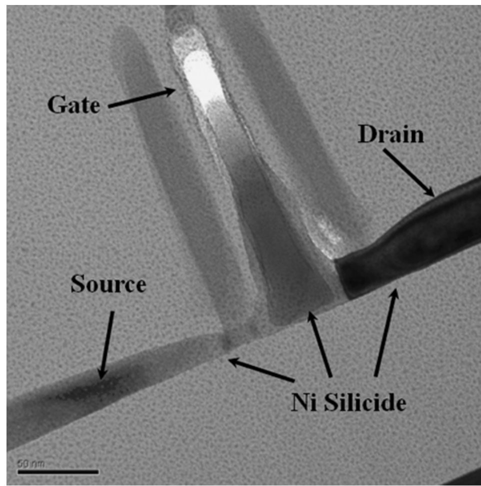

Fig. 2. Cross-sectional TEM of the 25-nm MSB FinFET fabricated by one-step rapid thermal silicidation at 600 °C for 30 s.

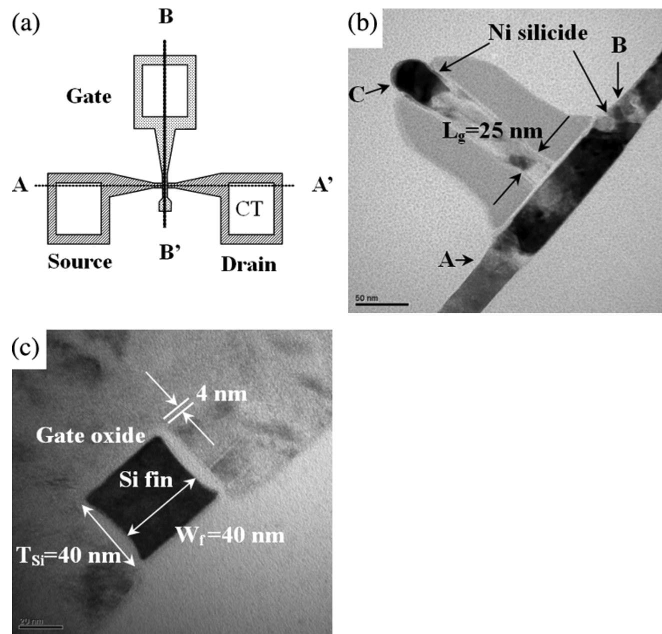

Fig. 3. (a) Schematic layout, (b) cross-sectional TEM micrograph along line A-A′ in (a), and (c) cross-sectional TEM micrograph along line B-B′ in (a) of the MSB FinFET with $L_g = 25$ nm, $W_f = 40$ nm and $T_{\mathrm{Si}} = 40$ nm.

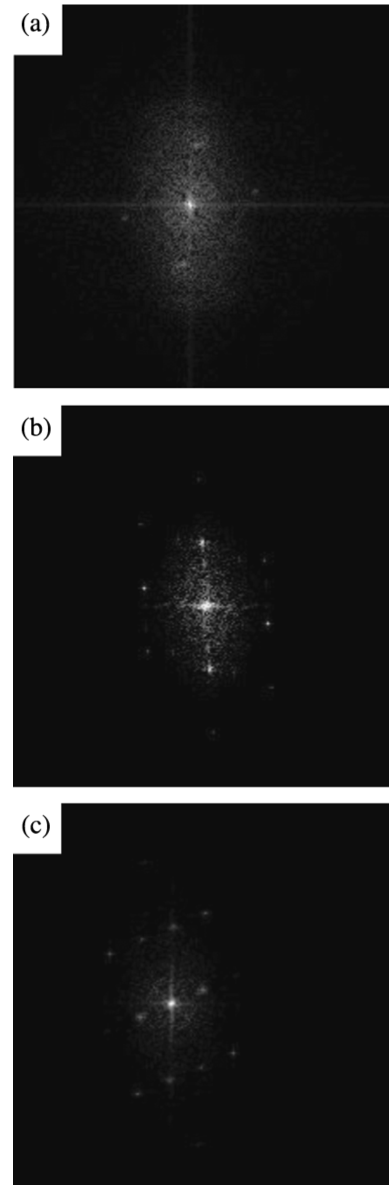

Fig. 4. Electron diffraction pattern of the Ni silicide at (a) position A, (b) position B, and (c) position C, as indicated in Fig. 3(b). Phases at the S/D region and gate region are $\mathrm{NiSi_2}$ and NiSi, respectively.

silicided and the silicide extended from S/D into the channel region so that the whole channel region was converted to silicide and the gate was directly shorted to S/D. The S/D to gate leakage current was measured for all devices.

To completely convert the Si layer in the S/D region into silicide with suitable lateral growth and without excess silicidation, a two-step annealing technique must be employed. Initially, the wafer deposited with 22-nm-thick Ni film was annealed in vacuum chamber at 300 °C for 80 min to form Ni_2Si at the S/D and the poly-Si gate regions. At this low temperature, Ni diffusion from the surrounding regions is slow and is insignificant to cause excess silicidation problem. After selective removal of unreacted Ni, the wafer was rapidly thermally annealed in ambient N_2 at 600 °C for 30 s. During this annealing step, there were no excess Ni atoms surrounding the small active region, so, the excess silicidation problem was avoided. Fig. 3 shows the schematic layout and cross-sectional TEM micrographs of the MSB FinFET with gate length (L_g) of 25 nm, fin thickness (W_f) of 40 nm, and fin height (T_{Si}) of 40 nm. The thickness and lateral growth of silicide are well controlled, and it is confirmed that the SDE was defect-free.

Fig. 4 shows the electron diffraction pattern at the positions of A, B (S/D region), and C (gate region) indicated in Fig. 3(b). The silicide phases at the gate region and S/D region were identified as NiSi and $NiSi_2$, respectively. This phase difference is presumably caused by the differing stresses in the S/D region and gate region [19].

The doping profile of the ultrashort SDE is critical. However, since the volume of the SDE is so small, neither secondary ion mass spectroscopy (SIMS) nor spreading resistance profiling (SRP) could be applied. The spatial resolution of scanning

capacitance microscopy (SCM) was also not sufficient. Kelvin probe force microscopy (KPFM) with a carbon nanotube probe might be a solution but great efforts would be needed to implement this technique [20]. Therefore, we could not correctly determine the doping profile of the SDE at this moment. However, electrical characteristics of the MSB devices shown in the next subsection clearly support the existence of the SDE.

B. Electrical Characteristics

Fig. 5 shows the typical output characteristics of the MSB FinFET and the SB FinFET with $L_g = 25$ nm, $W_f = 40$ nm, and $T_{\mathrm{Si}} = 40$ nm. It is known that for conventional SB devices, the "sublinear" phenomenon is pronounced in the linear region due to the SB and the channel-S/D offset. For our SB FinFET, the large channel-S/D offset should be the dominant mechanism, although the effect of SB cannot be ignored. For the MSB FinFET, the ultrashallow SDE will bridge the channel and S/D silicide. Furthermore, the SB thickness, i.e., the carrier injection resistance from source to channel, is reduced by the high concentration of ultrashort SDE. Therefore, the "sublinear" phenomenon is not observed. On the other hand, the parasitic series resistance is also effectively reduced by the fully silicided S/D structure. The driving current of the 25-nm MSB FinFET at $|V_{\mathrm{ds}}| = |V_{\mathrm{gs}} – V_{\mathrm{th}}| = 1$ V exceeds 108 μA/μm under the definition of channel width $W = 2 * T_{\mathrm{Si}} + W_f$, or 325 μA/μm under the definition of channel width $W = W_f$. It should be noted that the I_{on} could be further improved by shorter spacer length and thinner gate oxide thickness.

Fig. 6 presents the transfer characteristics of the MSB FinFET with $L_g = 25$ nm, $W_f = 40$ nm, and $T_{\mathrm{Si}} = 40$ nm. By inserting an ultrashort SDE to modify the SB property, the MSB FinFET can turn on more steeply and it had an extremely high $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio, exceeding 10^9. The 25-nm MSB FinFET also shows superior subthreshold characteristics with a swing of 83 mV/dec and a drain-induced barrier-lowering (DIBL) of 235 mV/V. These values are close to the three-dimensional simulation results and could be further improved by reducing of the fin height and fin thickness to get better gate controllability [12], [21].

The transfer characteristics of MSB, SB, and CN FinFETs with $L_g = 49$ nm, $W_f = 60$ nm, and $T_{\mathrm{Si}} = 40$ nm are compared in Fig. 7. The poor driving capability of the CN FinFET can be explained by the high S/D resistance due to the unsilicided S/D region. The better DIBL of the MSB FinFET than that of the CN FinFET confirms the advantage of the low thermal budget of the MSB process. The 49 nm MSB FinFET shows an excellent subthreshold swing (60.4 mV/dec), excellent DIBL (39 mV/V), and extremely high $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio ($> 10^9$). These results are better than those reported from conventional FinFETs and SB MOSFETs. Conversely, in the case of SB FinFET, a typical ambipolar operation is observed. For the p-channel operation, the SB FinFET has a poor subthreshold swing and an $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio of lower than 10^3. It has been proposed that the effective SB height of a thin-body SOI SB MOSFET is higher than that of the bulk SB MOSFET due to quantum confinement in the direction normal to the channel so that the on-state current is low [5]. The effective SB at the off-state is lowered by the

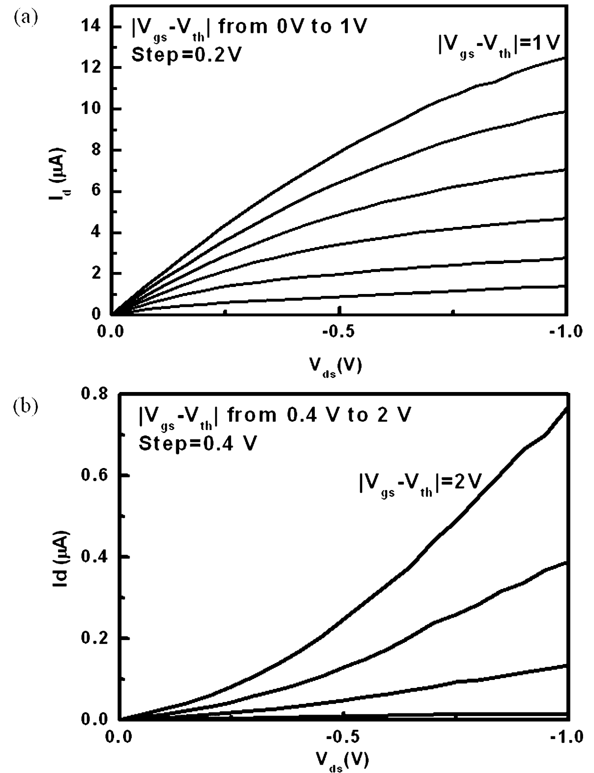

Fig. 5. Output characteristics of (a) the MSB FinFET and (b) the SB FinFET with $L_g = 25$ nm, $W_f = 40$ nm, and $T_{\mathrm{Si}} = 40$ nm.

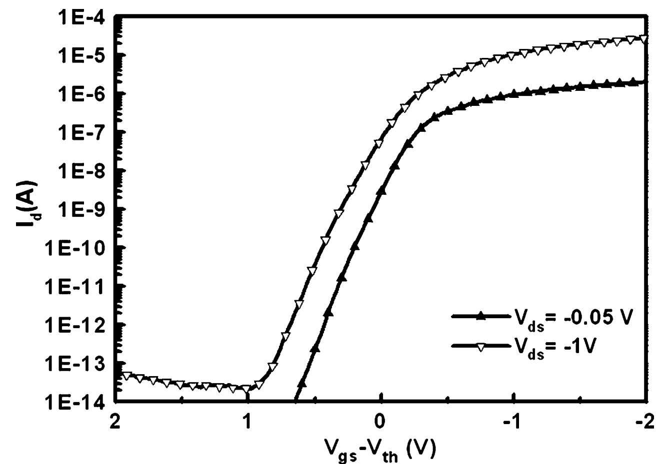

Fig. 6. Transfer characteristics of the MSB FinFET with $L_g = 25$ nm, $W_f = 40$ nm, and $T_{\mathrm{Si}} = 40$ nm.

GIDL-like mechanism, which makes the off-state characteristic of the SB FinFET undesirable [9].

According to the above observations, band diagrams of devices at the on-state and off-state are schematically illustrated in Fig. 8 and Fig. 9, respectively. When the device operates at the on-state, the high concentration ultrashort SDE effectively thins out the SB width between source silicide and the inverted channel so that the holes can tunnel through the barrier much more easily. On the other hand, when the device operates at the off-state, due to the ultrashort SDE, the modified SB at the drain contact is wider and higher than the conventional SB devices, so

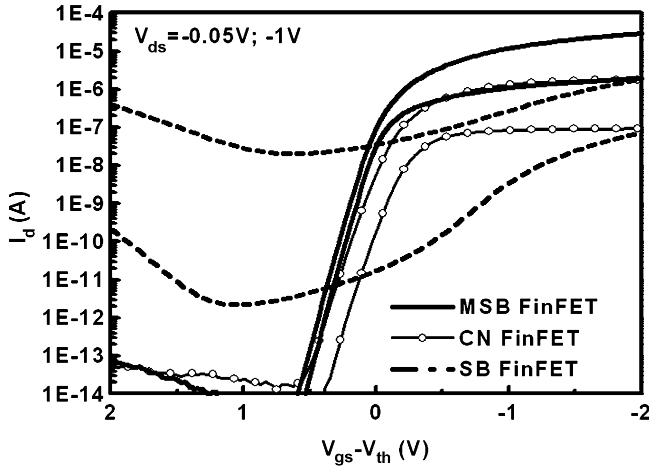

Fig. 7. Transfer characteristics of the MSB, SB, and CN FinFETs with $L_g = 49$ nm, $W_f = 60$ nm, and $T_{\mathrm{Si}} = 40$ nm.

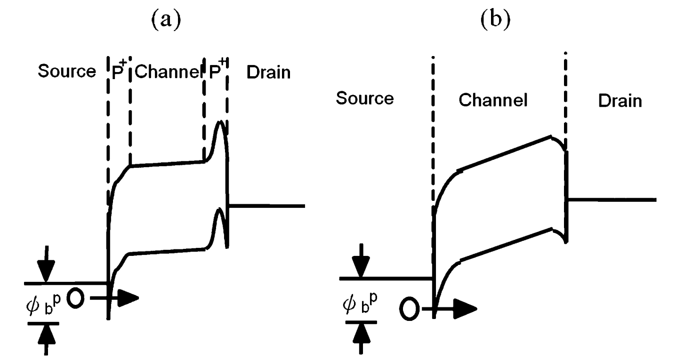

Fig. 8. Schematic band diagrams of (a) MSB FinFET and (b) SB FinFET during the on-state.

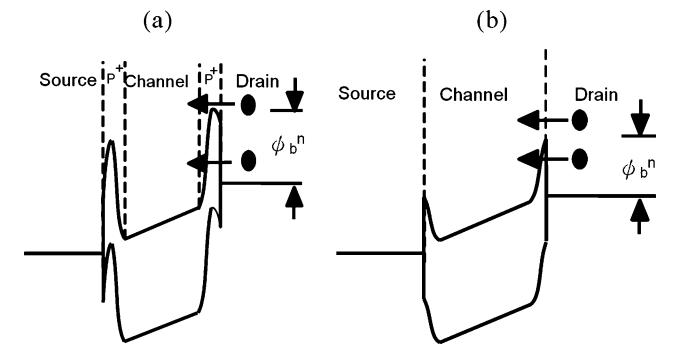

Fig. 9. Schematic band diagrams of (a) MSB FinFET and (b) SB FinFET during the off-state.

it can effectively block electron tunneling. Therefore the proposed MSB FinFET exhibits excellent on/off performance.

To further understand the conduction mechanism of the off-state leakage current, the *I–V* characteristic of the MSB FinFET with $L_g = 65$ nm was measured at different temperatures from 100 K to 500 K, as shown in Fig. 10. At room temperature, the MSB FinFET exhibits a subthreshold swing of 78 mV/decade at $V_{\mathrm{ds}} = -1$ V and extremely high $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio, exceeding 10^9. The I_{off} decreases at lower temperatures, so that the $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio well exceeding 10^{10}

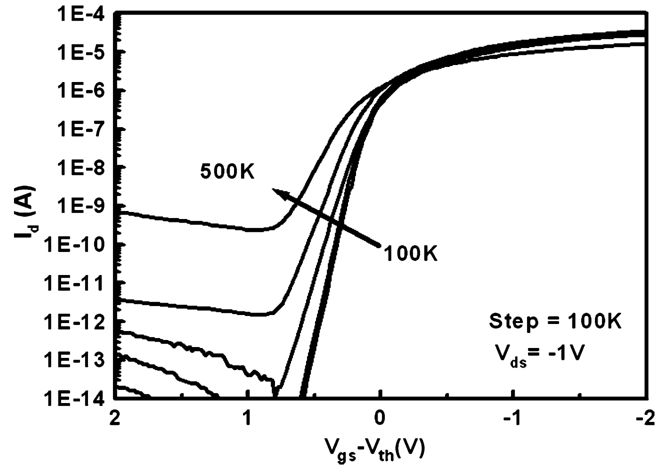

Fig. 10. Transfer characteristics of the MSB FinFET with $L_g = 65$ nm, $W_f = 60$ nm, and $T_{\mathrm{Si}} = 40$ nm measured at temperatures from 100 K to 500 K.

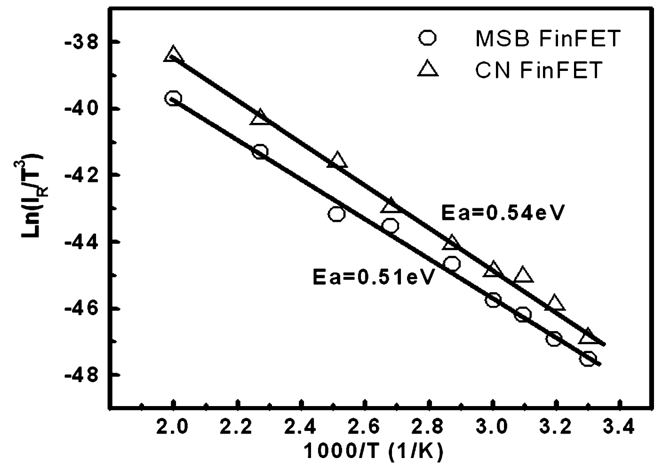

Fig. 11. Arrhenius plots of I_{off} at V_{gs}–$V_{\mathrm{th}} = 0.75$ V and $V_{\mathrm{ds}} = -1$ V of the MSB and CN FinFETs with $L_g = 65$ nm, $W_f = 60$ nm, and $T_{\mathrm{Si}} = 40$ nm.

and the subthreshold swing better than 74 mV/dec are achieved at 100 K. The Arrhenius plot of I_{off} for the 65-nm MSB FinFET and CN FinFET at $V_{\mathrm{ds}} = -1$ Vand V_{gs}–$V_{\mathrm{th}} = 0.75$ V are shown in Fig. 11. The activation energies are 0.51 and 0.54 eV for MSB FinFET and CN FinFET, respectively. The fact that there is almost the same activation energy implies that the MSB junction is very close to the pn junction and the low temperature process of 600 °C is sufficient to drive dopants out of the silicide. Since the S/D implantation does not directly damage the Si region of the MSB FinFET and the CN FinFET experiences high temperature post-S/D implantation annealing, the low activation close to half of the energy gap cannot be explained by the defects in the Si region. The leakage current mechanism of pn junction formed by the ITS process has been investigated in the literature [15], [22]. Since the Si region is almost defect-free, the area component of leakage current is dominated by the diffusion mechanism even at room temperature. However, the peripheral component of leakage current is dominated by the surface generation current due to the surface states at the isolation edge within the depletion region. For a square junction with area smaller than 10 μm^2, the leakage current will be dominated by the peripheral component

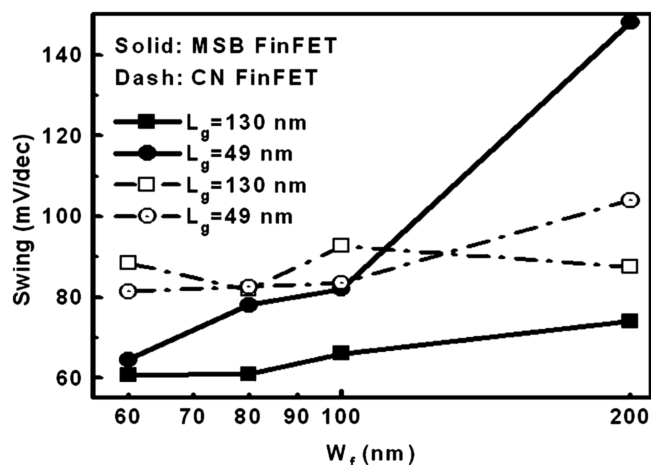

Fig. 12. Substhreshold swing of MSB and CN FinFETs with different fin thicknesses as $L_g = 130$ nm and 49 nm.

at temperatures lower than 200 °C. For fully depleted SOI devices, the junction area $T_{\rm Si} \times W_f$ is very small. The leakage current would be dominated by the surface generation current due to the surface states at the interface between gate oxide/Si and buried oxide/Si, so the low activation energy becomes reasonable. It is thus proposed that to further reduce the $I_{\rm off}$ of MSB FinFET, the interface quality of gate oxide and buried oxide must be improved.

C. Fin Width Effect

The short-channel effect of FinFETs has been studied numerically and experimentally by several research groups [23]–[25]. Pei *et al.* proposed that in order to suppress SCE, the fin thickness must be less than one third of the channel width [23]. Chau *et al.* reported that to maintain full substrate depletion, the Si body thickness should be about 1/3 or 2/3 of the gate length in the case of single gate or double gate structures, respectively [24]. In the case of a tri-gate structure, the required Si body thickness becomes equal to the gate length [25]. In fact, the threshold channel length depends on the gate structure and the fin concentration. Fig. 12 shows the subthreshold swing of the MSB and CN FinFETs as a function of fin thickness with $L_g = 49$ nm and 130 nm. The CN FinFETs shows weak fin thickness dependence, which is quite different from the results in some earlier reports [23], [25], which may be explained by the low fin concentration employed in this paper. Here, the top gate alone can fully deplete the channel, so the fin thickness does not clearly affect the SCE apparently. The subthreshold swing of the CN FinFETs is worse than that of the MSB FinFETs in Fig. 12, which may result from the induced higher interface state density induced by the boron penetration.

For the MSB FinFET, thinner fin thickness results in lower subthreshold swing. However, the extent of improvement differs for MSB and CN FinFETs. Furthermore, the 130 nm MSB FinFETs exhibit better swing than the 49 nm MSB FinFETs at all fin thicknesses. Since the CN FinFETs do not show this phenomenon, it cannot be explained by the gate control capability.

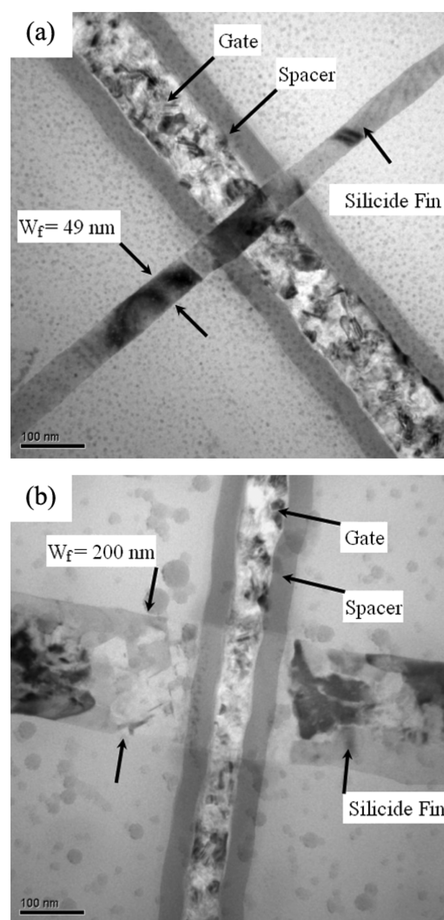

Fig. 13. Plane view TEM micrographs of the MSB FinFETs with (a) $W_f = 49$ nm and (b) $W_f = 200$ nm.

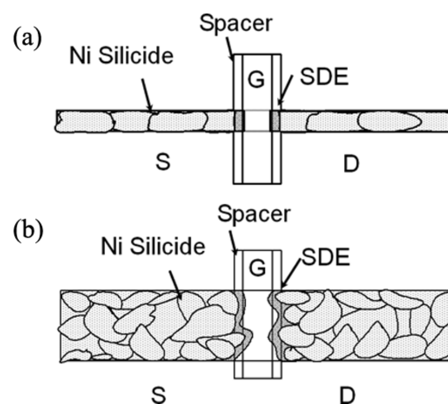

Fig. 14. Schematic drawing of the grain structure at the S/D region and the SDE profile of the MSB FinFETs with (a) $W_f = 49$ nm and (b) $W_f = 200$ nm.

We suspect that this unusual phenomenon is related to the S/D silicidation.

Fig. 13(a) and (b) shows the plane view TEM micrographs of the MSB FinFETs with $W_f = 49$ nm and 200 nm, respectively. The silicided narrow fin shows a bamboo structure and only a single grain exists at the front edge of the S/D region. As the fin thickness becomes larger, the S/D region consists of multiple grains. This multigrain structure results in a nonuniform front edge of the silicide, which in turn results in nonuniform front

edge of the ultrashort SDE, as shown schematically in Fig. 14. As the channel length is short, a minimal nonuniformity of the S/D junction front edge clearly affects the device subthreshold characteristic. This postulation is also supported by the weak fin thickness dependence of subthrehold swing for the CN FinFETs shown in Fig. 12 because the CN FinFETs have a smooth S/D junction front edge. For thin fin devices, the CN FinFETs show worse swing than the MSB FinFETs. The high external resistance of the unsilicided S/D of the CN FinFETs could explain this phenomenon.

Fig. 15 shows the DIBL of the MSB and CN FinFETs as a function of fin thickness, indicating a trend similar to the swing. It can be observed that with suitable combination of channel length and fin thickness, MSB FinFETs can be achieved with an excellent performance of nearly ideal subthreshold swing of 60.4 mV/dec and DIBL of 39 mV/V.

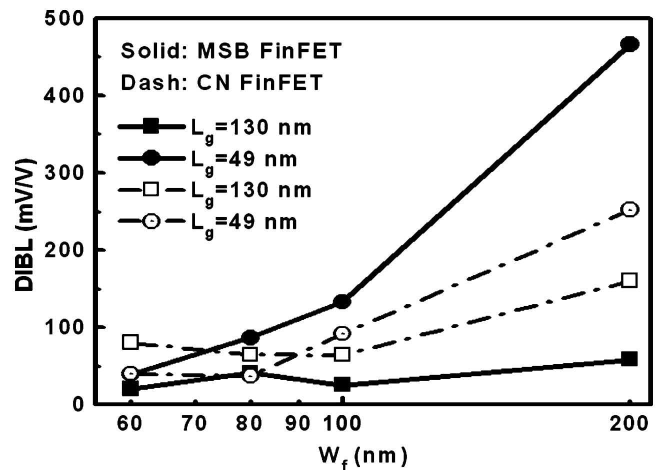

Fig. 15. DIBL of MSB and CN FinFETs with different fin thicknesses as L_g = 130 nm and 49 nm.

IV. Conclusion

This paper demonstrated a novel high-performance MSB FinFETs with several unique features such as fully silicided S/D, ultrashort SDE, defect-free S/D junction, and low-temperature processing. A two-step Ni-salicide process was developed to completely convert the Si layer at the S/D region to silicide with controlled lateral silicidation. By inserting an ultrashort SDE using the ITS technique, the SB was modified so that the barrier width was suppressed at the on-state and was increased at the off-state. In addition, the triple-gate wrapping around the fin also effectively diminished the SB by the gate-fringing effect. With a 4-nm-thick gate oxide, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio over 10^9 was achieved, and the room temperature subthreshold swings of 25 and 49 nm MSB FinFETs were as low as 83 and 60.4 mV/dec, respectively. These values are close to the theoretical limitations. The I_{on} of the 25-nm MSB FinFET at $|V_d| = |V_g–V_{\mathrm{th}}| = 1$ V was higher than 108 or 325 μA/μm, depending on the definition of channel width. The I_{on} of 108 μA/μm is lower than the conventional devices. However, if we consider the actual deriving capability of devices with the same layout width, the I_{on} of the MSB FinFET, 325 μA/μm, will be compatible with that of conventional planar MOSFETs. The contact resistance between silicide and heavily doped Si region increases greatly in the FinFET due to the nanoscale contact area, and this resistance may degrade device performance if not carefully controlled. Therefore, the contact resistance of the MSB junction must be examined so that the limitation of MSB FinFET can be well understood. Test wafers for extracting the contact resistance of the lateral MSB junction are currently being processed and the impact of contact resistance on device performance is under evaluation by three-dimensional simulators. These results will be reported later.

Activation energy analysis indicates that the SDE effectively modifies the SB, resulting in excellent electrical characteristics. The same activation energy of the low thermal budget MSB FinFETs and high thermal budget CN FinFETs confirms that the MSB junction is very close to the pn junction and the low temperature process of 600 °C is sufficient to drive dopants out of silicide. Since the leakage current of drain junction at the off-state is dominated by the surface generation current due to the surface states at the gate oxide/Si and buried oxide/Si interface, it is thus proposed that to further reduce the I_{off} of MSB devices, the interface quality of gate oxide and buried oxide must be improved.

Structural analysis shows that as the fin width becomes larger than the silicide grain size, the multigrain structure results in a rough front edge of the MSB junction, which in turn degrades the short channel device performance. This result indicates that the MSB process is suitable for FinFETs.

Beyond the 65-nm technology node, it is predicted that the metal gate and high-κ gate dielectric must be employed to improve the device characteristics continuously. Furthermore, thermal stability between metal gate and high-κ dielectric is a critical issue because the conventional S/D process requires a high-temperature annealing of at least 900 °C. Since the MSB process temperature is around 600 °C, the thermal stability issue is relaxed and the interfacial layer formation at high k dielectric and Si interface is also reduced. Furthermore, the low thermal budget produced by the ultrashort SDE helps device scale-down. It can thus be considered that the MSB FinFET is a very promising nanodevice.

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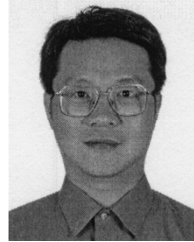

Bing-Yue Tsui (S’87-M’93-SM’01) was born in Chiayi, Taiwan, R.O.C., in 1963. He received the B.S., M.S., and Ph.D. degrees from National Chiao-Tung University, Hsinchu, Taiwan, in 1985, 1987, and 1992, respectively, all in electrical engineering.

He joined the Electronics Research and Service Organization, Industrial Technology Research Institute (ERSO/ITRI), Hsinchu in October, 1992. From 1992 to 1994, he worked on 0.5-μm/16-Mb DRAM process integration. Since 1995, he led the submicrometer device technology group to develop subquartermicrometer MOSFETs. Since 1997, he was Project Leader and Section Manager of etching technology. Since 1998, he has led the Etching and Process Integration Department to develop the deep submicrometer Al-interconnect and Cu/low-κ interconnect technologies. Currently, he is an Associate Professor at National Chiao-Tung University, Hsinchu. He is now interested in the Cu/low-κ dielectric integration, metal gate/high-κ dielectric integration, nanoscale Si devices, and carbon nanotube devices. He has authored or coauthored more than 40 journal papers and 60 conference papers. He also owns 16 Taiwan-based patents and 12 U.S. patents. Another 16 patents are pending.

Dr. Tsui was given the Research Paper Award by the Industrial Technology Research Institute and the Outstanding Young Electrical Engineer by the Institute of Chinese Engineers, both in 1998. He is a member of Phi Tau Phi and his name is listed in *Who is Who in the World, Who is Who in Finance and Industry, Who is Who in Science and Engineering*, and *Who is Who in Asia and the Pacific IX Nations*.

Chia-Pin Lin (S’02) was born in Hsinchu, Taiwan, R.O.C. in 1976. He received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, in 1999 and 2001, respectively, where he is currently pursuing the Ph.D. degree with the Institute of Electronics.

His current research topic is the fabrication and characterization of MSB FinFET and poly-Si thin-film-transistors (TFTs).