ESD Protection Design for I/O Cells With Embedded SCR Structure as Power-Rail ESD Clamp Device in Nanoscale CMOS Technology

Ming-Dou Ker, *Senior Member, IEEE,* and Kun-Hsien Lin, *Member, IEEE*

***Abstract*—This paper presents a new electrostatic discharge (ESD) protection design for input/output (I/O) cells with embedded silicon-controlled rectifier (SCR) structure as power-rail ESD clamp device in a 130-nm CMOS process. Two new embedded SCR structures without latchup danger are proposed to be placed between the input (or output) pMOS and nMOS devices of the I/O cells. Furthermore, the turn-on efficiency of embedded SCR can be significantly increased by substrate-triggered technique. Experimental results have verified that the human-body-model (HBM) ESD level of this new proposed I/O cells can be greater than 5 kV in a 130-nm fully salicided CMOS process. By including the efficient power-rail ESD clamp device into each I/O cell, whole-chip ESD protection scheme can be successfully achieved within a small silicon area of the I/O cell.**

***Index Terms*—Electrostatic discharge (ESD), input/output (I/O) cell, silicon controlled rectifier (SCR), power-rail ESD clamp device.**

I. Introduction

ON-CHIP electrostatic discharge (ESD) protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS integrated circuits (ICs) [1], [2]. The typical design of on-chip ESD protection circuits in a CMOS IC is illustrated in Fig. 1. The pMOS and nMOS are used as on-chip ESD protection devices for input and output pads. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [3]–[5], the power-rail ESD clamp circuit must be placed between VDD and VSS power lines [6]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), positive-to-VDD (PD-mode), negative-to-VSS (NS-mode), and negative-to-VDD (ND-mode) [7]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS and the VDD-to-VSS ESD clamp circuit to ground. However, due to the parasitic resistance and capacitance along the VDD and VSS power lines, ESD protection efficiency is dependent on the pin location in a chip. To quickly bypass the ESD current during ESD-stress condition, the efficient VDD-to-VSS ESD clamp circuits are repeatedly inserted between VDD and VSS power lines in the appropriate distance to provide a low-impedance path between the VDD and VSS power lines [6]. Therefore, how to realize the area-efficient and turn-on-efficient power-rail ESD clamp circuits will be an important challenge to system-on-a-chip (SOC) applications with a much larger chip size but a reduced cell pitch for the I/O cell.

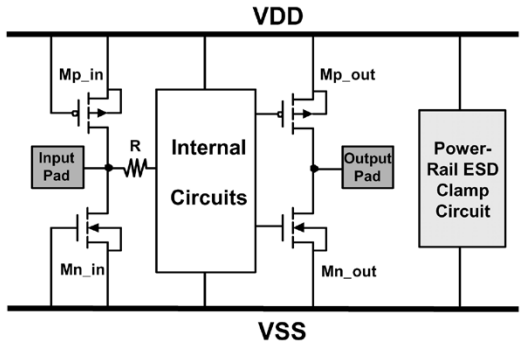

Fig. 1. Typical design of on-chip ESD protection circuits in a CMOS IC. The turn-on efficient power-rail ESD clamp circuit is placed between VDD and VSS power line to avoid unexpected ESD damage in the internal circuits.

For CMOS IC applications, SCR can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [8]–[11], which can even provide efficient ESD protection to the ultrathin gate oxide in nanoscale CMOS process [12]. However, SCR device was susceptible to latchup danger under normal circuit operating condition [13]–[15]. Because of the low holding voltage, such SCR devices could be accidentally triggered on by the noise pulses, when ICs are in normal circuit operating conditions.

In the traditional I/O cells, double guard rings had been often inserted between input (or output) pMOS and nMOS devices to avoid the latchup issue [16]. The layout view and device structures of the traditional I/O cell are shown in Fig. 2(a) and (b), respectively. With the scaled-down device dimension in nanoscale CMOS technology, the power supply voltage is also scaled down to meet the circuit requirement and gate-oxide reliability. The maximum supply voltage is only 1.2 V in a 130-nm CMOS technology with the thin gate oxide of 20 Å. If the holding voltage of parasitic SCR device is greater than the power supply voltage, latchup issue will not occur in such nanoscale CMOS process. Therefore, the SCR or parasitic SCR

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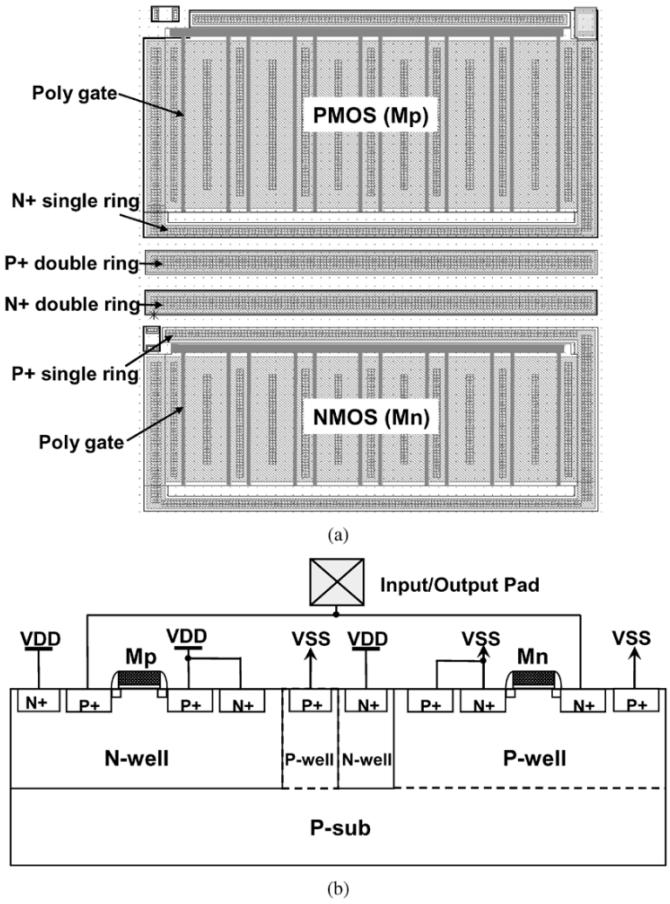

Fig. 2. (a) Layout view and (b) device structures of the traditional I/O cell with double guard rings inserted between input (or output) pMOS and nMOS devices.

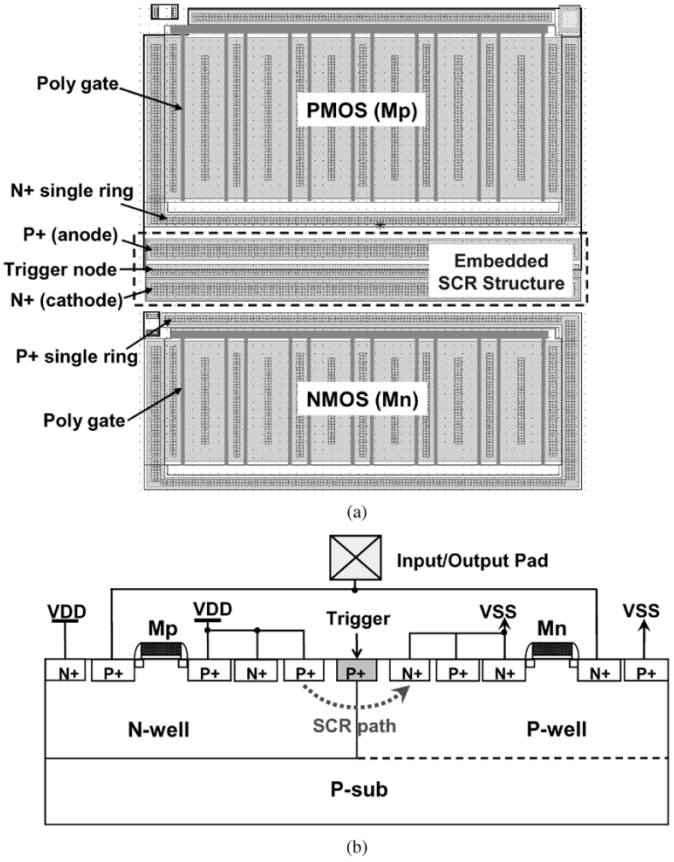

Fig. 3. (a) Layout view and (b) device structures of the new proposed I/O cell with embedded SCR structure I. The anode and cathode of embedded SCR structure I are formed by inserting extra p+ diffusion in n-well and n+ diffusion in p-well, respectively.

device can be used as on-chip ESD protection device without latchup concern in nanoscale CMOS process.

In this paper, SCR is used as VDD-to-VSS ESD clamp device within each I/O cell in a 130-nm CMOS process without latchup issue. Two new embedded SCR structures are proposed to replace the double guard rings in the traditional I/O cells. The turn-on speed of embedded SCR structures is enhanced to quickly discharge ESD current by substrate-triggered technique [17]. Such new proposed I/O cells with embedded SCR structure as power-rail ESD clamp device have been successfully verified in a 130-nm CMOS process for SOC applications.

II. Embedded SCR Structures in I/O Cells

If the holding voltage of the parasitic SCR is greater than the maximum voltage level of circuit operation, the double guard rings surrounding the input (or output) pMOS and nMOS devices in the I/O cells can be removed. To avoid the latchup occurrence in the internal circuits due to the noise triggering at the I/O pad, the additional guard rings should be added between the I/O cells and the core circuits [16]. Thus, the parasitic SCR structure between input (or output) pMOS and nMOS devices can be used as power-rail ESD clamp device in each I/O cell. The layout view and device structures of the new proposed I/O cell with embedded SCR structure I are shown in Fig. 3(a) and (b), respectively. Keeping the single guard ring in the I/O cell, the anode and cathode of embedded SCR structure I are formed by inserting the extra p+ diffusion in n-well and the extra n+ diffusion in p-well, respectively. To enhance the turn-on speed of embedded SCR structure, the p+ diffusion inserted half in n-well and half in p-well is connected out as substrate-triggered node. When a trigger current is applied into this trigger node, SCR will be triggered into its latching state quickly through the positive feedback regeneration mechanism [18]. The substrate-triggered technique can be realized by the *RC*-based ESD detection circuit [17]. With *RC*-based ESD detection circuit, the embedded SCR structure is kept off during the normal circuit operating condition, but it can be quickly triggered on during the ESD stress condition.

The ESD current discharging paths through the I/O cell with embedded SCR structure I under PS-mode, PD-mode, NS-mode, and ND-mode ESD stresses are shown in Fig. 4(a)–(d), respectively. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through two discharging paths (path A and path B), as the dashed lines shown in Fig. 4(a). The first discharging path (path A) is that the ESD current is discharged through the parasitic diode of pMOS (Mp) to VDD, and then through the embedded SCR structure from the VDD power line to the grounded VSS power line. The second discharging path (path B) is that the ESD current is directly discharged through the parasitic SCR structure from the I/O pad to the grounded VSS power line. Because the ESD

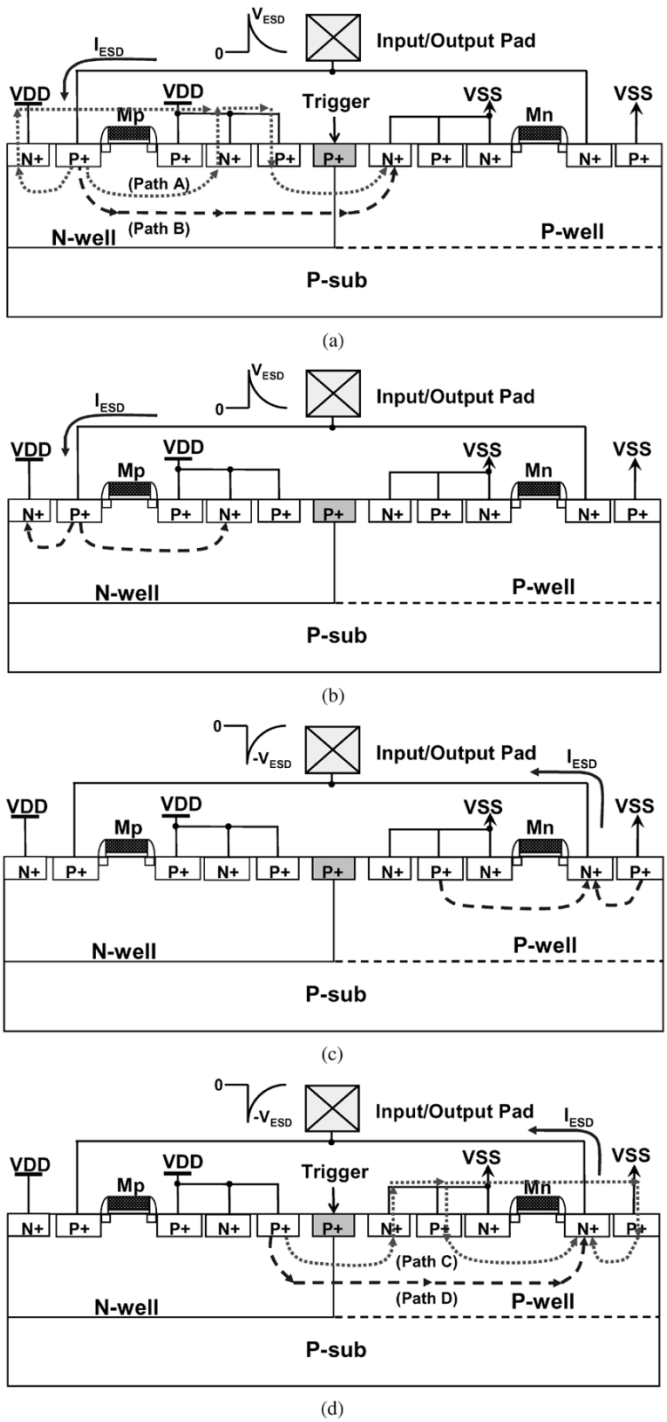

Fig. 4. ESD current discharging paths of the I/O cell with embedded SCR structure I under: (a) positive-to-VSS ESD stress condition, (b) positive-to-VDD ESD stress condition, (c) negative-to-VSS ESD stress condition, and (d) negative-to-VDD ESD stress condition.

current will be discharged through parasitic forward-diode path to VDD first, the ESD detection circuit can detect such ESD pulse to provide the substrate-triggered current to raise up the local substrate potential. The embedded SCR structure and the parasitic SCR structure from the drain of the pMOS to the grounded n+ in the p-well can be quickly triggered on to discharge the ESD current by such substrate-triggered current. The major ESD current will be discharged through the path with lower clamping voltage and lower turn-on resistance. The ESD current at the I/O pad under PD-mode ESD stress can be discharged through the parasitic diode of pMOS (Mp) to the grounded VDD power line, as the dashed lines shown in Fig. 4(b). The negative ESD current at the I/O pad under NS-mode ESD stress can be discharged through the parasitic diode of the nMOS (Mn) to the grounded VSS power line, as the dashed lines shown in Fig. 4(c). The negative ESD current at the I/O pad under ND-mode ESD stress can be discharged through two discharging paths (path C and path D), as the dashed lines shown in Fig. 4(d). The first discharging path (path C) is that the negative ESD current is discharged through the parasitic diode of nMOS (Mn) to VSS, and then through the embedded SCR structure from the VSS power line to the grounded VDD power line. The second discharging path (path D) is that the negative ESD current is directly discharged through the parasitic SCR structure from the I/O pad to the grounded VDD power line. Because the negative ESD current will be discharged through the parasitic forward-diode path to VSS first, the ESD detection circuit can detect such ESD pulse to provide the substrate-triggered current to raise up the local substrate potential. The embedded SCR structure and the parasitic SCR structure from the p+ connected to VDD in the n-well to the drain of the nMOS can be quickly triggered on to discharge the ESD current by such substrate-triggered current. With the two discharging paths, the ESD robustness of the I/O pad under PS-mode and ND-mode ESD stresses can be further improved. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed I/O cell with embedded SCR structure I.

The layout area of the I/O cell can be further reduced by the new embedded SCR structure II. The layout view and device structures of the new proposed I/O cell with embedded SCR structure II are shown in Fig. 5(a) and (b), respectively. Without the double guard rings, the anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively. The poly gate in the layout view has a close-loop ring to increase the anode and cathode areas of embedded SCR structure II. The ESD current discharging paths of the I/O cell with embedded SCR structure II under four modes ESD stresses are the same with that of the I/O cell with embedded SCR structure I. Especially, under the PS-mode ESD stress, the parasitic SCR (path B) from the drain of pMOS to the source of nMOS can be triggered on to discharge ESD current. Under the ND-mode ESD stress, the parasitic SCR (path D) from the source of pMOS to the drain of nMOS provides the second ESD discharging path. It is important to note that the second discharging path for the I/O cell with embedded SCR structure II under PS-mode ESD stress (path B) or under ND-mode ESD stress (path D) becomes more efficient due to the smaller anode-to-cathode spacing of the parasitic SCR structure. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed I/O cell with embedded SCR structure II.

The new proposed whole-chip ESD protection scheme with embedded SCR structure as power-rail ESD clamp device in each I/O cell is shown in Fig. 6. With the embedded SCR structure in each I/O cell, the whole-chip ESD protection efficiency

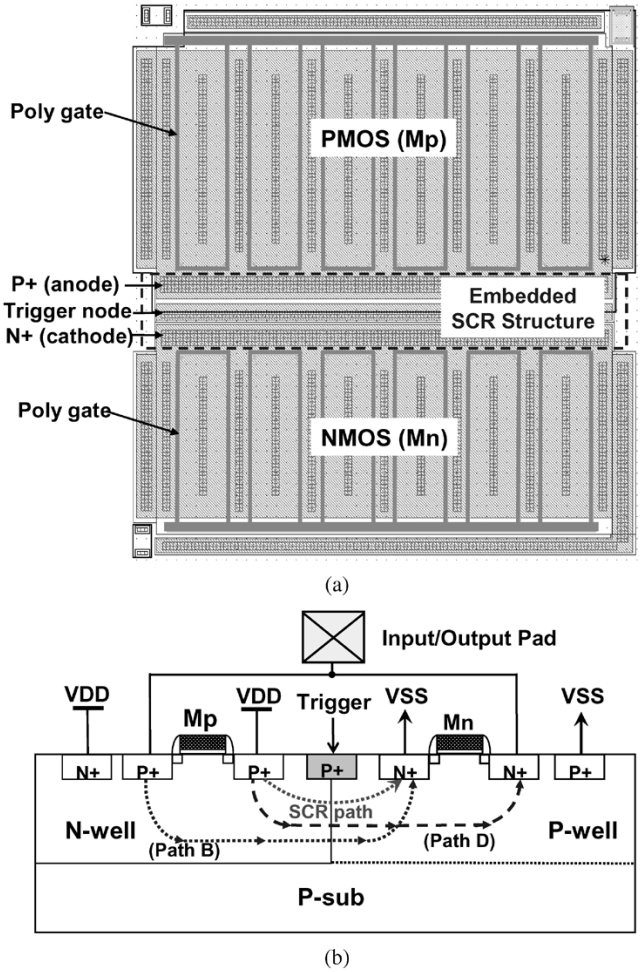

Fig. 5. (a) Layout view and (b) device structures of the new proposed I/O cell with embedded SCR structure II. The anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively.

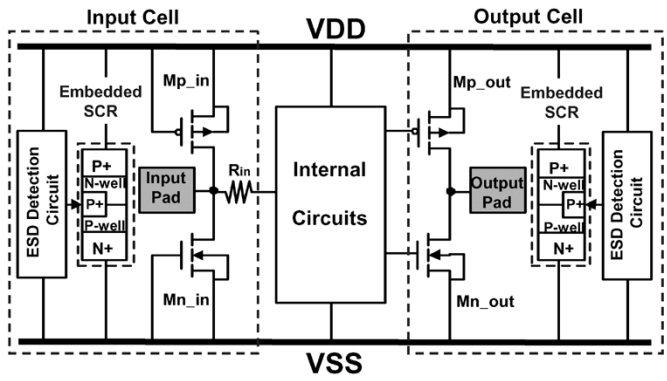

Fig. 6. The new proposed whole-chip ESD protection scheme with embedded SCR structure in each I/O cell. The substrate-triggered technique was realized by the *RC*-based ESD detection circuit.

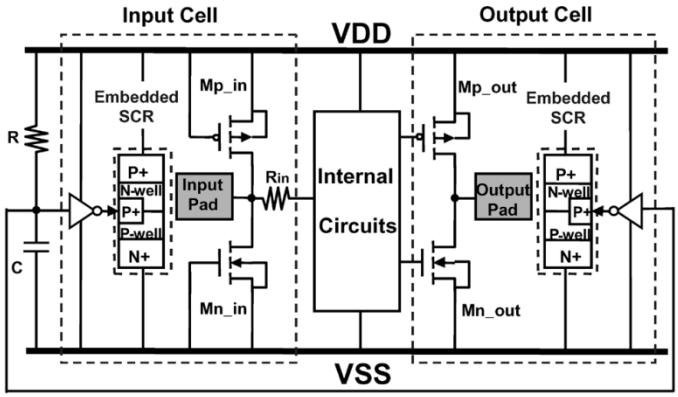

Fig. 7. In the whole-chip ESD protection scheme, one set of delay-based *R* and *C* in the ESD detection circuit can be shared for all I/O cells to reduce the layout area for high-pin-count applications.

is not degraded by the different pin locations in the chip. This will be more valuable for applications in the SOC chip with hundreds of I/O pins. To reduce the layout area for high-pin-count applications, one set of delay-based *R* and *C* in the ESD detection circuit can be shared for all I/O cells, which are powered with the same power domain, as shown in Fig. 7. Such *R* and *C* can be implemented in the area of VDD or VSS cells, which provide the power for I/O cells.

III. Experimental Results

The testchips with the traditional I/O cells and the new proposed I/O cells have been fabricated in a 130-nm salicided CMOS process. The input ESD protection devices are realized by the gate-connected-to-source pMOS (GDPMOS) and gate-grounded nMOS (GGNMOS) with the device dimensions (W/L) of 240/0.18 and 180/0.18 (μm/μm), respectively. The output ESD protection devices are realized by the output buffer of pMOS and nMOS with the same device dimensions as those of the input cell. The layout parameters of input ESD protection devices and output buffers are drawn according to the foundry's ESD rules with or without silicide blocking for comparison. In the new proposed I/O cells, the embedded SCR structures I and II are fully silicided with the SCR device widths of 49.5 and 45.5 μm, respectively. The spacing from anode to cathode of the embedded SCR structure is kept at 2.35 μm. The total layout area of the whole I/O cell with embedded SCR structure I is only 60 μm $\times$ 50 μm, and that with embedded SCR structure II is only 50 μm $\times$ 50 μm. The ESD detection circuit including *R*, *C*, and inverter is realized with $R = 60$ kΩ, $C = 3$ pF, pMOS dimension $W/L = 40/0.18$ (μm/μm), and nMOS dimension $W/L = 8/0.18$ (μm/μm). The layout area of ESD detection circuit is 60 μm $\times$ 17 μm.

A. DC I–V Characteristics

To avoid the latchup issue, the holding voltage of the ESD protection circuit with SCR device must be designed greater than the maximum voltage level of VDD. The DC *I–V* characteristics of embedded SCR structures I and II in the I/O cells are measured (using Tek370 curve tracer) by applying a voltage sweep on the VDD pin under the bias condition of 0–V VSS but I/O pad is floating. The measured DC *I–V* characteristics of embedded SCR structures I and II under different temperatures are shown in Fig. 8(a) and (b), respectively. The dependence of holding voltage of embedded SCR structures under different temperatures is summarized in Fig. 9. From the measured results, the holding voltage of embedded SCR structures slightly reduces when the temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is

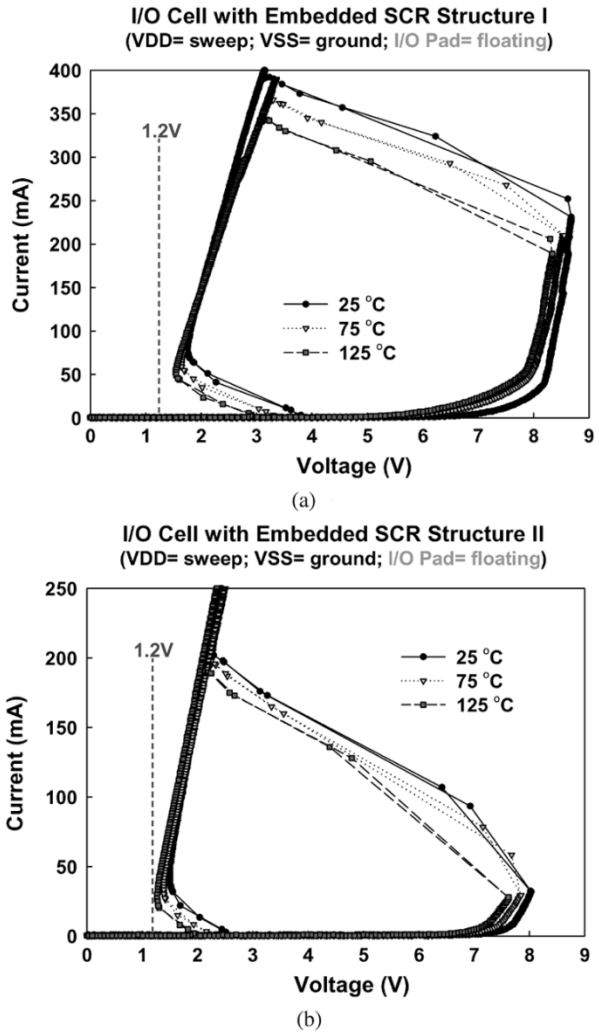

Fig. 8. Measured DC *I–V* characteristics of (a) the embedded SCR structure I, and (b) the embedded SCR structure II, in the I/O cells under different temperatures.

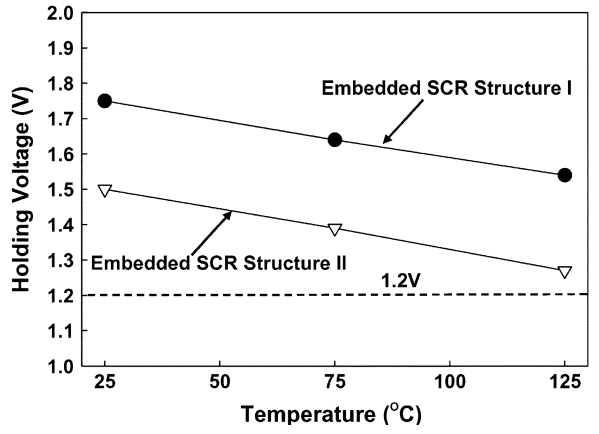

Fig. 9. Relation between the holding voltage of the embedded SCR structures and the operating temperature.

increased with the increase of temperature. With smaller equivalent well resistance, the holding voltage of embedded SCR structure I is larger than that of embedded SCR structure II. The holding voltages of embedded SCR structures I and II at temperature of 125 °C are 1.54 and 1.27 V, respectively, which

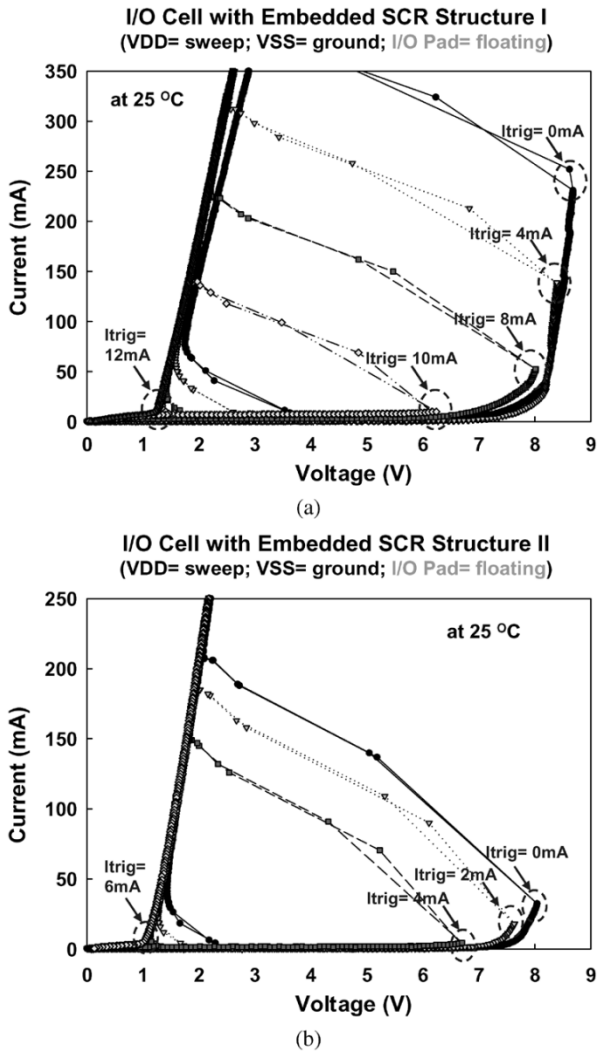

Fig. 10. Measured DC *I–V* characteristics of the (a) embedded SCR structure I, and (b) embedded SCR structure II, in the I/O cells under different substrate-triggered currents (Itrig).

are both greater than VDD of 1.2 V. The measured results have verified that the embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup issue. Especially, the embedded SCR I has a high switching current of greater than 200 mA in Fig. 8(a), which is suitable for application in a noisy environment to avoid accidental triggering.

The measured DC *I–V* characteristics of embedded SCR structures I and II in the I/O cells under different substrate-triggered currents (Itrig) are shown in Fig. 10(a) and (b), respectively. As shown in Fig. 10, the switching voltage of the embedded SCR structure I without the substrate-triggered current is ∼8.5 V (by p+ trigger node/n-well junction breakdown), and that of the embedded SCR structure II is ∼8 V. The switching current and switching voltage of the embedded SCR structure are decreased while the substrate-triggered current is increased. ESD protection devices with low switching voltage can be turned on more quickly to discharge ESD current to provide more effective protection for internal circuits. To provide effective ESD protection to the ultrathin gate oxide in 130-nm CMOS process, the substrate-triggered current of 12 mA for embedded SCR structure I and substrate-triggered current of

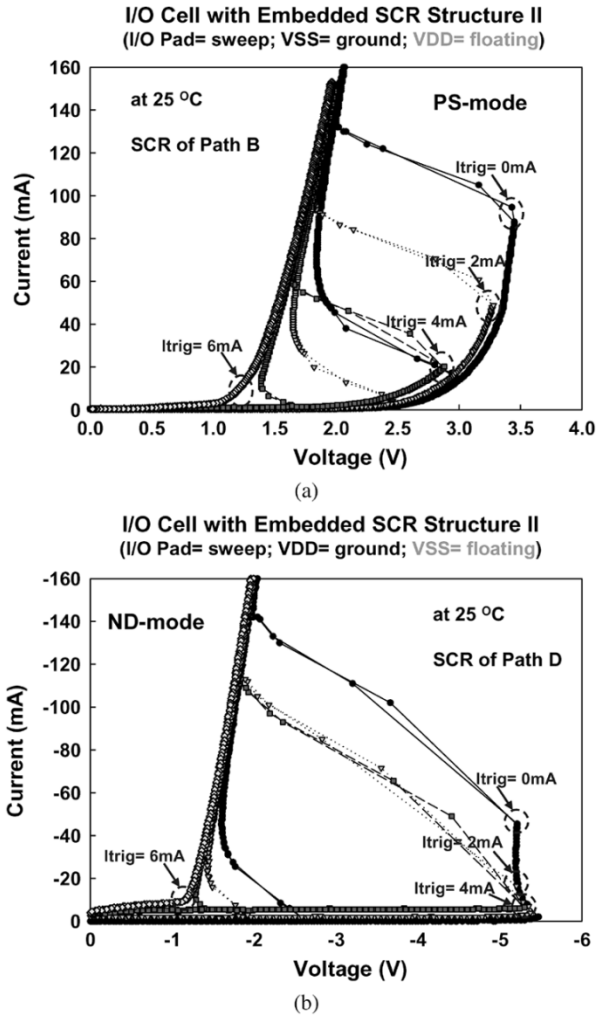

Fig. 11. Measured DC *I–V* characteristics of (a) the parasitic SCR structure (path B) between I/O pad and VSS power line, and (b) the parasitic SCR structure (path D) between I/O pad and VDD power line, in the I/O cell with embedded SCR structure II under different substrate-triggered currents (Itrig).

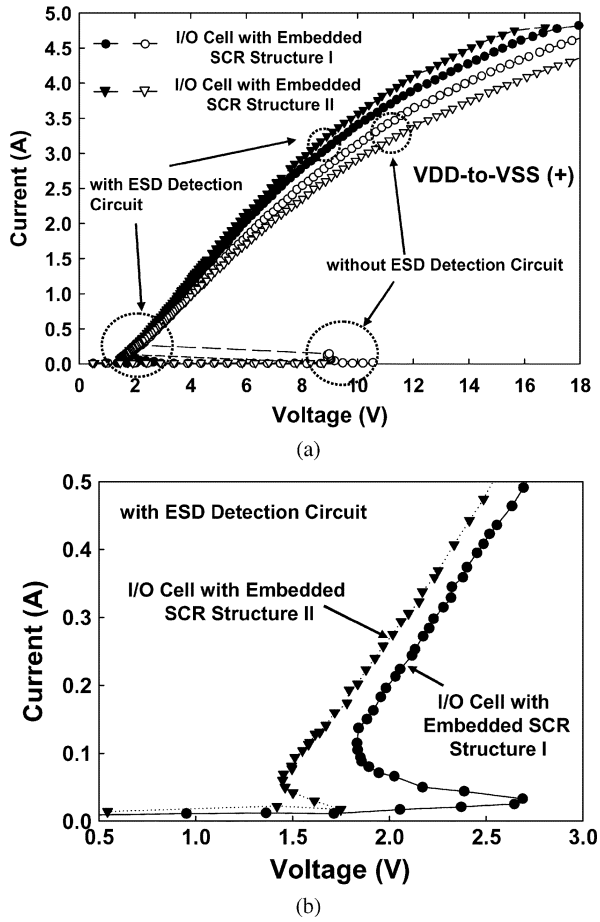

Fig. 12. (a) The TLP-measured *I–V* curves of the I/O cells with embedded SCR structures I and II under positive VDD-to-VSS ESD stress with or without ESD detection circuit. (b) The enlarged view around the switching point of the measured curves for I/O cells with ESD detection circuit.

6 mA for embedded SCR structure II are suggested for the design.

From the discussions in Section II, one parasitic SCR structure (path B) between I/O pad and VSS power line can be triggered on to discharge ESD current for I/O pad under PS-mode ESD stress, and another parasitic SCR structure (path D) between I/O pad and VDD power line can be triggered on to discharge ESD current for I/O pad under ND-mode ESD stress. The DC *I–V* characteristics of these parasitic SCR structures for the I/O cell with embedded SCR structure II are measured to verify their effectiveness. The DC *I–V* characteristics of parasitic SCR structure (path B) between I/O pad and VSS power line are measured by applying a voltage sweep on the I/O pad under the bias condition of 0–V VSS but VDD is floating similar to PS-mode. The measured DC *I–V* characteristics of parasitic SCR structure (path B) between I/O pad and VSS power line under different substrate-triggered currents are shown in Fig. 11(a). In addition, the DC *I–V* characteristics of parasitic SCR structure (path D) between I/O pad and VDD power line are measured by applying a negative voltage sweep on the I/O pad under the bias condition of 0–V VDD but VSS is floating similar to ND-mode. The measured DC *I–V* characteristics of parasitic SCR structure (path D) between I/O pad and VDD power line under different substrate-triggered currents are shown in Fig. 11(b). From the measured results, the holding voltage of parasitic SCR structure (path B) between I/O pad and VSS power line at temperature of 25 °C is 1.84 V, and that of parasitic SCR structure (path D) between I/O pad and VDD power line is 1.6 V. The switching voltage of parasitic SCR structure between I/O pad and VSS power line without the substrate-triggered current is ∼3.5 V (by n+/p-well of nMOS junction breakdown), and that of parasitic SCR structure between I/O pad and VDD power line is ∼5.5 V (by p+/n-well of pMOS junction breakdown). The switching voltage of these parasitic SCR structures can be effectively decreased while the substrate-triggered current is increased. Although the switching voltage of these parasitic SCR structures without the substrate-triggered current is lower than that of embedded SCR structure, both SCR structures can be triggered on quickly to discharge ESD current with the appropriate substrate-triggered current generated from the ESD detection circuit.

B. TLP I–V Characteristics

To investigate the device behavior during high ESD current stress, transmission line pulse (TLP) generator with a pulse

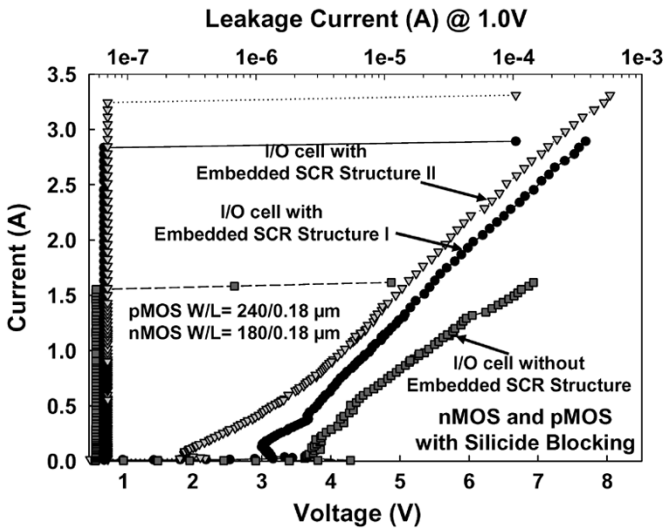

Fig. 13. The TLP-measured *I–V* curves of the input pad under positive-to-VSS ESD stress with or without embedded SCR structure, where the I/O nMOS and pMOS are silicide-blocking but the embedded SCR structures are fully silicided.

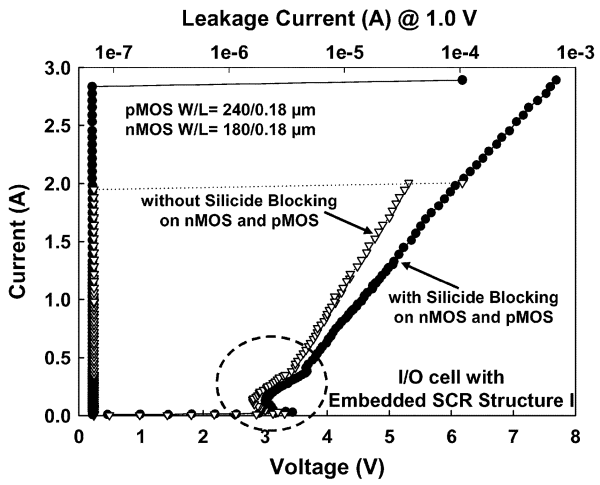

Fig. 14. TLP-measured *I–V* curves of the input pad under positive-to-VSS ESD stress with or without silicide blocking on the input pMOS and nMOS devices, whereas the embedded SCR structures are fully silicided.

width of 100 ns and a rise time of ∼10 ns is used to measure the second breakdown current (It2) of the device [19]. The TLP-measured *I–V* characteristics of the I/O cells with embedded SCR structures under positive VDD-to-VSS ESD stress with or without ESD detection circuit are shown in Fig. 12(a). The enlarged view around the switching point for I/O cells with ESD detection circuit is shown in Fig. 12(b). From the measured results, the switching voltages of embedded SCR structures I and II without ESD detection circuit are 10.5 and 8.8 V, respectively. However, the switching voltages of embedded SCR structures I and II can be reduced to only 2.7 and 1.74 V, respectively, by the ESD detection circuit without involving the avalanche junction breakdown mechanism. Therefore, the switching voltage of embedded SCR structure can be significantly reduced by the substrate-triggered technique to ensure effective ESD protection. The It2 per micron of embedded SCR structure is as high as ∼100 mA/μm, without using the silicide-blocking process modification.

The TLP-measured *I–V* curves of I/O cells with or without embedded SCR structure under PS-mode ESD stress are compared in Fig. 13. Without the embedded SCR structure, the ESD current at the input pad under PS-mode ESD stress is discharged through the silicide-blocking GGNMOS by snapback breakdown. The switching voltage (snapback breakdown voltage) of GGNMOS is 4.3 V, and the It2 of silicide-blocking GGNMOS with dimension $W/L = 180/0.18$ (μm/μm) is 1.6 A. However, the switching voltages of input cell with embedded SCR structures I and II under PS-mode ESD stress are only 3.44 and 2.5 V, respectively. In addition, the It2 of input cell with embedded SCR structure under PS-mode ESD stress can be increased to ∼3 A. From the measured results, the new proposed I/O cells with embedded SCR structure have lower switching voltage, lower clamping voltage level, smaller turn-on resistance, and higher ESD robustness, as compared with the traditional I/O cells. Therefore, the ESD level of the I/O cell can be efficiently improved by inserting the embedded SCR structure in the I/O cell.

The TLP-measured *I–V* curves of the input pad under PS-mode ESD stress with or without silicide blocking on the input pMOS and nMOS devices are shown in Fig. 14. The It2 of the input pad under PS-mode ESD stress with silicide blocking on pMOS and nMOS devices is ∼3 A, and that without silicide blocking is ∼2 A. Whereas the embedded SCR structures are fully silicided in these I/O cells. From the measured *I–V* curves, there is a distinct change of slope in the high current stress region, because the clamping voltage on the pad reaches the triggering voltage of the nMOS to cause a decrease on the turn-on resistance. With smaller turn-on resistance of fully silicided nMOS, the total turn-on resistance of the input pad under PS-mode ESD stress can be effectively reduced by input cell with fully silicided process. But with the fully silicided process, the It2 is dropped because the input nMOS device can sustain less ESD current when the parasitic npn bipolar transistor is triggered on. From the electrical measurements after the input pad under PS-mode ESD stress, the input pad is shorting to ground to indicate that the ESD damages are located at the input nMOS device. Therefore, with lower clamping voltage, the I/O cell with embedded SCR structure II is the design suggestion for the fully silicided process.

The TLP-measured *I–V* curves of the I/O cells with embedded SCR structures I and II under NS-mode ESD stress are shown in Fig. 15. The It2 of input pad under NS-mode ESD stress with embedded SCR structure I is 4 A, and that with embedded SCR structure II is 3 A. The I/O cell with embedded SCR structure I under NS-mode ESD stress has a higher It2 current, because the p+ pickup in the layout with a close-loop ring causes a larger effective turn-on area (parasitic diode of nMOS) for ESD current discharging. For the I/O cell with embedded SCR structure II under NS-mode ESD stress, there is a change of slope at high current stress region. The parasitic npn bipolar transistor of nMOS device is suspected to be triggered on to discharge ESD current from source (collector) to drain (emitter) to cause the decrease on the turn-on resistance.

C. ESD Robustness and Failure Analysis

To verify the ESD robustness of the new proposed ESD protection scheme, the output buffer of pMOS (Mp_out) and nMOS (Mn_out) in the output cell are individually controlled by the input cells, as shown in Fig. 16. The SCR structure is embedded

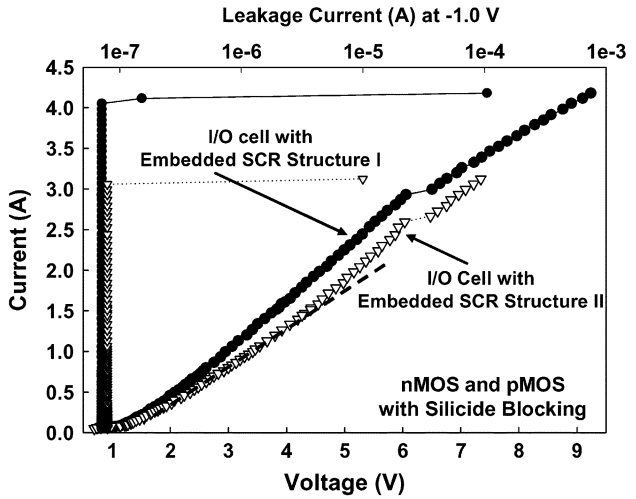

Fig. 15. TLP-measured *I–V* curves of the I/O cells with embedded SCR structures I and II under negative-to-VSS ESD stress.

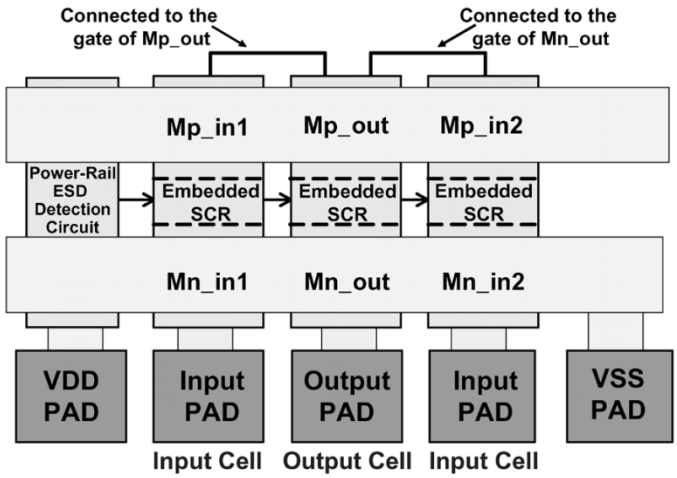

Fig. 16. The testchip to verify ESD robustness of the I/O cells with embedded SCR structures. The output buffer of pMOS (Mp_out) and nMOS (Mn_out) in output cell are individually controlled by the input cells.

in each I/O cell. The human-body-model (HBM) ESD robustness of the new proposed ESD protection scheme with embedded SCR structures I and II under different pin combinations is listed in Table I. The failure criterion is defined as 30% corresponding *I–V* curve shifting at 1-μA current bias. With the embedded SCR structure I, the ESD level of the I/O pads is 4.5 kV, which is dominated by the I/O pad under PS-mode ESD stress. However, the ESD levels of the I/O pads under other modes of ESD stresses are near to or even over 8 kV. The ESD damages of the I/O cells with embedded SCR structure I under PS-mode ESD stress are located at input or output nMOS device. Fig. 17(a) shows the failure location at the input nMOS device for the I/O cells with embedded SCR structure I under PS-mode ESD stress. Although the major ESD current path is discharged through the embedded SCR structure or parasitic SCR structure for the I/O pad under PS-mode ESD stress, the parasitic npn bipolar transistor of input or output nMOS device can be triggered on at high current stress region. However, this

TABLE I
HBM ESD ROBUSTNESS OF THE NEW PROPOSED ESD PROTECTION SCHEME WITH EMBEDDED SCR STRUCTURE IN EACH I/O CELL

ESD Protection Scheme \ HBM ESD Stress	PS-Mode VSS (+)	NS-Mode VSS (-)	PD-Mode VDD (+)	ND-Mode VDD(-)	VDD-to-VSS (+)	VDD-to-VSS (-)
I/O Cells with Embedded SCR I (Input Pad)	5.0kV	7.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR I (Output Pad)	4.5kV	7.75kV	>8kV	>8kV		
I/O Cells with Embedded SCR II (Input Pad)	5.5kV	5.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR II (Output Pad)	5.5kV	5.0kV	>8kV	>8kV		

Silicide Blocking only on nMOS and pMOS
Input/Output pMOS W/L= 240/0.18 (μm) SCR I width= 49.5 (μm)
Input/Output nMOS W/L= 180/0.18 (μm) SCR II width= 45.5 (μm)

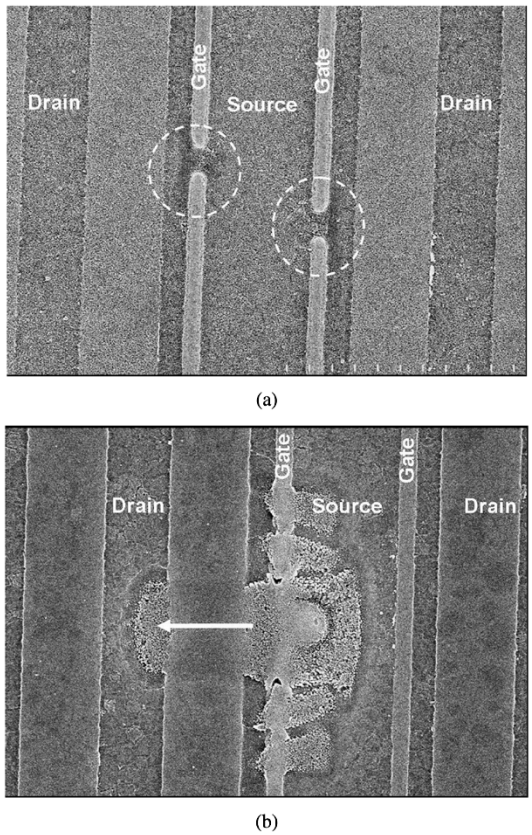

Fig. 17. (a) Failure location at the input nMOS device for the I/O cells with embedded SCR structure I under positive-to-VSS ESD stress. (b) Failure location at the input nMOS device for the I/O cells with embedded SCR structure II under negative-to-VSS ESD stress.

ESD level of such I/O cells is higher enough for safe IC production and field applications. To further improve ESD level, the increase of SCR effective area is a design suggestion.

With the embedded SCR structure II, the ESD level of the I/O pads is 5.0 kV, which is dominated by the I/O pad under NS-mode ESD stress. The I/O pad under NS-mode ESD stress with embedded SCR structure II has a lower ESD level than that with embedded SCR structure I, which has been confirmed by the TLP-measured *I–V* curves in Fig. 15. From the failure

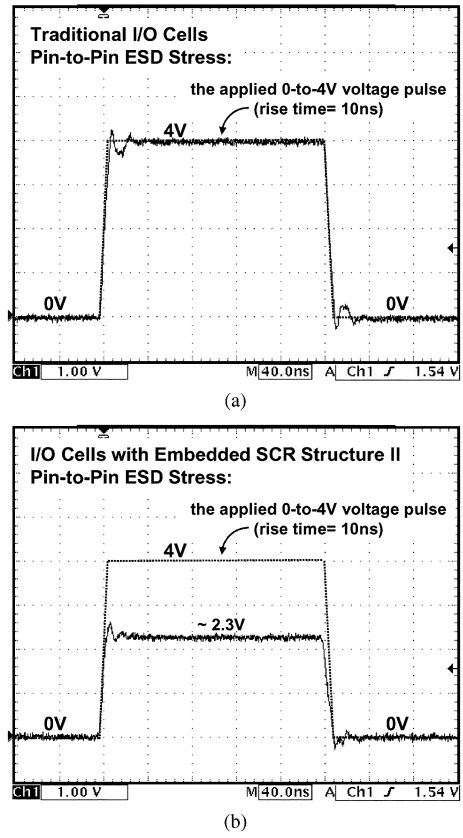

Fig. 18. Measured voltage waveforms on the I/O pads triggered by a 0–4 V voltage pulse with a rise time of 10 ns for (a) the traditional I/O cells, and (b) the new proposed I/O cells with embedded SCR structure II, under pin-to-pin ESD stress condition. (Y axis: 1 V/div., X axis: 40 ns/div.).

analysis, the ESD damages of the I/O cells with embedded SCR structure II under both PS-mode and NS-mode ESD stresses are located at input or output nMOS device. Fig. 17(b) shows the failure location at the center finger of input nMOS device for the I/O cells with embedded SCR structure II under NS-mode ESD stress. From the failure spot in Fig. 17(b), the ESD current is discharged from source (collector) to drain (emitter) to imply that the parasitic npn bipolar transistor of nMOS device is triggered on. Although the parasitic forward-diode path of nMOS device is turned on first, the parasitic npn bipolar transistor of nMOS device is still triggered on at high current stress region. With an ESD level of 5 kV in a small layout area, such I/O cells are very suitable for high-pin-count SOC applications.

D. Turn-On Verification During Pin-to-Pin ESD Stress

To verify the turn-on efficiency of the proposed I/O cells with embedded SCR structure in whole-chip ESD protection scheme, a 0–4 V sharply rising voltage pulse with a rise time of 10 ns is applied to one I/O pad while another I/O pad is relatively grounded (to simulate the pin-to-pin ESD stress condition). The measured voltage waveforms on the I/O pads of traditional I/O cells and new proposed I/O cells with embedded SCR structure II under pin-to-pin ESD stress condition are compared in Fig. 18(a) and (b), respectively. With the traditional I/O cells, the applied 0–4 V voltage waveform is not degraded. It implies that the ESD protection devices in traditional I/O cells cannot be triggered on by the applied voltage pulse. However, with the new proposed I/O cells, the applied 0–4 V voltage pulse can quickly trigger on the ESD protection circuit to cause a degraded voltage waveform in Fig. 18(b) with a clamped voltage level of ~2.3 V. This implies that the embedded SCR structure II or the parasitic SCR structure between I/O pad and VSS power line can be triggered on by the applied voltage pulse. The degraded voltage waveform has verified the effectiveness of the proposed I/O cells with embedded SCR structure to protect the ultrathin gate oxide in nanoscale CMOS process.

IV. Conclusion

An area-efficient ESD protection design for I/O cells in a 130-nm CMOS technology with embedded SCR structures has been proposed and verified. The embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup danger. The turn-on speed of the SCR can be significantly enhanced by the substrate-triggered technique. The ESD discharging paths of the new proposed I/O cells with embedded SCR structures under ESD stresses have been clearly investigated by TLP stress, failure analysis, and turn-on verification. High ESD robustness has been practically achieved in the testchip with the new proposed I/O cells to sustain HBM ESD stress of up to 5 kV in a 130-nm salicided CMOS process. By including the embedded SCR structure as the power-rail ESD clamp device in each I/O cell, one set of high-ESD-robust and high-area-efficient I/O cells have been developed in a 130-nm CMOS technology for system-on-a-chip (SOC) applications.

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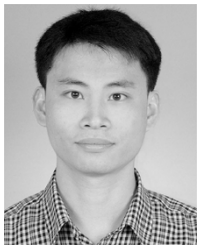

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