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EFFECT OF GE INCORPORATION ON THE PERFORMANCE OF *P*-CHANNEL POLYCRYSTALLINE $Si_{1-x}Ge_x$ THIN-FILM TRANSISTORS

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Abstract—In this study, *p*-channel polycrystalline silicon–germanium thin-film transistors (poly-$Si_{1-x}Ge_x$ TFTs) with different Ge contents in the channel layer were fabricated and characterized. A novel device process was developed to fabricate the test samples. The device structure utilized the *in situ* boron-doped poly-$Si_{0.79}Ge_{0.21}$ with an extremely low resistivity (below 2 mΩ cm) as the source/drain and the undoped poly-Si (or $Si_{1-x}Ge_x$) as the channel layer. It is observed that the addition of Ge atoms in the channel would significantly increase the amount of trap density at grain boundaries thus degrading the device performance. Based on these results, we recommend the use of poly-$Si_{1-x}Ge_x$ source/drain to reduce the contact resistance but do not recommend that it is appropriate to replace poly-Si as the channel material of TFTs.

1. INTRODUCTION

Recently, it was shown by several groups[1–10] that the use of polycrystalline silicon–germanium (poly-$Si_{1-x}Ge_x$) instead of polycrystalline silicon (poly-Si) would significantly reduce the thermal budget of device fabrication. This material has also been utilized for fabricating polycrystalline thin-film transistor (TFTs) below 600°C[3,7–10], showing its potential on the application of active-matrix liquid crystal display (AMLCD) manufacturing. However, these completed devices did not exhibit acceptable performance as comparing to the poly-Si ones thus preventing them from practical usage. In the work of Cao *et al.*[9], they used a low pressure chemical vapor deposition (LPCVD) technique to prepare the poly films and explored the nature of gap states in a hydrogenated poly-$Si_{0.8}Ge_{0.2}$ film. Their results showed that the poly-$Si_{0.8}Ge_{0.2}$ was with a much higher density of gap states than the poly-Si. This led to the degraded device characteristics and was correlated to the lower H-passivation efficiency of Ge dangling bonds, smaller grain size of poly-$Si_{0.8}Ge_{0.2}$ as well as the higher impurity (e.g. O) concentrations contained in the films.

In the present study, we used a novel approach, ultra-high vacuum chemical vapor deposition (UHV/CVD), to deposit the poly-Si and poly-$Si_{1-x}Ge_x$ films and investigated the effect of Ge content on the TFT performance. The ultra-high vacuum chemical vapor deposited poly films are different from those grown using LPCVD with the following properties.

(i) The films are with stable fine grains when deposited at a temperature as low as 550°C [2,3,11,12] and no recrystallizing treatment is required to transform them into the polycrystalline state.
(ii) Grain size of the deposited poly-$Si_{1-x}Ge_x$ films is larger than that of poly-Si ones[12] (see Table 1), which is in contrast to the samples used in the previous work[9].
(iii) The base pressure of this UHV/CVD system is about 10^{-8} torr which is four orders lower than that of LPCVD approach. Such a condition ensures a minimal impurity contamination during deposition[11,13].
(iv) No hydrogenation step was used in this study, so the "intrinsic" properties of the deposited films can be probed.

Meanwhile, in order to get a more clear consequence between the incorporated Ge content in the channel layer and the resulted device performance, we fabricated TFTs with several different Ge contents.

2. DESCRIPTION OF THE UHV/CVD TECHNIQUE FOR DEPOSITING THE POLY FILMS

The UHV/CVD system consists of a growth chamber and a load-lock chamber[2,13]. The load-lock chamber is made of stainless steel while the growth chamber is a quartz tube of 6-inch in diameter, which is capable of 3- to 5-inch Si multi-wafer processing. These two chambers are connected by a gate valve and pumped down separately by their own turbo pumps, which are back supported by mechanical pumps. The pumping speeds of the turbo pumps are 1300 l/s^{-1} and 150 l/s^{-1} for growth chamber and load-lock chamber, respectively. The base pressure in

Table 1. Grain size of the undoped poly films*

Ge fraction, x	Deposition temperature (°C)	Grain size (nm)
0	550	57
0.1	550	98
0.16	550	105
0.21	550	115

*Film thickness of the measured samples is around 200 nm.

the growth chamber is maintained at about 2×10^{-8} torr which contains O_2 and H_2O less than 10^{-9} and 5×10^{-9} torr, respectively, as investigated by the residual gas analyzer (RGA)[13]. Under such a low background pressure, we have found that the oxygen and carbon concentrations in the grown films were below the detection limit of secondary ion mass spectroscopic (SIMS) measurement, which is about 10^{18} and 10^{17} cm^{-3} for oxygen and carbon, respectively. In the standby state, the tube temperature was kept at 550°C all the time.

The flow rates of the reaction gases were controlled by their own mass flow controllers (fully metal-sealed type, TYLAN FC-780 MFC). Pure silane (SiH_4) and 10% germane (GeH_4) in H_2 was used as the source gases for Si and Ge, respectively, while 1% or 100 ppm B_2H_6 in H_2 was used as the doping gas. Each MFC is interfaced to a personal computer for a flexible growth process control via automation.

In this work, the poly films were deposited on 3-inch Si wafers coated with a thermally grown oxide layer. Prior to deposition, the wafers were cleaned in a mixture of H_2SO_4/H_2O_2 (3:1) for 15 min, followed by a 5 min deionized water rinse. Substrates were then blown dry with nitrogen gas and put on a quartz boat inside the loading chamber. After this step, the load-lock chamber was pumped down to a level below 2×10^{-6} torr normally within 30 min. Then, the gate valve was open and the wafers were transferred into the growth chamber via a magnet-coupled linear/rotatory transfer rod. During the transferring process, a hydrogen flow of 600 sccm was introduced into the growth chamber to suppress the contamination from the load-lock chamber.

3. MATERIAL PROPERTIES

With the aforementioned growth conditions, we have demonstrated in our previous publications [2,3,11,12] that this technique is capable of producing both poly-Si and poly-$Si_{1-x}Ge_x$ films with stable fine grains. As Ge atoms were incorporated, the peak locations of X-ray diffraction (XRD) spectra shifted to lower angle values and the amount of shift increased with increasing Ge content. This indicated that Ge incorporated uniformly. Additionally, the undoped poly-$Si_{1-x}Ge_x$ films were found to be with a larger grain size than poly-Si[12] (see Table 1) owing to the high surface mobility of Ge atoms during deposition.

We have also studied the characteristics of boron-doped poly-$Si_{1-x}Ge_x$ films. The results showed that the resistivity of deposited films grown at 550°C can be lower than 2 mΩ cm without further annealing treatment. This is due to the non-equilibrium doping effect[1,2], that is, the effective carrier concentration contained in the films is higher than the solid solubility of dopant. This effect can be resolved with the XRD technique. Figure 1 shows the XRD spectra done on the poly-$Si_{0.79}Ge_{0.21}$ film grown at 550°C with

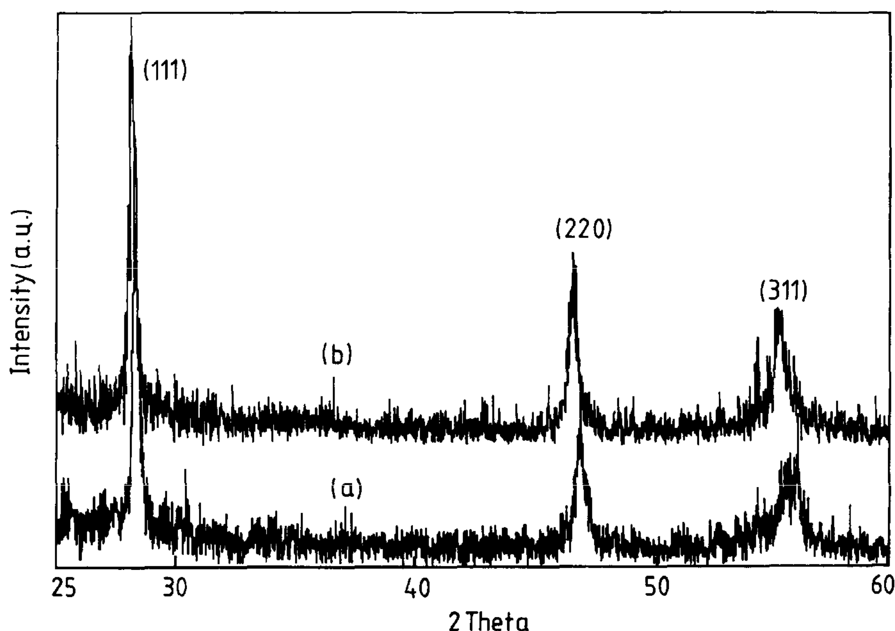

Fig. 1. XRD spectra of a non-equilibrium boron-doped poly-$Si_{0.79}Ge_{0.21}$ film with a carrier concentration of 4.8×10^{20} cm^{-3}: (a) the as-deposited film and (b) after a 900°C 1-h anneal.

a boron concentration of about 2×10^{21} cm^{-3} before and after a 900°C 1-h annealing. It is observed that the peak positions shift to the lower 2θ values after the annealing treatment, implying that the lattice constant is expanded. This is a reasonable result. Under the non-equilibrium doping state, the boron atoms which occupy the substitutional sites of $Si_{1-x}Ge_x$ lattice would result in a smaller average lattice constant because of its smaller covalent radius as compared with those of Si or Ge atoms. Hall measurements showed that the hole concentration decreased from 4.8×10^{20} cm^{-3} for this as-deposited poly-$Si_{0.79}Ge_{0.21}$ film to 1.2×10^{20} cm^{-3} after an above-mentioned high-temperature treatment. After the annealing step, the non-equilibrium boron atoms would precipitate and lead to a larger lattice constant observed in Fig. 1. To our knowledge, this is the first time that the non-equilibrium effect for poly films is clearly identified with the XRD method.

Such low resistivity of *in situ* boron-doped poly-$Si_{1-x}Ge_x$ makes it a potential candidate for low-temperature device fabrication. This way can replace the conventional ion-implantation method to eliminate the long-term activation step. In order to utilize this advantage, we proposed the use of poly-Si/poly-$Si_{1-x}Ge_x$ multi-layers and developed a novel process presented in the next section for TFT fabrication.

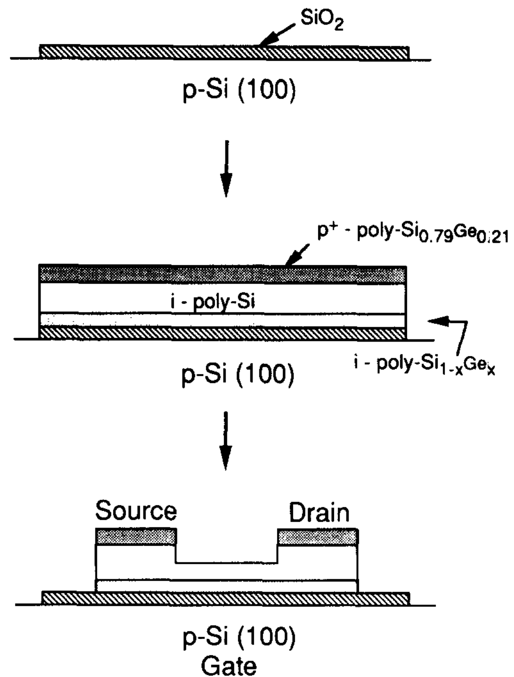

Fig. 2. Process flow of the proposed poly-$Si_{1-x}Ge_x$ TFT fabrication.

4. DEVICE FABRICATION AND CHARACTERIZATION

The main process steps for the proposed TFT process are illustrated in Fig. 2. Device structure is with a bottom-gate configuration. 3-inch p-type Si(100) wafers were used as the starting materials and, for simplicity, as the gate electrode. A 60 nm-thick dry oxide layer was grown on the Si substrates and served as the gate dielectrics. Prior to deposition, the wafers were cleaned in a mixture of H_2SO_4/H_2O_2 (3:1) for 15 min, followed by a 5 min rinse in D.I. water and then spun dry with nitrogen gas. Then, an i-$Si_{1-x}Ge_x$/i-Si/p^+-$Si_{0.79}Ge_{0.21}$ multilayer was deposited sequentially on the gate oxide. All these layers were deposited at 550°C. The i-$Si_{1-x}Ge_x$ was employed as the channel layer and four different Ge contents, namely, $x = 0$, 0.1, 0.16, and 0.21, were used for this study. In the mean time, the i-Si acted as a buffer layer for allowing p^+-$Si_{0.79}Ge_{0.21}$ to be etched selectively on. Thickness of the gate oxide is 60 nm. Other detailed structural parameters are given in Table 2. The p^+-$Si_{0.79}Ge_{0.21}$ layer is with carrier concentration and thickness of 4.8×10^{20} cm^{-3} and 36 nm, respectively. The sheet resistance of the as-deposited films is 450 ± 20 Ω/square. Cross-sectional TEM micrographs of the deposited i-Si/p^+ $Si_{0.79}Ge_{0.21}$ and i-$Si_{0.79}Ge_{0.21}$/i-Si/p^+-$Si_{0.79}Ge_{0.21}$ are shown in Fig. 3(a, b), respectively. As can be seen in the two pictures that the one used for poly-Si TFT fabrication [Fig. 3(a)] is with a relatively smaller grain size as comparing to the other sample [Fig. 3(b)]. This is consistent with the observation shown previously[12]. As a consequence, the undoped poly-$Si_{1-x}Ge_x$ channel layers with a larger grain size would act as the seed for subsequentially grown undoped poly-Si layer, making the interface between the two unclear. The larger grain size also leads to the rougher surface morphology of the deposited films.

Following the film deposition, source and drain regions were defined by a photomask and then etched in a $HNO_3:CH_3COOH:HF = 20:40:1$ solution. The etching rate ratio for boron-doped poly-$Si_{0.79}Ge_{0.21}$ with respect to undoped poly-Si films is over 10. After these steps, active regions were then defined by dry etching, and followed by low-temperature oxide (LTO) passivation, contact hole definition, and Al metallization steps. Finally, a 30-min sintering

Table 2. Structural parameters for poly-Si and poly-$Si_{1-x}Ge_x$ TFTs used in Fig. 2

	Poly-$Si_{1-x}Ge_x$ TFT	Poly-Si TFT
Gate oxide	60 nm	60 nm
Channel layer	50 nm ($x = 0.1$, 0.16, and 0.21)	250 nm
Undoped poly-Si buffer layer	200 nm	*
P^+ poly-$Si_{1-x}Ge_x$ Layer	36 nm	36 nm

*The channel layer of poly-Si TFTs was also used as the undoped poly-Si buffer layer.

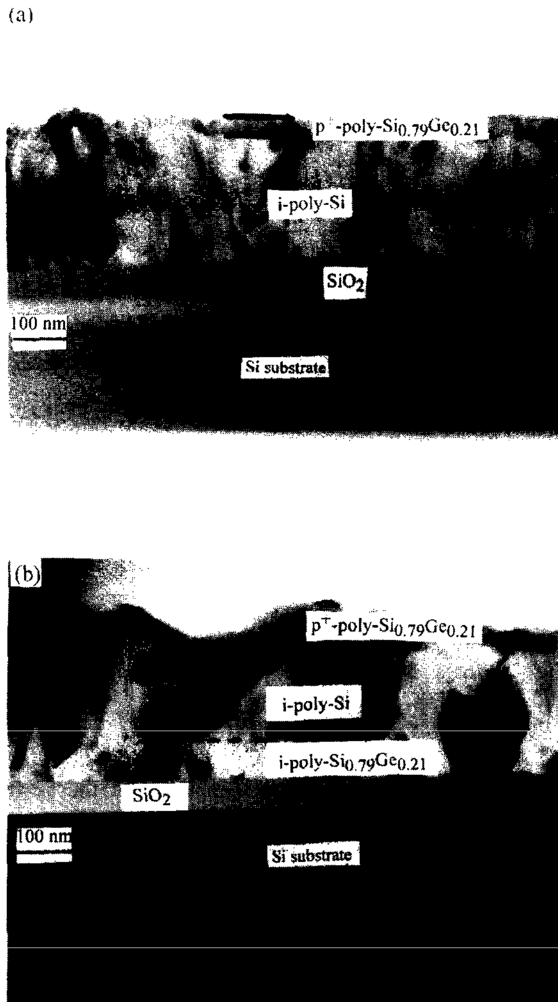

Fig. 3. Cross-sectional TEM micrographs of (a) i-poly-Si/p^+-poly-$Si_{0.79}Ge_{0.21}$, and (b) i-poly-$Si_{0.79}Ge_{0.21}$/i-poly-Si/p^+-poly-$Si_{0.79}Ge_{0.21}$ multilayers deposited on a 60 nm-thick oxide layer.

treatment was given at 400°C, which is the highest temperature step after the deposition of poly films.

Current–voltage characterization was performed using an HP4145B parameter analyser. It should be noted that throughout these processes stated above, no post treatments, such as recrystallization, post-ion-implantation annealing, or hydrogenation, were imposed on the films after deposition. Therefore, the intrinsic electrical properties of the as-deposited films can be evaluated directly via the performance of the completed devices.

5. RESULTS AND DISCUSSION

Typical drain current vs gate voltage characteristics exhibited by the four types of TFTs with different Ge contents in the channel layer are shown in Fig. 4. These measured devices are with identical channel length and width of 140 and 120 μm, respectively.

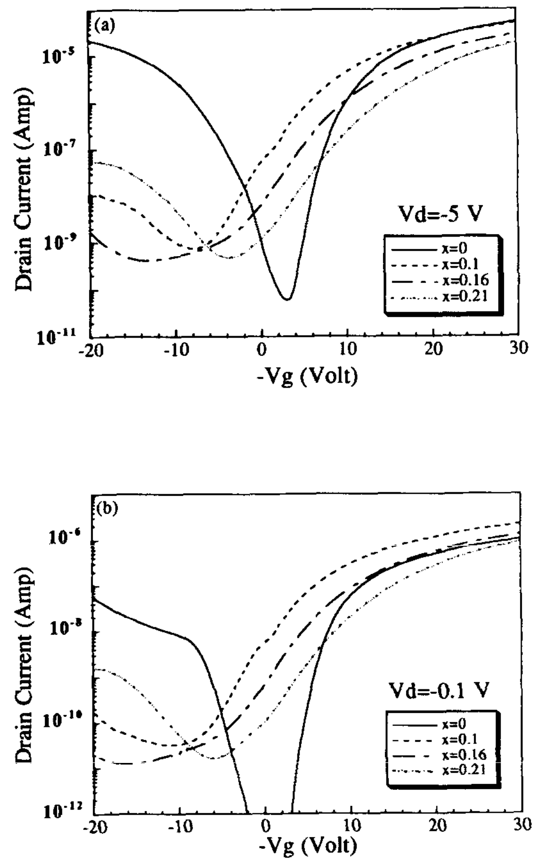

Fig. 4. Subthreshold characteristics of TFTs with different Ge contents in the channel measured at (a) $V_{ds} = -5$ V and (b) $V_{ds} = -0.1$ V.

The drain voltages (V_{ds}) used are −5 and −0.1 V in Fig. 4(a, b), respectively. Output characteristics of these devices are shown in Fig. 5. The field effect mobility is evaluated in linear region at $V_{ds} = -0.1$ V with maximum transconductance. Detailed summary of these characteristics is given in Table 3.

The large amount of trapping states contained at the grain boundaries is essential in influencing the electrical characteristics of poly-Si films and makes the conduction behavior of poly-Si TFTs significantly different from that of Si MOSFETs[14]. It is known that the carrier-trapping model[15–17] is a simple but

Table 3. Typical characteristics of the poly-Si and poly-$Si_{1-x}Ge_x$ TFTs. The channel width and length are 120 and 140 μm, respectively

Ge content in channel (at.%)	0	10	16	21
Threshold voltage (V)*	−11.6	−7.6	−12.6	−16.7
Field effect mobility ($cm^2\ V^{-1}\ s^{-1}$)*	19	13	9	6
Subthreshold swing (V decade^{-1})*	0.77	3	2.9	3.6
On–off current ratio ($\times 10^5$)†	9	0.7	0.8	0.4
Density of trapping states ($\times 10^{12}\ cm^{-2}$)*	5.3	9.8	10.7	12.6

*Measured at $V_{ds} = -0.1$ V.
†Measured at $V_{ds} = -5$ V.

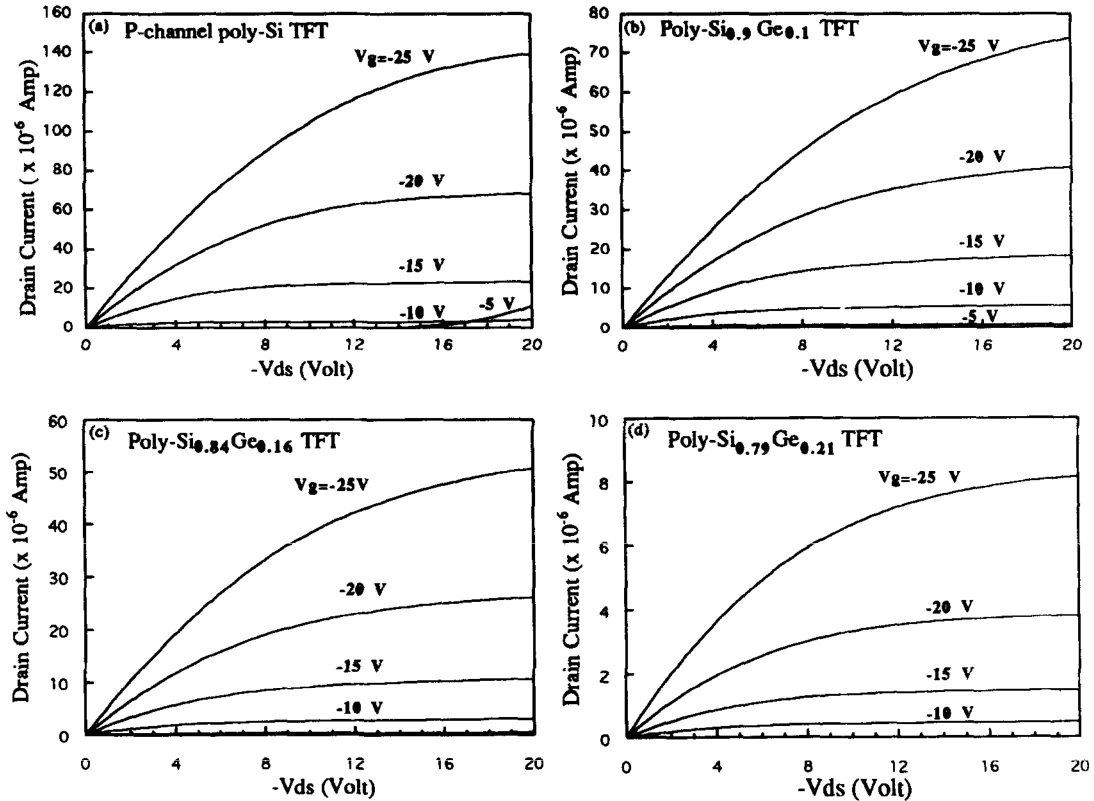

Fig. 5. Drain current vs drain voltage characteristics for (a) poly-Si, (b) poly-$Si_{0.9}Ge_{0.1}$, (c) poly-$Si_{0.84}Ge_{0.16}$ and (d) poly-$Si_{0.79}Ge_{0.21}$ TFTs.

efficient way in describing the conduction behavior of carriers in polycrystalline materials. The potential barrier created by the trapping states is related to the difference in carrier concentration between the grains and the grain boundaries. For a TFT operation, the variation of gate voltage would modulate the carrier concentration inside the conduction channel and, thus, the barrier height at grain boundaries. Based on the method proposed by Levinson *et al.*[18] and modified by Proano *et al.*[19], we can estimate and compare the magnitude of the density of grain-boundary trapping states (N_t) from the current–voltage characteristics.

Value of N_t for the poly-Si TFT is about $5.3 \times 10^{12}\ cm^{-2}$. This is very close to the value shown in our previous study[20] ($4.7 \times 10^{12}\ cm^{-2}$) which was extracted from the relationship between resistivity and carrier concentration using the carrier-trapping model. In Fig. 4, the poly-Si TFT exhibits an on/off current ratio of about 10^6 at $V_{ds} = -5$ V and the maximum field-effect hole mobility of $19\ cm^2\ V^{-1}\ s^{-1}$ in the linear region evaluated at $V_{ds} = -0.1$ V. It should be noted that these electrical characteristics are difficult to be achieved for other approaches without any post-treatment. The superior device performance obtained by us is attributed to the high-quality poly films deposited with the UHV/CVD system. The magnitude of the field-effect mobility and the on–off current ratio have been found to be closely related to the strain-bond tail states[21]. As mentioned in Section 2 that the impurity levels, such as the oxygen and carbon atoms, contained in the deposited poly films were below the detection limit of SIMS measurement. This is in strong contrast to that grown with conventional LPCVD techniques [9,22,23]. We believe that this low-level impurity contamination would result in a low density of tail states, which accounts for the high field-effect mobility and high on–off current ratio achieved in this work.

On the other hand, the addition of Ge in the channel would introduce an additional amount of N_t. The values of N_t for poly-$Si_{1-x}Ge_x$ TFTs are around or higher than $10^{13}\ cm^{-2}$. This implies that the Ge incorporation in the channel layer would degrade the device performance. As observed in Fig. 4 and Table 3, the subthreshold swing and on–off current ratio become worse for the TFT with a higher Ge content in the channel layer. This is obviously due to the larger amount of N_t introduced with the Ge incorporation.

A similar trend also occurs to the case of field-effect mobility. This is seen in Fig. 6 in which the field-effect mobility is shown as a function of Ge content in the channel layer. Over 20 devices were measured for each type of TFT to confirm this trend. Although the incorporation of Ge atoms would enlarge the grain size significantly, as shown in Fig. 3, but the

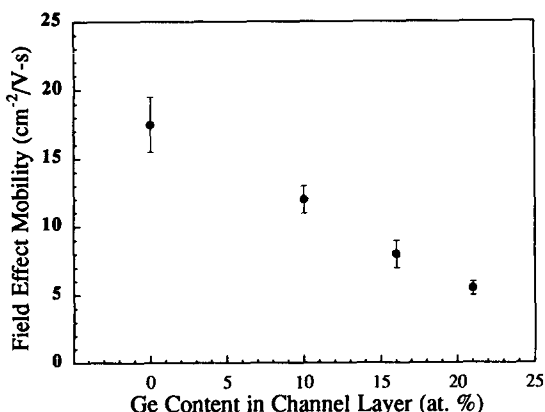

Fig. 6. Field-effect mobility of the completed TFT devices as a function of the GE content in the channel layer.

field-effect mobility decreases with increasing Ge content owing to the higher N_t value. These observations indicate that the "intrinsic" material properties of poly-$Si_{1-x}Ge_x$ are not good enough to replace poly-Si as the channel layer of TFT devices. However, the causes of more trapping centers for poly-$Si_{1-x}Ge_x$ films are complicated since the alloy composition and require more investigations to understand. More detailed identifications about the distribution of trapping states inside the gap using the field-effect conductance method are getting underway and will be presented in the next report.

The threshold voltage is defined as the intercept of linear drain current with the axis of gate voltage. Figure 7 plots the threshold voltage as a function of the channel Ge content. When the Ge atoms were incorporated, the absolute value increases with increasing Ge content. This is mainly related to the higher amount of N_t contained in the device with a higher Ge content in the channel[24]. On the other hand, though the undoped poly-Si films are with a much lower N_t value as compared with the poly-$Si_{1-x}Ge_x$ ones, the absolute value of threshold voltage for poly-Si TFT is smaller than and comparable to the poly-$Si_{0.9}Ge_{0.1}$ and poly-$Si_{0.84}Ge_{0.16}$ TFTs,

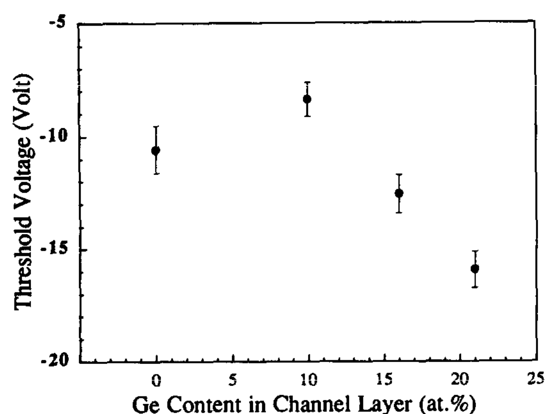

Fig. 7. Threshold voltage of the completed TFT devices as a function of the Ge content in the channel layer.

respectively. This observation is presumably caused by the different nature of oxide fixed charge between the two cases. Referring to several recent works [25,26], a considerable amount of negative fixed charge presented at the oxide/$Si_{1-x}Ge_x$ interface was identified using the capacitance–voltage (C–V) measuring technique. These charges are of opposite sign to that found at oxide/Si interface[27] would explain the results shown in Fig. 7.

6. CONCLUSIONS

In this report, we present a novel process for fabricating poly-Si and poly-$Si_{1-x}Ge_x$ TFTs at low temperatures (below 550°C) and investigated the effect of Ge incorporation in the channel layer on the performance of the completed devices. Our work reveals that the incorporation of Ge in the channel layer of polycrystalline TFTs would introduce a large amount of trapping states at the grain boundaries. This would degrade on–off current ratio, subthreshold swing and field-effect mobility of the completed devices. Our findings indicate that the poly-$Si_{1-x}Ge_x$ films are not appropriate to be used as the channel layer.

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