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Low Distortion and Swing Suppression Sigma-Delta Modulator with Extended Dynamic Range Scheme

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Abstract. This work presents a new low distortion and swing suppression second order sigma-delta modulator with extended dynamic range scheme. The proposed modulator is based on the dual-quantizer architecture and can effectively extend the dynamic range by only adding two simple digital filters in the digital circuit. The techniques of low distortion and swing suppression integrator designs are also employed in the new architecture. Accordingly, this new architecture can improve the circuitry nonlinearity, and the in-band noise can be significantly suppressed to achieve a high resolution in mid or wide bandwidth applications. A second order SDM for Bluetooth application with bandwidth of 500 KHz and sampling frequency of 40 MHz was designed and implemented. The peak SNDR of the experimental SDM is 78 dB.

Key Words: analog-to-digital converter, blind on-line calibration, dual-quantizer, dynamic range, low distortion, sigma-delta modulator, swing suppression, wide bandwidth

1. Introduction

The oversampling sigma-delta analog-to-digital converters (ADCs) have significantly impacted applications in communications, measurement, and data-acquisition, due to their ability to deliver high resolution from untrimmed analog circuits with modest complexity [1]. Importantly, sigma-delta modulator (SDM) ADCs can achieve high-resolution signal conversion without high precision component matching, as required by the conventional signal converters such as flash type A/D converters or those A/D converters based on sub-ranging or successive approximation techniques [1]. However, the sigma-delta modulators are normally limited to low or mid bandwidth applications due to their over-sampling nature. Sigma-delta modulation can be designed by several types of architectures such as single-loop, cascaded, feed-forward summation [2], distributed feedback, . . . , etc. [1].

With the improvement of VLSI technologies, SDM is becoming attractive for use in mid or wide bandwidth applications, such as xDSL modems and wireless wideband transceivers. However, at the low oversampling ratio (OSR) required for such applications, the SDMs are increasingly sensitive to circuit imperfections, and thus require high-order or multi-bit architectures [1]. In this work, a new second order sigma-delta modulator with extended dynamic range (DR) scheme is proposed. This architecture is accomplished by a dual-quantizer approach [3]. The quantizers are in multi-bit architecture, but the feedback of the SDM is a single bit DAC (digital-to-analog converter). The analog circuit complexity and imperfections of this architecture can be effectively improved to the same performance as that of the multi-bit architecture. The technique is applicable even for low OSR SDMs and can simplify the circuit implementation. Moreover, the techniques of low-distortion and swing-suppression integrator design are also proposed. According to the simulation results, this new SDM architecture is well suited for wide bandwidth applications such as Bluetooth, xDSL and others. A SDM for Bluetooth application with bandwidth of 500 KHz and sampling frequency of 40 MHz was designed and implemented to verify the proposed architecture. The performance of the designed SDM is as expected.

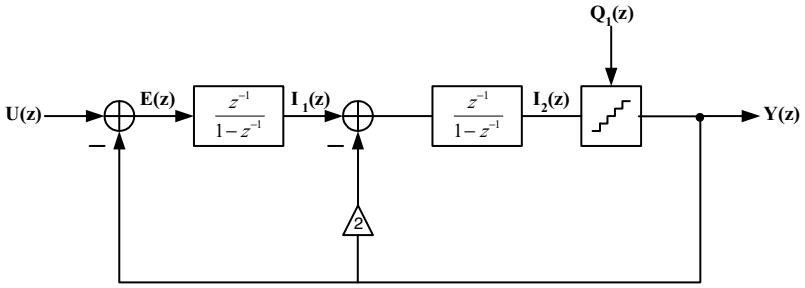

Fig. 1. The conventional topology of a second-order SDM.

The rest of this paper is organized as follows. Section 2 describes the conventional SDM architecture. Section 3 introduces the proposed SDM architecture. Section 4 then presents the circuit design of the proposed SDM architecture. Section 5 presents the comparisons and simulation results. Conclusions are finally made in Section 6. The digital correction method, digital blind on-line calibration technique, is described in Appendix A.

2. Conventional Sigma-Delta Modulators

2.1. Distortion in the Conventional Topology

Figure 1 shows the topology of a conventional second-order SDM. In this architecture, the linear model of the SDM includes two inputs. One is the actual input $U(z)$, and the other is the quantization noise, $Q_1(z)$. Two transfer functions, the signal transfer function (STF) and the noise transfer function (NTF), are given by

$$Y(z) = U(z)STF + Q_1(z)NTF, \tag{1}$$

where $STF = z^{-2}$ and $NTF = (1 - z^{-1})^2$. However, in practice, the transfer function of the integrator is different from (1) due to the influence of the non-idealities of the electrical implementation. Considering the implementation by the leaky integrators, the transfer function with finite amplifier dc gain is given by

$$H(z) = \frac{1}{1 - (1 - \mu)z^{-1}}, \tag{2}$$

where $\mu = 1/A_v$ and A_v is the finite amplifier dc gain. For this case the transfer function of the output of the second-order sigma-delta modulator becomes approximately

$$Y(z) \cong z^{-2}X(z) + [(1 - z^{-1})^2 + 2\mu z^{-1}(1 - z^{-1}) + \mu^2 z^{-2}]Q_1(z). \tag{3}$$

In the bracket, the first term is an ideal second-order shaped function; the second term is the first order shaped error, and the third term is the unshaped quantization error. The second and third terms are extra quantization errors, and the extra quantization power, $\Delta P_Q(\mu)$, is injected into the SDM. The resulting baseband quantization noise power can be expressed as

$$P_Q(\mu) = P_Q + \Delta P_Q(\mu) \cong \frac{\Delta^2}{12}\left[\frac{\pi^4}{5(OSR)^5} + \frac{2\mu^2\pi^2}{3(OSR)^3} + \frac{\mu^4}{(OSR)}\right]. \tag{4}$$

The factor, OSR, is oversampling ratio, and Δ equals the difference between the two adjacent quantization levels. The extra error term, $\Delta P_Q(\mu)$, depends on μ and grows with the order of the modulator. In order to reduce the nonlinearity distortion, a high OSR is usually applied in this architecture to minimize the $\Delta P_Q(\mu)$ effects, and therefore the input signal bandwidth is restricted to low or mid bandwidth applications.

2.2. Integrator Output Swing in the Conventional Topology

A large amplitude signal, which is the sum of the input signal and quantization noise, is usually integrated into the integrator of the oversampling SDM. The large output swings of the integrator may not only cause the nonlinearity of the opamp but also limit the power supply

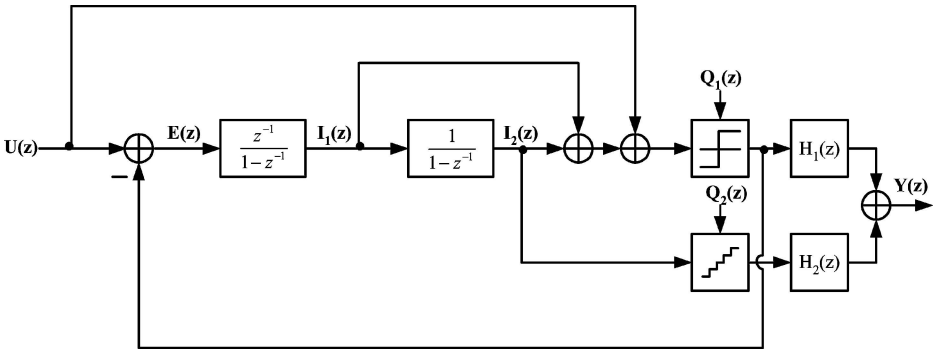

Fig. 2. The proposed topology of a second-order SDM.

voltage of the analog circuit. Scaling techniques have been proposed to overcome this problem [1], but these techniques also reduce the dynamic range of the modulator. In this work, a swing suppression topology is proposed to improve these problems.

2.3. Wideband Architecture in the Conventional Topology

By the continuing advancement of the VLSI technology, the SDM is attempted to be applied in wide bandwidth applications [4–7]. Due to the low OSR requirement of the wideband applications, both the order of the modulator and the bit number of the internal quantizer have to be increased to achieve the desired resolution in the desired frequency band. The architectures of high-order single-bit, low-order multi-bit, or MASH may solve this problem [1]. However, the complexity of the analog circuit and the stability problems limit the performance of the high-order single-loop architecture. In the low-order multi-bit architecture, the DAC mismatch seriously degrades the overall performance and the dynamic element matching technique is applied to improve this degradation. The MASH architecture can cascade several low-order stages to achieve high-order performance, but the imperfect cancellation between analog and digital circuits may cause the leakage noise to degrade the performance. In this work, a dual quantizer architecture is proposed. By our approach, a one-bit DAC is used in the feedback loop, and thus the multi-bit DAC mismatch problems are avoided but the performance is still good enough. The details are discussed in next section.

3. Proposed Topology

Figure 2 shows the proposed second-order dual quantizer SDM and it is similar to the architecture proposed by Silva and Temes [8]. In this SDM, the transfer functions of the two integrators are different. The first integrator is a conventional integrator, but the transfer function of the second integrator is $\frac{1}{1-z^{-1}}$. In this topology, the gains of the forward paths are unity, and therefore the value of capacitors is less than Silva's topology in [8]. Besides the two integrators, there are two quantizers, the low-bit quantizer $Q_1(z)$ and the high-bit quantizer $Q_2(z)$. $H_1(z)$ and $H_2(z)$ are digital filters, $H_1(z) = z^{-1}$ and $H_2(z) = (1 - z^{-1})^2$, and they are used to extend the dynamic range. The details of $Q_1(z)$, $Q_2(z)$, $H_1(z)$, and $H_2(z)$ are discussed in the following subsections.

3.1. Proposed Low-Distortion Topology

Figure 1 shows a conventional second order SDM, however as mentioned in Section 2.1 it has serious nonlinearity distortion problems. In order to overcome the nonlinearity distortion problems, a high OSR is usually applied in this architecture, and therefore it is restricted to low or mid bandwidth applications. When carefully analyzing the signal flows of Fig. 1, we can find the error signal $E(z)$ is the difference between the input signal $U(z)$ and output signal $Y(z)$, and the noise-shaping mechanism of Fig. 1 tries to minimize the difference in the desired frequency band. The STF is a delay version of the input signal and it causes $E(z)$ to restore the integrator outputs, $I_1(z)$ and $I_2(z)$. When the effects of the nonlinear amplifier DC-gain, slew rate limitation, and incomplete setting noise are considered, the harmonic

components of the input signal can be created at the integration outputs, $I_1(z)$ and $I_2(z)$ [8]. Medeiro and Perez-Verdu [9] reported that the non-linear amplifier open-loop gain, A_v, whose dependency on the output voltage (v) could be approximated by a polynomial function, $A_v = A_0(1 + \gamma_1 v + \gamma_2 v^2 + \cdots)$. Where A_0 is the dc gain with zero output voltage, γ_1 and γ_2 are the first and second order deviating coefficients respectively. Thus, the harmonic distortion of the SC integrator caused by a nonlinear dc gain can be modified as [9]

$$v_o(n) \cong v_o(n-1) + g_1\left[v_i(n-1) - \frac{v_i(n-1) + v_o(n)}{A_0} + \gamma_1 v_o(n)\frac{v_i(n-1) + v_o(n)}{A_0} + \gamma_2 v_o^2(n)\frac{v_i(n-1) + v_o(n)}{A_0}\right], \quad (5)$$

where v_i and v_o are the input and output of the SC integrator respectively. The equivalent distortion at the integrator input can be estimated by analyzing the harmonics in brackets in (5). If the input and output of the integrator are approximated by their first harmonic,

$$v_i \cong V_i \sin(2\pi f_b n T_S) \quad v_o \cong V_o \cos(2\pi f_b n T_S) \quad (6)$$

where f_b is the frequency of the input and T_S is the sampling period. Substituting the expressions in (5) and performing a Fourier series expansion of those terms in the bracket, the amplitudes of the second and third harmonics referred to the integrator input are [9]:

$$A_{H,2} = \frac{|\gamma_1|}{2A_0} V_o \sqrt{V_i^2 + V_o^2}$$
$$A_{H,3} = \frac{|\gamma_2|}{4A_0} V_o^2 \sqrt{V_i^2 + V_o^2} \quad (7)$$

According to equations (7), the harmonic distortion grows with the amplitudes of V_i and V_o. For this reason the input signal $U(z)$ can be cancelled out from $I_1(z)$ and $I_2(z)$, and this can reduce the output swing of the integrator. Therefore, the amplitudes of V_i and V_o can also be minimized to reduce the harmonic distortions. Based on this function, a new SDM architecture is proposed and is shown in Fig. 2. The STF and NTF of this SDM are given as follows:

$$STF(z) = 1, \quad (8)$$
$$NTF(z) = (1 - z^{-1})^2. \quad (9)$$

Under this architecture, the STF is unaffected, but the integrators only process the quantization noises, and the performance requirements of the integrators can be significantly relaxed. Both Figs. 1 and 2 are simulated with a sampling frequency of 40 MHz and the input signal is a sine wave of frequency 200 KHz with -6 dB amplitude and two 2-bit quantizers are used. Figure 3 shows the spectra of $I_1(z)$ and $I_2(z)$ of both architectures. Obviously the distortions in $I_1(z)$ and $I_2(z)$ of the proposed architecture are reduced significantly.

3.2. The Proposed Swing-Suppression Topology

The proposed architecture has the characteristic of swing suppression. As discussed in Section 2.2, the integrator output swing should be reduced to avoid the nonlinearity and overload in the low power supply voltage SDM. The transfer functions of $I_1(z)$ and $I_2(z)$ in Fig. 1 are expressed as [10]:

$$I_1(z) = (1 - z^{-1})z^{-1}U(z) + (1 - z^{-1})z^{-1}Q_1(z), \quad (10)$$

and

$$I_2(z) = z^{-2}U(z) + (-2z^{-1} + z^{-2})Q_1(z). \quad (11)$$

Furthermore, the transfer functions of $I_1(z)$ and $I_2(z)$ in Fig. 2 are derived as:

$$I_1(z) = -(1 - z^{-1})z^{-1}Q_1(z), \quad (12)$$

and

$$I_2(z) = -z^{-1}Q_1(z). \quad (13)$$

From equations (10) to (13), $I_1(z)$ and $I_2(z)$ (equations (10) and (11)) of Fig. 1 contain both input signal, $U(z)$, and quantization noise, $Q_1(z)$, but $I_1(z)$ and $I_2(z)$ (equations (12) and (13)) of Fig. 2 contain only quantization noise, $Q_1(z)$. Therefore, the integrator output swings of the proposed architecture are smaller than that of the conventional one. The simulated integrator output waveforms of both the proposed and conventional architectures, with a sampling frequency of 40 MHz, a 100 KHz sine wave input with -6 dB amplitude, and with 2-bit quantizers and DAC, are shown in

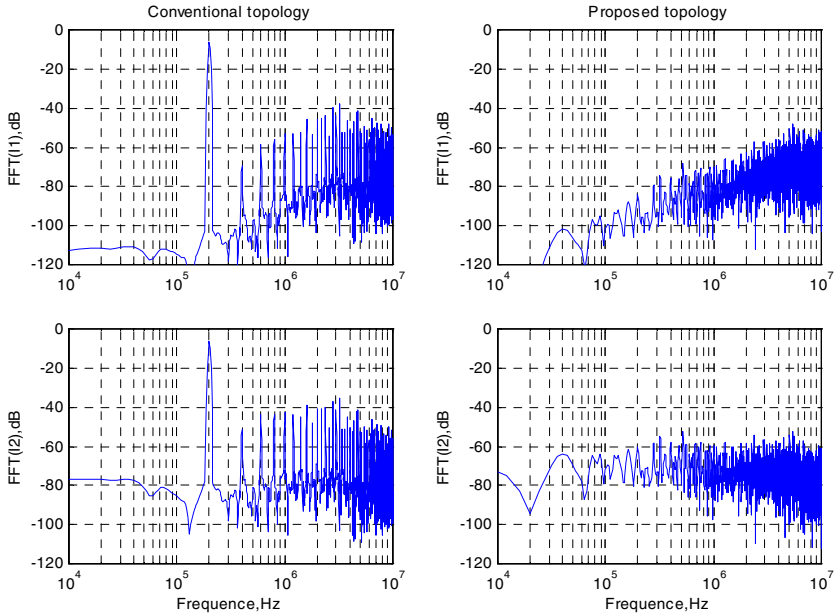

Fig. 3. Distortion simulation of the traditional and proposed architectures.

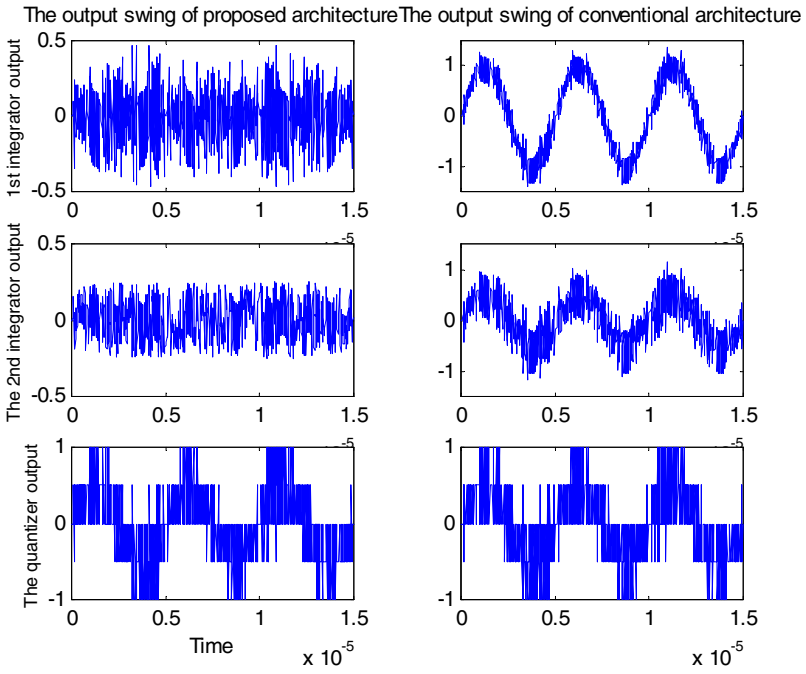

Fig. 4. The output swings of the proposed and conventional architecture.

Fig. 4. According to Fig. 4, the integrator output swings of the proposed architecture are much smaller than that of the conventional architecture. The output swings of conventional SDM are in the range from 1 V to −1 V, but in our architecture, the first integrator output swing is reduced from 0.5 V to −0.5 V and especially the second integrator output swing is reduced from 0.2 V to −0.2 V.

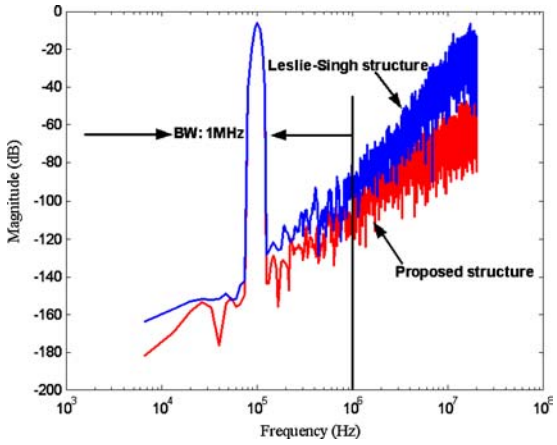

Fig. 5. The output spectrum of the proposed and Leslie-Singh architecture.

3.3. *Proposed Topology with Extended Dynamic Range*

Accordingly, the power of the quantization noise, which is shaped by the second-order high-pass function, can be expressed as [11]:

$$P_{Q_2} \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{1}{OSR^5}\right), \tag{14}$$

where Δ is a quantization step and the relationship of the intervals of the high-bit quantizers between the proposed and the Leslie-Singh architecture can be given by

$$\Delta_P \cong \frac{1}{4}\Delta_L, \tag{15}$$

where Δ_P and Δ_L are the high-bit quantizer intervals of the proposed and the Leslie-Singh architecture, respectively. By equations (14) and (15), the dynamic range of the proposed architecture can be improved by 12 dB compared with that of the Leslie-Singh architecture. Figure 5 shows the output spectra of the proposed and Leslie-Singh architectures. The low- and high-bit quantizers of the architecture are equal to 2-bit and 4-bit, respectively and the sampling rate and bandwidth are equal to 40 MHz and 1 MHz, respectively.

In practice, the transfer functions of $H_1(z)$ and $H_2(z)$ can be realized accurately by a digital circuit, but the exact form of the noise transfer function $NTF(z)$ will depend on the analog components of the low-bit modulator loop. If $NTF(z)$ and $H_2(z)$ cannot be identical, then the leakage noise will be appeared in the output of the modulator and may degrade the performance. Indeed the leakage noise can be reduced and the cancellation technique is discussed in the following subsection.

3.4. *Digital Calibration Techniques*

In practice, the gain error and pole error of the integrator may degrade the performance of the modulator. Consider the non-ideal effects of the proposed second-order modulator, as shown in Fig. 6. α_1, β_1 and α_2, β_2 are the actual gain coefficients and pole coefficients of the first integrator and second integrator in our proposed modulator, respectively. Ideally, the gain and

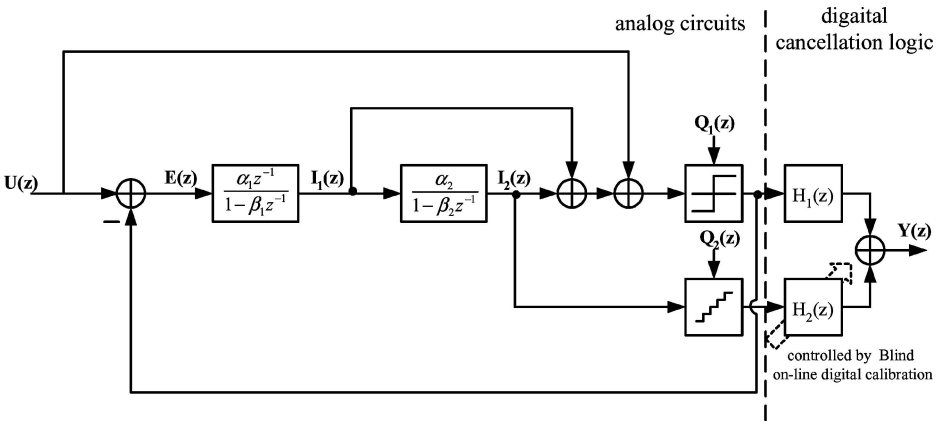

Fig. 6. The linear model of the proposed SDM with gain error and pole error.

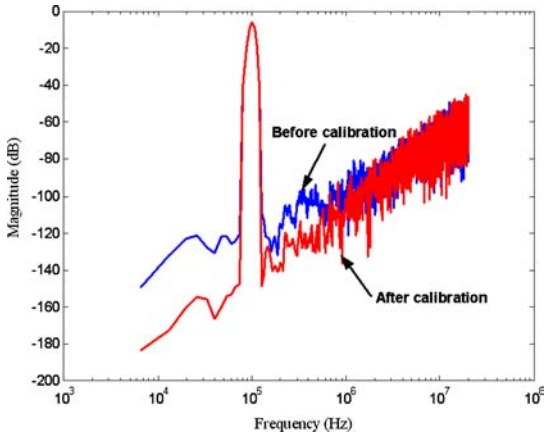

Fig. 7. The output spectrum of the proposed modulator with blind on-line calibration.

pole coefficients of the integrators must equal unity and the low-bit quantization error of the modulator can thus be cancelled by the digital cancellation filter, $H_2(z)$. Unfortunately, the coefficients varying due to the pole and gain errors may cause leakage noise in the modulator output [1]. The digital cancellation filter, $H_2(z)$, must equal the NTF of the modulator to solve this problem, and can be expressed as follows,

$$H_2(z) = \frac{1-\beta_1 z^{-1}}{\alpha_1}\frac{1-\beta_2 z^{-1}}{\alpha_2}. \tag{16}$$

Therefore, the key to the digital correction is a technique to adaptively estimate the digital filter coefficients [12–15]. The blind on-line digital calibration [12] can be used to correct the leakage noise in the modulator output. By the least-square formulation of the calibration, we can modify the coefficients of the digital cancellation filter, $H_2(z)$, and cancel the leakage noise. The detail of the blind on-line calibration is given in Appendix A. Figure 7 shows the output spectra of the proposed SDM with a 2% gain error and a 50 dB finite op-amp gain by using blind on-line calibration.

The effective SNDR of the proposed SDM, obtained by the blind on-line calibration technique as a function of the number of the calibration samples and the relative signal bandwidth $f_n/f_s = 1/OSR$, can be analyzed as follows. A lower bound on the number of samples, L, required for calibration is approximated by [12]

$$\left(1-\frac{1}{OSR}\right)L > n-1, \tag{17}$$

where n is the number of the estimated parameters of $H_2(z)$. The rank of the effective number of the linearly independent calibration samples must exceed the number of the estimated parameters of $H_2(z)$. Simulation results indicate that an excellent performance is obtained with only 256 calibration samples with five-time iterations of the linear regression for the proposed SDM (modulator order = 2, OSR = 40) using blind on-line calibration.

4. Circuit Implementation

Based on the proposed architecture, a SDM for Bluetooth application (BW = 500 KHz) with sampling rate of 40 MHz under 0.25 μm 1P5 M mixed-mode CMOS process was designed and implemented. The digital filter coefficients are calculated by using Matlab tool, and the cancellation logics are not implemented to the circuits. The details of the circuit design are discussed in the following subsections.

4.1. Opamp Circuit Design

The opamp is a key component of the sigma-delta modulators and may affect the performance of the modulators seriously. A fully differential folded-cascode OTA with gain-boosted technique [16] is applied to the proposed modulator and is shown in Fig. 8. Due to the fully differential architecture of the opamp, the common mode feedback circuit (CMFB) must be added. In order to optimize the opamp circuit specifications such

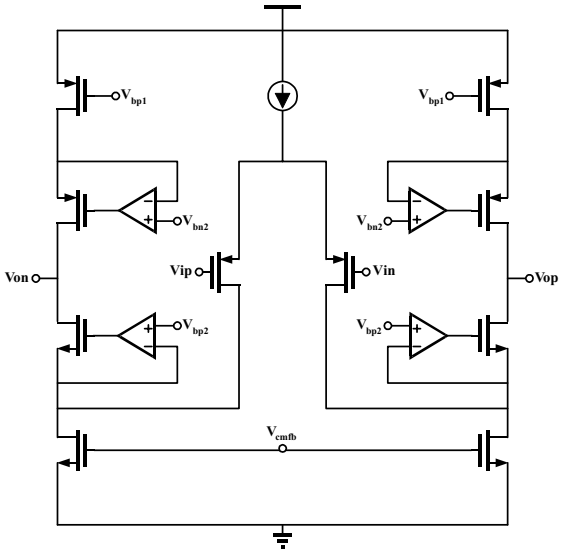

Fig. 8. The gain-boosting folded-cascode OTA.

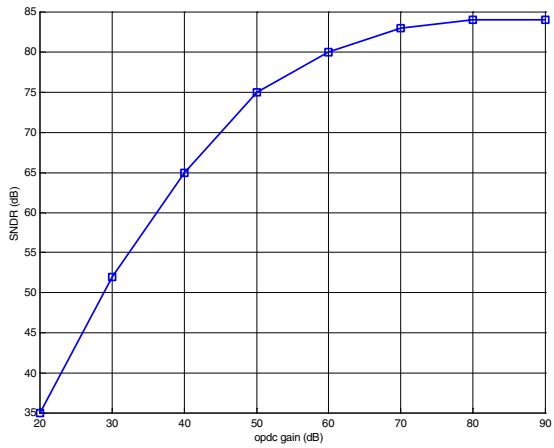

Fig. 9. The SNDR of the proposed modulator versus finite opamp gain.

as dc gain and unity-gain bandwidth . . . etc, the system level simulation is used to obtain the optimum opamp specifications. Figure 9 shows the simulated SNDR as a function of the finite op-amp gain for the proposed SDM with an input magnitude of −6 dB. The key performance parameters for the opamp are summarized in Table 1.

4.2. Comparator and Quantizer Circuits Design

Figure 10 shows the comparator circuit used in the proposed SDM. This comparator has one stage of the pre-amplification followed by a track-and-latch stage, and is suited to the high-speed sigma-delta modulator design [17].

Table 1. Performance summary of the gain-boosted folded-cascode OTA.

Opamp specification	Values
DC gain	72 dB
GBW	300 MHz (@5 pF load)
Phase margin	72 degree
Differential output swing	2.4 V ($V_{dd} = 2.5$ V)
Maximum current	1 mA
Power dissipation	15 mW
Technology	0.25 μm CMOS

The three-level quantizer can be implemented by using two comparators and two logic gates (XOR and AND). Figure 11 shows the schematic of a 1.5-bit (three-level) quantizer circuit. The performance of the modulator is relatively insensitive to the offset and hysteresis in the three-level quantizer because the effects of the impairments are attenuated in the baseband by the second-order noise shaping.

The 4-bit quantizer is implemented by a fully differential flash ADC with 16 parallel comparators and a resister divider to generate the reference voltage of the comparators. Figure 12 shows the schematic of the 4-bit quantizer circuit. The modulator performance is also very tolerant to the nonlinearity and hysteresis

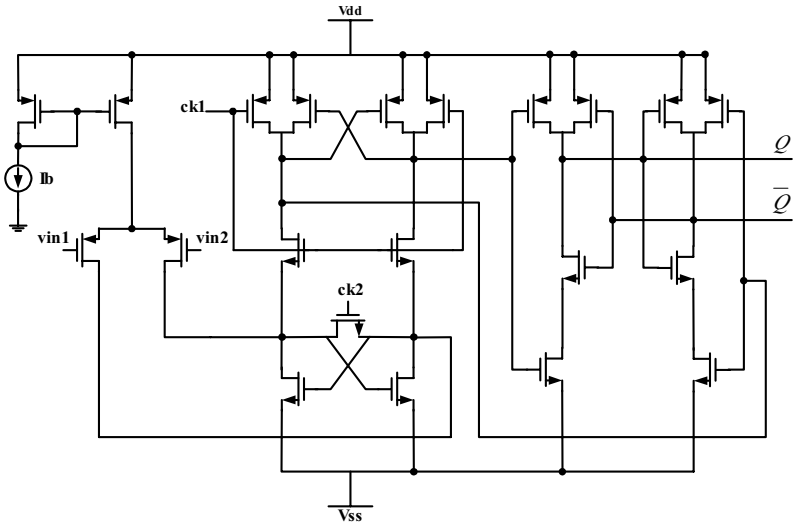

Fig. 10. The comparator circuit of the proposed modulator.

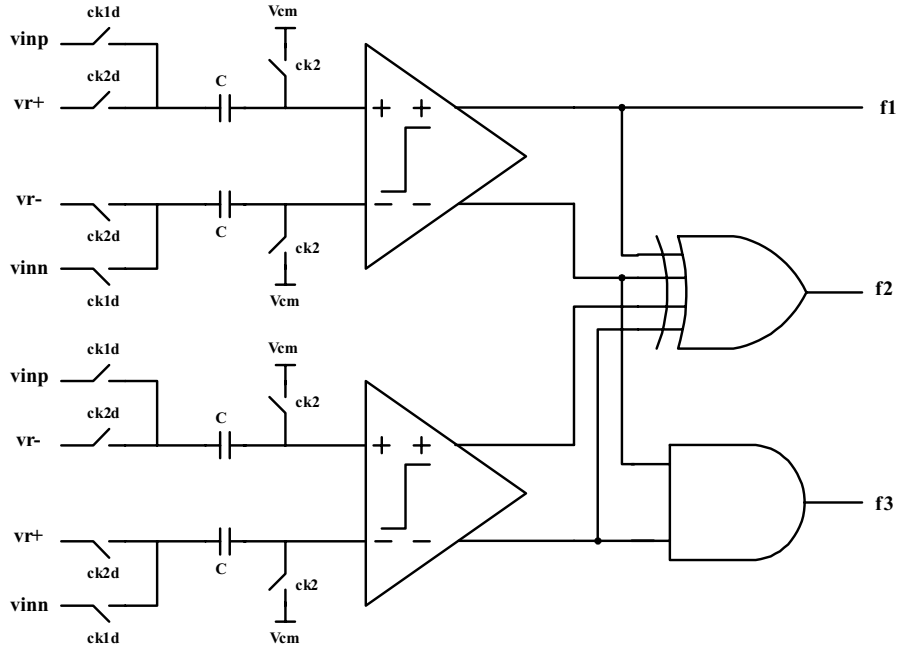

Fig. 11. The circuit schematic of the 1.5-bit (three-level) quantizer.

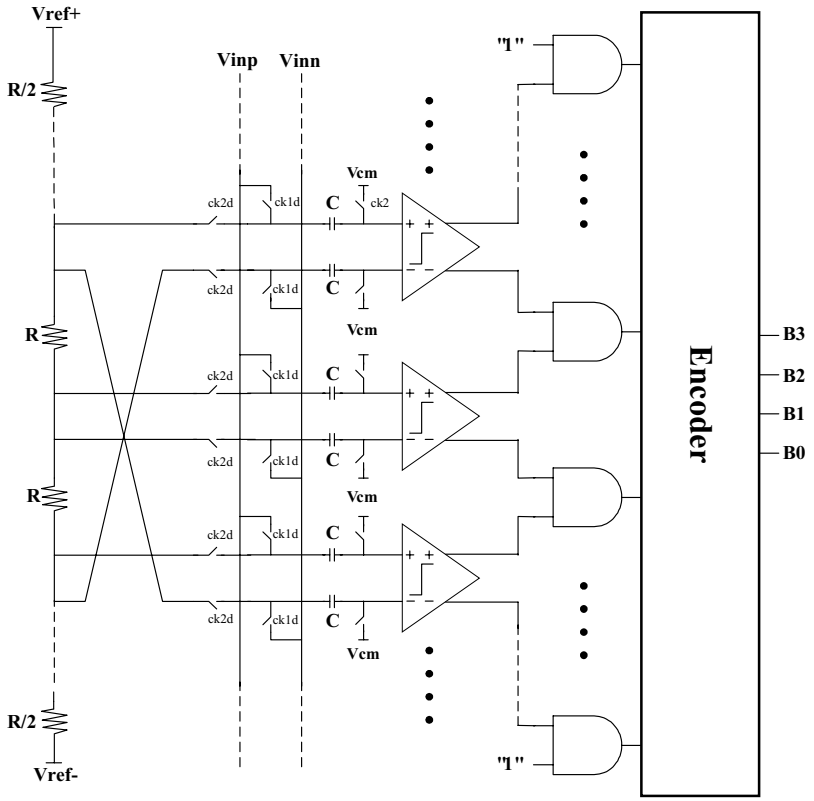

Fig. 12. The circuit schematic of the 4-bit flash ADC.

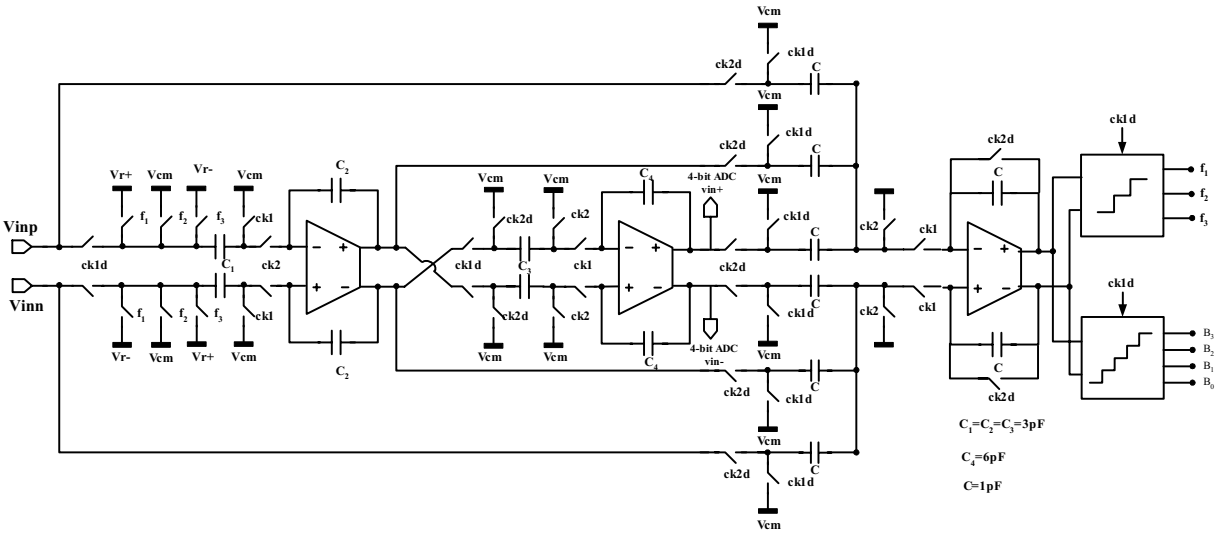

Fig. 13. The circuit diagram implementation of the proposed SDM.

in the 4-bit quantizer because the outputs of the 4-bit quantizer are not in the feedback loop of the modulator.

4.3. Proposed Second-Order Sigma-Delta Modulator

The circuit diagram of the proposed SDM implementation (for simplicity, the 4-bit quantizer circuit is not shown here) is shown in Fig. 13. The switch sizes (W/L) of the nMOS and pMOS are chosen as 10 μm/0.25 μm and 40 μm/0.25 μm respectively to achieve a 150 Ω switch turn-on resistance. The sampling capacitor value is chosen as 3pF to minimize the thermal noise. A three-level quantizer (as shown in Fig. 12) is used instead of the 2-bit quantizer (as shown in Fig. 2) to avoid the DAC mismatch and reduce the analog circuit complexity, but the gain of the second integrator must be equal to 0.5 to avoid the overloading of the integrators. This will cause 6 dB loss of the dynamic range in circuit implementation, but the feedback loop does not need a multi-bit DAC.

The first integrator of the modulator can be implemented by a noninverting SC integrator and has the equivalent transfer function of $\frac{z^{-1}}{1-z^{-1}}$. The second integrator of the modulator can be implemented as an inverting SC integrator and has the equivalent transfer function of $\frac{-0.5}{1-z^{-1}}$. Due to the inverting characteristic of the second integrator, the outputs of the first integrator must be across to the inputs of the second integrator to achieve the positive transfer function of $\frac{0.5}{1-z^{-1}}$. The summing stage of the modulator can be implemented as a SC summing amplifier.

5. Experimental Results and Comparisons

The SDM is implemented in a 0.25 μm, 1-poly 5-metal, CMOS process, operating from a 2.5-V supply. The chip area including bonding pads is 1.29 mm × 1.29 mm and shows in Fig. 14. In the floor

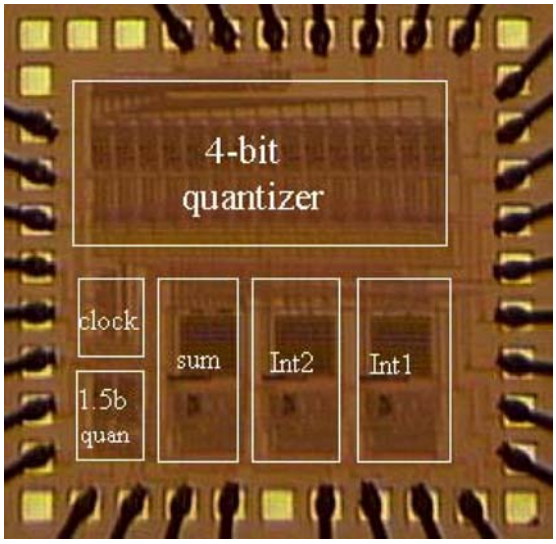

Fig. 14. Chip photomicrograph.

Table 2. Measured results of the experimental SDM.

Parameter	Values
Sampling rate	40 MHz
Signal bandwidth	0.5 MHz
Oversampling ratio	40
Peak SNDR	78 dB
Supply voltage	2.5 V
Power dissipation	56 mW
Technology	0.25 μm, 1P5M, CMOS
Chip area	1.29 mm $\times$ 1.29 mm

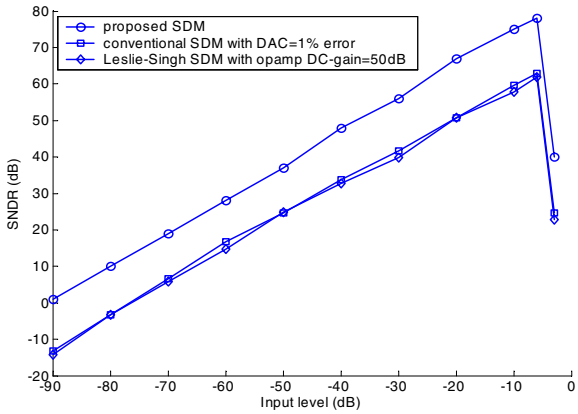

Fig. 16. The SNDR versus input level of the proposed and conventional architectures.

plan, we try to divide the active circuitry into two parts, analog circuit and digital circuit, and give independent power supply voltages. In order to avoid the digital noise coupling, the guard ring and shield techniques are applied to the analog circuit components. By these arrangements, the performance of the modulator can have a better SNDR in the mixed-mode circuit design.

The whole modulator is integrated by the building blocks as mentioned in the above sections. The peak SNDR of the measurement results, which is calculated within a 500 KHz signal bandwidth, is 78 dB. A 32768-point FFT plot of the SDM output spectrum is shown in Fig. 15, where a 100 KHz and a -6 dB input signal is applied. The measurement results are close to that obtained in the circuit simulation. The whole sigma-delta modulator power dissipation is about 56 mW. The measured results of the experimental SDM circuit are shown in Table 2.

The proposed second-order SDM has several advantages compared with conventional SDMs. Firstly, the proposed SDM use a single-bit DAC in the feedback loop, but the performance is still as good as that of the multi-bit SDM. This advantage can avoid the effects of the DAC mismatch, and reduce the circuit complexity. Secondly, the proposed SDM can improve

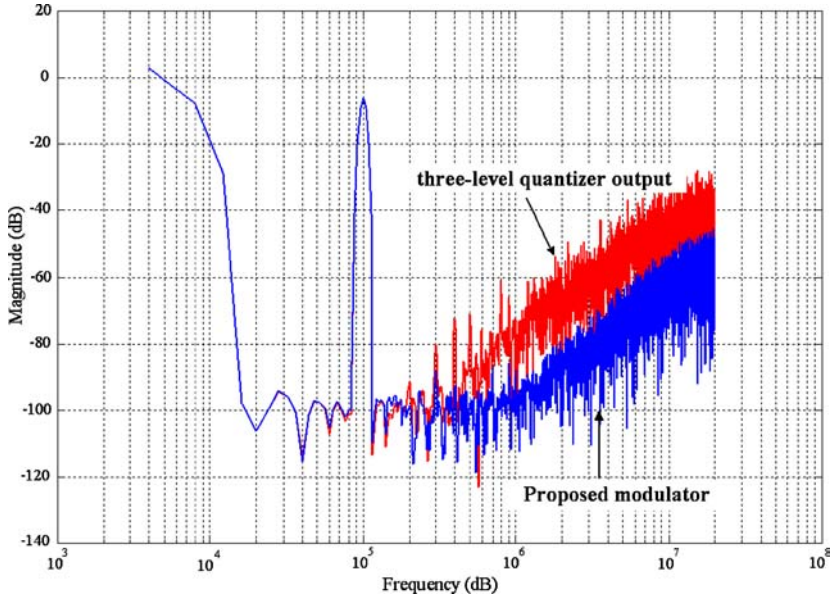

Fig. 15. FFT plot of the SDM outputs.

Table 3. The comparisons of the various architectures used in Bluetooth application.

	Architectures		
Specifications	Conventional Multi-bit 2nd-order SDM	Leslie-Singh [3] Dual-quantizer 2nd-order SDM	Proposed Dual-quantizer 2nd-order SDM
Quantization bits	4	1.5 and 4	1.5 and 4
Bandwidth (MHz)	0.5	0.5	0.5
OSR	40	40	40
Sampling ratio (MHz)	40	40	40
SNDR with ideal case (dB)	84	74	84
SNDR with $A_{dc} = 50$ dB (dB)	76	62	78
SNDR with 1% DAC mismatch (dB)	62	74 (none DAC error)	78 (none DAC error)

the nonlinear distortion of the modulator and reduce the output swing of the integrators in the modulator. Furthermore, the gain error and pole error of the proposed modulator can be improved by using the blind on-line digital calibration technique. Finally, the proposed modulator can extend the dynamic range of the modulator and is suited to wide-bandwidth applications such as xDSL and Bluetooth ... etc. The simulated SNDR as a function of the input level is shown in Fig. 16. According to Fig. 16, the SNDR of the proposed SDM has better tolerance than Leslie-Singh [3] with non-linear amplifier dc gain. Moreover, our proposed SDM is suitable to multi-bit quantizer implementation. Comparing with the conventional multi-bit second-order SDM, the non-linearity DAC effects have been avoided in our approach. The comparisons of the various second-order multi-bit SDM architectures used in Bluetooth application are shown in Table 3.

6. Conclusions

A low-distortion and swing-suppression second-order SDM is proposed to extend the dynamic range and bandwidth. The architecture is effective for low OSR and imperfect components of the modulator, and it can simplify the circuit complexity. According to the mixed-mode 0.25 μm CMOS technology, the proposed architecture can achieve a DR of 90 dB and a peak SNDR of 78 dB at a Nyquist rate of 1 MHz for the Bluetooth application.

In order to improve the nonlinearity effects of the proposed dual-quantizer second-order SDM such as pole error and gain error, the blind on-line digital calibration is applied to the modulator. According to the simulation results, the modulator performance can be improved closely to the ideal case of the modulator. Therefore, the proposed dual-quantizer second-order SDM is very suited to wide-bandwidth application by the standard CMOS process.

Appendix A: Blind On-Line Digital Calibration

Blind on-line digital calibration was proposed by Cauwenberghs [12] and can be used to correct the gain and pole errors of the multi-stage or dual-quantizer SDMs. The task of estimating the parameters α_1, α_2, β_1, and β_2 in equation (16) is ill-defined (i.e. blind). The approach requires a band-limited input signal, with a sampling frequency, f_s, strictly above the Nyquist rate, $f_N = 2f_b$, where f_b is the base-band frequency. Figure A1 illustrates the stop band $[f_b, f_s - f_b]$ that is reserved for calibration. No additional cost is incurred since an anti-aliasing band-limited filter is present for perfect reconstruction of the input.

A high-pass filter, H_c, spanning the band $[f_b, f_s - f_b]$ eliminates the input signal, X. The only complication arises from the frequency dependency of the quantization noise in equation (16) through the noise shaping. The key to blind on-line calibration is to match the

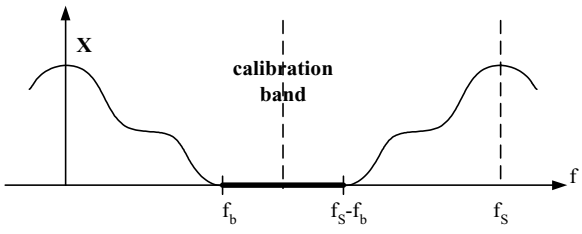

Fig. A1. Signal stop band for the blind on-line calibration.

noise-shaping of the quantization noise as faithfully as possible in the least-square formulation of the parameter estimation, and is explained in the following paragraph.

First, the highpass filter, H_c, is applied to eliminate the band-limited input, X. From equation (16), the coefficients of the digital cancellation filter, $H_2(z)$, is estimated by minimizing the variance of the quantization noise, $Q_2(z)$, assuming a white and uniform power spectrum over the calibration band:

$$|H_c Q_2(z)|^2 = \left| \frac{\alpha_1}{z-\beta_1} \frac{\alpha_2}{z-\beta_2} H_c Y \right|^2 \approx |N_c Y_1 + H(z) N_c Y_2|^2 , \quad \text{(A1)}$$

where $z \equiv e^{j\Omega}$ with $\Omega = 2\pi f / f_s$, and the digital emphasis filter,

$$N_c(z) = \frac{1}{(z-1)^2} H_c(z) \approx \frac{\alpha_1}{z-\beta_1} \frac{\alpha_2}{z-\beta_2} H_c(z), \quad \text{(A2)}$$

serves to equalize the newly proposed noise-shaping of the spectrum of $Q_2(z)$ in the estimation and removes the signal band of X. The error generated in the approximation of the unknown noise-shaping in equation (A2) does not affect the accuracy of the results to the first order.

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