Comments and Corrections

Correction to "A Third-Order ΣΔ Modulator in 0.18-μm CMOS With Calibrated Mixed-Mode Integrators"

J. H. Shim, I.-C. Park, and B. Kim

We recently received feedback from the authors of [2] that the modulator structure in Fig. 1(c) used in our recent paper [1] is similar to that described in [2].

This paper should have been included as a reference in our paper [1]. It was left out by oversight.

References

[1] J. H. Shim, I.-C. Park, and B. Kim, "A third-order ΣΔ modulator in 0.18-μm CMOS with calibrated mixed-mode integrators," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 918–925, Apr. 2005.

[2] D.-Y. Lee, M.-K. Kim, D.-Y. Shim, and W. Kim, "Dynamic range extension technique for high-order ΣΔ ADC's by digital level control," *Electron. Lett.*, vol. 33, pp. 2094–2096, 1997.

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Correction to "A 15-Bit 40-MS/s CMOS Pipelined Analog-to-Digital Converter With Digital Background Calibration"

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In the above paper [1], the authors commented that the gain error correction plus the DAC noise cancellation (GEC + DNC) technique can only be applied to multibit pipeline stages and it also doubles the required opamp's output range [2]–[5]. This statement is misleading and partially incorrect, as pointed out by the author of [2]. The authors would like to change the comment as follows:

If a pipeline stage includes a multibit sub-DAC, the mismatch errors in the sub-DAC can be eliminated by the DAC noise cancellation technique [2]. Correcting the pipeline stage's gain error can further improve the A/D resolution [3]–[5]. The gain error correction technique of [3] demands an increase of the required opamp's output range and an increase of complexity in the sub-DAC design [4]. In the [4] case, the required opamp's output range is increased by 50%. While the continuous gain correction technique of [5] does not increase the required opamp's output range, its performance depends on the accuracy of the sub-ADC [4], and it cannot function properly under certain input conditions

References

[1] H.-C. Liu, Z.-M. Lee, and J.-T. Wu, "A 15-Bit 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1047–1056, May 2005.

[2] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 3, pp. 185–196, Mar. 2000.

[3] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analogue-to-digital converters," *IEE Electron. Lett.*, vol. 36, pp. 617–618, Mar. 2000.

[4] ——, "A digitally enhanced 1.8-V 15-b 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[5] K. Nair and R. Harjani, "A 96 dB SFDR 50 MS/s digitally enhanced CMOS pipeline A/D converter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 456–465.

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