The Design of CMOS Continuous-Time VHF Current and Voltage-Mode Lowpass Filters with Q-Enhancement Circuits

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***Abstract*—In this paper, very high frequency (VHF) current and voltage biquadratic lowpass filters implemented directly by the linear wideband finite-gain current and voltage amplifiers, respectively, are proposed and analyzed. A new Q-enhancement circuit which consists of a finite-gain wideband tunable voltage amplifier and a Miller capacitor is also proposed. It can increase the maximum-gain frequency f_M and enhance the maximum-gain quality factor Q_M of the VHF lowpass filters. Experimental results have successfully verified the capability of the proposed new filter implementation method in realizing both VHF current and voltage lowpass filters with maximum-gain frequency f_M tunable in the range of 148 MHz to 92 MHz. It is also shown from experimental results that the VHF current lowpass biquad with the Q-enhancement circuit has the maximum-gain frequency f_M near 185 MHz and the maximum-gain quality factor Q_M up to 18.5. A fourth-order Chebyshev current lowpass filter with the cut-off frequency of 190 MHz has been successfully designed by using the current biquads with Q-enhancement circuits.**

I. Introduction

In disk-drive read-channel systems, lowpass filters with the passband frequency up to 50 MHz are required. In this specific application, continuous-time technique has been proposed and widely used to implement the required filters [1]–[8]. In many very high frequency (VHF) filtering applications, continuous-time filters rather than sampled-data filters are also preferred. Thus many efforts have been contributed to develop continuous-time VHF filters including both current-mode and voltage-mode filters [5], [6], [8], [12], [19]–[21].

In the construction of continuous-time current-mode filters, current integrators derived from the switched-current (SI) integrator [11]–[13] or current-mode G_m-C integrators [14]–[16] are the basic building blocks. These implementation methods can realize the current-mode filters in the frequency range of several tens megahertz. On the other hand, the basic building blocks of many voltage-mode continuous-time filters are formed by loading the capacitors at the output of the transconductance amplifiers [9]–[10]. The filters using this kind of integrator as the basic cells are the well-known G_m-C filters [1]–[8] which can be operated in the VHF range in current CMOS technologies.

To form a biquadratic lowpass filter, two current integrators or G_m-C voltage integrators as well as some constant-gain stages are connected together in a feedback structure. For certain filter specifications, a high quality factor is needed [17]–[18]. A design method which uses multiple-output nonlinearized operational transconductance amplifiers (OTA's) as building blocks has been developed for the implementation of high Q and high-frequency second-order filters [18]. The second-order filters can be cascaded to form high-order filters. Recently, a new design method which uses the transresistance-$C(R_m$-$C)$ differentiator as the second-order bandpass filter and the basic building block of high-order filters has also been developed and successfully applied to the realization of VHF bandpass filters with center frequencies up to 100 MHz [19]–[21].

In this paper, simple unity-gain current and voltage amplifiers constructed by G_m and R_m amplifier stages are proposed and analyzed. Considering the device capacitances of the MOS transistors as filter elements, both unity-gain current and voltage amplifiers can be used directly to realize current-mode and voltage-mode lowpass tunable biquadratic filters, respectively. The biquads can be further used to build high-order filters. Moreover, a new circuit called the Q-enhancement is proposed. Applying the circuit to lowpass current biquads, the maximum-gain frequency f_M and the maximum-gain quality factor Q_M can be enhanced efficiently.

In realizing biquadratic or high-order lowpass VHF filters, the proposed circuits have the advantages of compact structure and easy design. The proposed Q-enhancement circuit has the advantage of efficient increase of the quality factor Q. It also makes the controlling voltage (V_{cq}) of the quality factor separated from the controlling voltage ($V_{cn} = -V_{cp}$) of the center-frequency ω_0 for easy tuning, although extra power dissipation and chip area are required for the Q-enhancement circuit. Moreover, the tuning of the proposed Q-enhancement circuit can be easily achieved with good stability by a controlling gate voltage.

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In Section II, the circuit structures of the wideband finite-gain current and voltage amplifiers are proposed and analyzed. In Section III, VHF current and voltage biquadratic lowpass filters design based on the unity-gain amplifiers are described. The special Q-enhancement circuit used to increase both f_M and Q_M of the VHF lowpass biquad is proposed and analyzed. High-order filter design with the biquads as basic building blocks is also demonstrated. The experimental results are presented and discussed in Section V. In Section V, conclusions are given.

II. Wideband Amplifiers Design

Fig. 1 shows the proposed linear wideband current amplifier. In the circuit of Fig. 1, a symmetric push–pull common-gate amplifier is formed by the transistors *MP*2, *MN*1, *MP*1, and *MN*2 to perform a simple I to V conversion and offer a low input impedance to the current amplifier. Basically, this stage can be treated as a transresistance (R_m) amplifier whose outputs are connected to the gates of MOSFET's in the next stage. In the second stage, the transistors *MPR*, *MNR*, *MP*3, *MN*3, *MP*5, and *MN*5 form a pair of tunable G_m amplifiers. The triode-operated transistors *MPR* and *MNR* serve as the tunable resistors to make the G_m values of the transconductance amplifiers tunable. The left G_m amplifier formed by *MP*3 and *MN*3 is connected as a shunt-shunt feedback to the open-loop R_m amplifier to achieve lower input impedance, lower output impedance, and wider amplifier bandwidth. Thus, the performance of the close-loop R_m amplifier can be enhanced. The right G_m amplifier receives the voltage signal from the input R_m amplifier and converts it into the output current.

Due to the symmetric push-pull structure of the input R_m amplifier, the small-signal voltages at nodes 1 and 3 are nearly equal. Thus they can be merged into one node in the small-signal equivalent circuit. Similarly, the nodes 4 and 5 can be merged together. The resultant small-signal equivalent circuit of the current amplifier is shown in Fig. 2 where g_m and g_d are the transconductance and the drain conductance of the MOS devices, respectively. Assume $g_m >> g_d$ for all MOS transistors, the dc gains of the open-loop R_m amplifier and the left feedback G_m amplifier can be expressed as

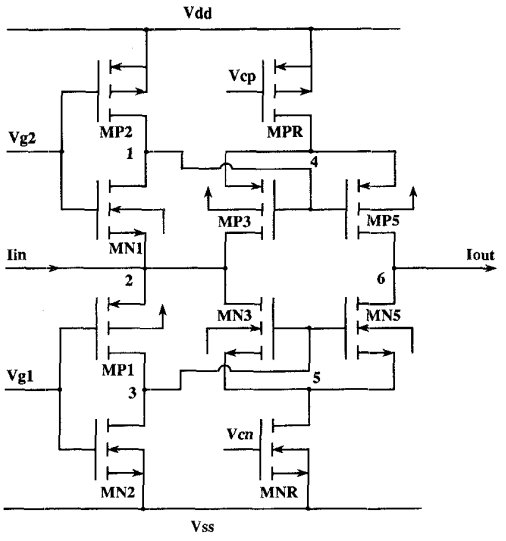
$$R_m \cong \left(\frac{1}{g_{dn1} + g_{dn2} + g_{dp1} + g_{dp2}}\right) = \frac{1}{g_{d1} + g_{d2}} \quad (1)$$

$$G_{m3} \cong \frac{g_{mp3} + g_{mn3}}{1 + \left(\dfrac{g_{mp3} + g_{mn3}}{g_{dpr} + g_{dnr}}\right)} = \frac{g_{m3}}{1 + \dfrac{g_{m3}}{g_{dr}}}. \quad (2)$$

Similarly, the gain of the right output G_m amplifier is

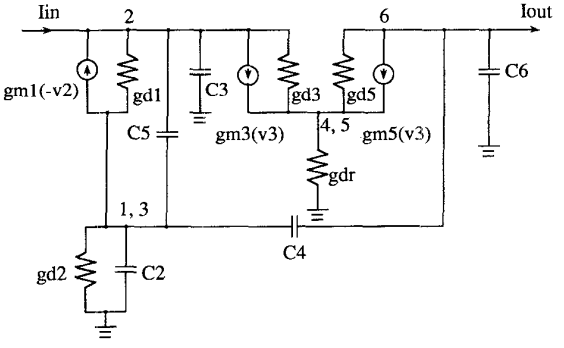
$$G_{m5} \cong \frac{g_{m5}}{1 + \dfrac{g_{m5}}{g_{dr}}} \quad (3)$$

where g_{dr} is the output conductance of the transistors *MPR* and *MNR* operated in the linear region.



	MP2	MN1	MP1	MN2	MPR	MP3	MP5	MN3	MN5	MNR
W (um)	258	108	330	66	300	300	300	100	100	100
L (um)	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6

Fig. 1. The new linear wideband current amplifier.



gm1= gmp1+gmn1 gd1= gdp1+gdn1 gm3 = gmp3+gmn3 gd3 = gdp3+gdn3
gd2 = gdp2+gdn2 gm5 = gmp5+gmn5 gd5 = gdp5+gdn5 gdr = gdpr+gdnr
C2 = Cgdp2+Cgdn1+Cdbp2+Cdbn1+Cgsp3+Cgsp5+Cgdn2+Cgdp1+Cdbn2+Cdbp1+Cgsn3+Cgsn5
C3 = Cgsn1+Csbn1+Cdbp3+Cgsp1+Csbp1+Cdbn3
C4 = Cgdp5+Cgdn5
C5 = Cgdp3+Cgdn3
C6 = Cdbp5+Cdbn5

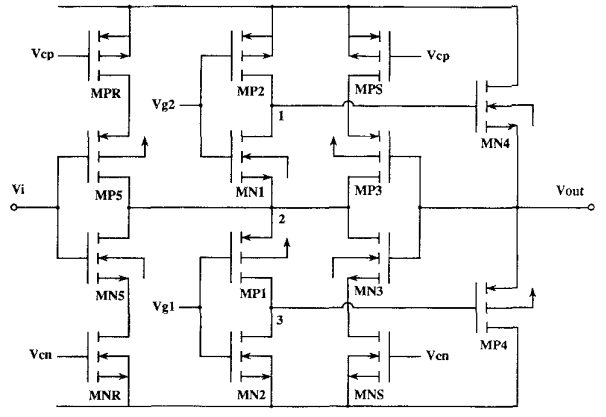
Fig. 2. The small-signal equivalent circuit of the current amplifier shown in Fig. 1.

From Fig. 2, the gain, input resistance, and output resistance of the current amplifier in Fig. 1 can be easily derived as

$$A_i = -G_{m5}\left(\frac{R_m}{1 + G_{m3}R_m}\right) \cong -\left(\frac{G_{m5}}{G_{m3}}\right) \quad (4)$$

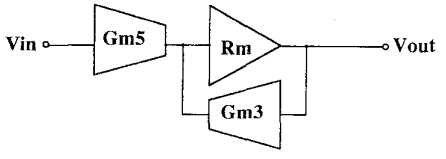
$$r_{\text{in}} \cong \frac{g_{d2}}{G_{m3}g_{m1}} \quad (5)$$

$$r_{\text{out}} \cong \frac{1}{g_{d5}} + \frac{1}{g_{dr}}\left(1 + \frac{g_{m5}}{g_{d5}}\right) \quad (6)$$



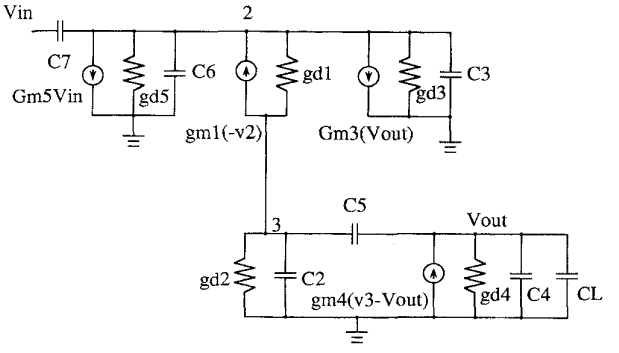
	MPR	MP5	MN5	MNR	MP2	MN1	MP1	MN2	MPS	MP3	MN3	MNS	MN4	MP4
W (um)	120	120	40	40	330	108	354	98.4	120	120	40	40	204	552
L (um)	2	1.6	1.6	2	1.6	1.6	1.6	1.6	2	1.6	1.6	2	1.6	1.6

(a)



(b)

Fig. 3. (a) The new linear wideband voltage amplifier. (b) The block diagram of the linear wideband voltage amplifier.



gm1 = gmp1+gmn1 gd1 = gdp1+gdn1
gd2 = gdp2+gdn2 gm3 = gmp3+gmn3
gd3 = gdp3+gdn3 gm4 = gmp4+gmn4
gd4 = gdp4+gdn4 gm5 = gmp5+gmn5
gd5 = gdn5+gdp5
C2 = Cgdn2+Cdbn2+Cgdp1+Cdbp1+Cgdp4+Cgbp4+Cgdp2+Cdbp2+Cgdn1+Cdbn1+Cgdn4+Cgbn4
C3 = Cdbn3+Cdbp3+Cgsp1+Cgsn1+Csbn1+Csbp1
C4 = Csbn4+Csbp4+Cgsn3+Cgsp3+Cgbn3+Cgbp3
C6 = Cdbp5+Cdbn5
C5 = Cgsn4+Cgsp4+Cgdn3+Cgdp3
C7 = Cgdp5+Cgdn5

Fig. 4. The small-signal equivalent circuit of the voltage amplifier shown in Fig. 3.

where G_{m3} and G_{m5} are given in (2) and (3), respectively. As may be seen in (4), the current gain of the current amplifier depends upon the G_m ratio of the two G_m amplifiers. Thus the current gain may be unity or finite value, depending upon the transistor geometric ratio of the two G_m amplifiers. According to the HSPICE simulation results, the values of r_{in} and r_{out} in the designed current amplifier are 7.42 ohm and 5.75k ohm, respectively.

As shown in Fig. 1, the two triode-operated MOSFET's *MPR* and *MNR* are connected between the power supplies and the source nodes of the transistors in both G_m amplifiers. They act as common tunable resistors for the two G_m amplifiers. Their resistances can be adjusted by simply changing the control gate voltages V_{cn} and V_{cp}. These tunable source series resistances change the gate-source voltages of the MOS transistors and thus change the G_m values of the G_m amplifiers. If the dimensions of *MN5* (*MP5*) and *MN3* (*MP3*) are the same, the current gain almost remains unity independent of the tuning.

The circuit diagram and the block diagram of the proposed linear wideband voltage amplifier are shown in Fig. 3(a) and (b), respectively. In this voltage amplifier, the input voltage signal is converted to the current signal through the G_m amplifier and then the current signal is converted to the voltage signal through the close-loop R_m amplifier. The input tunable G_m amplifier has a CMOS inverter structure with the triode-operated MOSFET's *MPR* and *MNR* controlled by the voltages V_{cp} and V_{cn}, respectively. The close-loop R_m amplifier has a complementary source follower to reduce the output resistance. It also has a feedback tunable G_m amplifier connected from the source follower output to the input of the close-loop R_m amplifier so that the output resistance can be further decreased.

The small-signal equivalent circuit of the voltage amplifier in Fig. 3 is shown in Fig. 4. Assuming $g_m >> g_d$ for all transistors, the voltage gain and the output resistance of the voltage amplifiers can be derived similarly as those of the current amplifier. They can be expressed as

$$A_v = -G_{m5}\left(\frac{R_m}{1 + G_{m3}R_m}\right) \cong -\left(\frac{G_{m5}}{G_{m3}}\right) \tag{7}$$

$$r_{\text{out}} \cong \frac{g_{d1} + g_{d2}}{g_{m4}G_{m3}}. \tag{8}$$

The voltage amplifier has an infinite input resistance. The HSPICE simulated value of r_{out} of the voltage amplifier is as low as 2.84 ohm.

III. VHF Biquad and High-Order Lowpass Filter Design

A. VHF Current Biquadratic Filter

To analyze the high-frequency behavior of the current amplifier, the small-signal equivalent circuit of Fig. 2 with device capacitances is used. Assuming $g_m >> g_d$ for all transistors and neglecting of higher-order non-dominant terms, the transfer function can be expressed as

$$H(s) = \frac{i_{\text{out}}(s)}{i_{\text{in}}(s)} \cong \frac{-D}{s^2A + sB + C} \tag{9}$$

where

$$A \cong (C_2 + C_4)(C_3 + C_5) + C_3C_5 \tag{10}$$

$$B \cong g_{m1}(C_2 + C_4) + G_{m3}C_5 \tag{11}$$

$$C \cong g_{m1}G_{m3} \tag{12}$$

$$D \cong g_{m1}G_{m5}. \tag{13}$$

Apparently, the transfer function expressed in (9) is the form of current lowpass biquad with the center frequency ω_0 and the quality factor Q expressed as

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{g_{m1}G_{m3}}{(C_2 + C_4)(C_3 + C_5) + C_3C_5}} \tag{14}$$

$$Q \cong \sqrt{\frac{C_3 + C_5}{C_2 + C_4}}\left(\frac{G_{m3}}{g_{m1}}\right). \tag{15}$$

The maximum-gain frequency f_M denotes the frequency at which $|H(j2\pi f)|$ has a peak and the maximum-gain quality factor Q_M denotes the gain at f_M. Both f_M and Q_M are defined by the formulas

$$f_M = f_0\sqrt{1 - \frac{1}{2Q^2}} \tag{16}$$

$$Q_M = \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}}. \tag{17}$$

It is seen from (14) and (15) that the center frequency ω_0 and the quality factor Q can be tuned by adjusting the control voltages V_{cn} and V_{cp} to change G_{m3}. Since G_{m5} is also simultaneously tuned as described in Section II, the gain of the current filter, which is equal to G_{m5}/G_{m3} from (12) and (13), remains almost unchanged during the tuning.

In the small-signal equivalent circuit of Fig. 2, there exist parasitic zeros which are usually very far away from f_M so that they can be neglected in deriving (9). According to the HSPICE simulation results on the current biquad of Fig. 1 with $V_{cn} = -V_{cp} = 2.5$ V and without any external capacitor, the maximum-gain frequency f_M is as high as 225 MHz and the nearest LHP zero is 14.6 GHz which is about 70 times larger than f_M. However, to generate a farther LHP zero from f_M even under worst-case process variations or operation temperature, three external linear capacitors denoted as C_{fixed} may be added to the nodes of 1, 2, and 3 of the current biquad of Fig. 1. This decreases f_M and keeps the nearest LHP zero about 100 times larger than f_M. Since the value of C_{fixed} is not critical, it can be realized by a simple MOS device.

With $V_{cn} = -V_{cp} = 2.5$ V and $C_{\text{fixed}} = 0.5$ pF at the nodes 1, 2, and 3 of Fig. 1, the HSPICE simulated maximum-gain frequency f_M (center frequency f_0) and maximum-gain quality factor Q_M (pole quality factor Q) are 153.69 MHz (218.49 MHz) and 1.15 (1.002), respectively. The corresponding transfer function can be expressed as

$$H(s) = \frac{-1.866 \times 10^{18}}{s^2 + 1.37 \times 10^9 s + 1.885 \times 10^{18}} \tag{18}$$

From the HSPICE simulated output list files, the node capacitances and transistor transconductances of the current VHF filter can be calculated. The calculated values including three external linear capacitors are $C2 \cong 3.6$ pF, $C3 \cong 2.43$ pF, $C4 \cong 0.0274$ pF, $C5 \cong 0.0274$ pF, $g_{m1} \cong 0.0024$ mho, and $G_{m3} \cong 0.00525$ mho.

Since $C2 >> C4$, $C3 >> C5$, and $G_{m3} \cong g_{m3}$, (14) and (15) can be further simplified as

$$\omega_0 \cong \sqrt{\frac{g_{m1}g_{m3}}{C_2C_3}} \tag{19}$$

$$Q \cong \sqrt{\frac{C_3g_{m3}}{C_2g_{m1}}}. \tag{20}$$

Using these simplified formulas, the center frequency f_0 and pole quality factor Q can be easily calculated by hand. The calculated center frequency f_0 (cal) is about 191 MHz, and the pole quality factor Q (cal) is about 1.2149. As compared with the HSPICE simulation results, the deviations are 12.6% and 21.2%, respectively. Since these deviations can be compensated by tuning, (19) and (20) can be used as the design equations to design the geometric dimensions of the MOS transistors.

Assume that the channel lengths and widths of the MOS transistors *MP*2, *MN*2, *MPR*, and *MNR* are fixed and the geometric dimension of the MOS transistor *MN*3 (*MP*3) is equal to that of *MN*5 (*MP*5) under the consideration of unity current gain. Equations (19) and (20) can be rewritten as

$$g_{m3} \cong \omega_0 QC_2 \tag{21}$$

$$g_{m1} \cong \frac{\omega_0 C_3}{Q} \tag{22}$$

where

$$\begin{aligned} C_2 &= 2C_{\text{fixed}} + C_{dbMN1} + C_{dbMP1} + C_{gsMP3} + C_{gsMN3} \\ &\quad + C_{gsMP5} + C_{gsMN5} \\ &= 2C_{\text{fixed}} + C_{db1} + C_{gs3} + C_{gs5} \\ &= 2C_{\text{fixed}} + C_{db} + 2C_{gs3} \\ &= 2C_{\text{fixed}} + (W_{P1} + W_{N1})W_dC_{pn} \\ &\quad + \tfrac{4}{3}C_{\text{ox}}(W_{P3}L_{P3} + W_{N3}L_{N3}) \end{aligned} \tag{23}$$

$$\begin{aligned} C_3 &= C_{\text{fixed}} + \tfrac{2}{3}C_{\text{ox}}(W_{P1}L_{P1} + W_{N1}L_{N1}) \\ &\quad + \tfrac{5}{3}C_{pn}(W_{P1} + W_{N1})W_s + C_{pn}(W_{P3} + W_{N3})W_d. \end{aligned} \tag{24}$$

In the above formulas, C_{pn} is the source-bulk (drain-bulk) junction capacitance which is dependent upon junction bias voltage. W_d is the typical distance between junction edge and poly gate edge. Further expressing g_{m1} and g_{m3}

as functions of device currents and dimensions, (21) and (22) can be written as

$$g_{m3} = \sqrt{2\mu_p C_{ox} I_3 \frac{W_{P3}}{L_{P3}}} + \sqrt{2\mu_N C_{ox} I_3 \frac{W_{N3}}{L_{N3}}}$$
$$= \omega_0 Q\{C_{fixed} + (W_{P1} + W_{N1})W_d C_{pn}$$
$$+ \tfrac{4}{3} C_{ox}(W_{P3}L_{P3} + W_{N3}L_{N3})\} \quad (25)$$

$$g_{m1} = \sqrt{2\mu_p C_{ox} I_1 \frac{W_{P1}}{L_{P1}}} + \sqrt{2\mu_N C_{ox} I_1 \frac{W_{N1}}{L_{N1}}}$$
$$= \frac{\omega_0}{Q}\{C_{fixed} + \tfrac{2}{3} C_{ox}(W_{P1}L_{P1} + W_{N1}L_{N1})$$
$$+ \tfrac{5}{3} C_{pn}(W_{P1} + W_{N1})W_s + C_{pn}(W_{P3} + W_{N3})W_d\} \quad (26)$$

where $\mu_N(\mu_P)$ is the surface mobility. If the channel lengths of the MOS transistors are fixed and the device parameters, the biasing currents $I1$ and $I3$, and the desired center frequency f_0 and quality factor Q are given, the channel widths W_{P3}, W_{N3}, W_{P1}, and W_{N1} can be calculated from (25) and (26).

B. VHF Voltage Filter

To analyze the high-frequency behavior of the voltage amplifier in Fig. 3, the small-signal analysis of the voltage amplifier including device capacitances is performed by using the small-signal equivalent circuit in Fig. 4. Assuming $g_m >> g_d$ for all transistors and neglecting of higher-order nondominant terms, the transfer function can be expressed as (27), shown at the bottom of the page.

From (27), it is seen that the transfer function is the form of voltage lowpass biquad with the pole frequency ω_0 and the pole quality factor Q expressed as

$$\omega_0 = \sqrt{\frac{(G_{m3} + g_{d2})(g_{m1} + g_{d1})}{C_2(C_3 + C_6)}} \quad (28)$$

$$Q = \sqrt{\frac{(C_3 + C_6)(G_{m3} + g_{d2})}{C_2(g_{m1} + g_{d1} + g_{d3})}}. \quad (29)$$

The tuning method of ω_0 and Q is the same as that of the current-mode lowpass biquad.

With $V_{cn} = -V_{cp} = 2.5$ V, the HSPICE simulated maximum-gain frequency f_M (center frequency f_0) and maximum-gain quality factor Q_M (pole quality factor Q) are 149.5 MHz (197.7 MHz) and 1.18 (1.044), respectively. Thus, the corresponding transfer function can be expressed as

$$H(s) = \frac{-1.521 \times 10^{18}}{s^2 + 1.189 \times 10^9 s + 1.543 \times 10^{18}}. \quad (30)$$

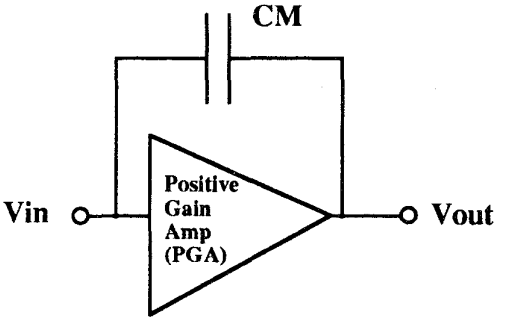


Fig. 5. The block diagram of the new Q enhancement circuit.

C. New Q-Enhancement Circuit

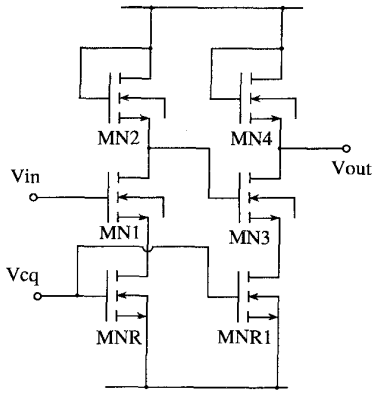
As can be seen from (14) and (15), if the capacitance of $C2$ at the node 1 or node 3 is reduced, the center frequency f_0 and the quality factor Q can be increased. If the reduction quantity can be adjusted, f_0 and Q can be tuned. Here a new circuit is proposed to reduce $C2$ and enhance the Q value.

If a capacitor CM is connected across the input and the output of a voltage amplifier with the voltage gain A_v as shown in Fig. 5, the equivalent capacitance seen from the input node of the amplifier is $CM(1 - A_v)$, known as the Miller Effect. If the voltage gain of the amplifier is positive and larger than one, the effective input capacitance seen from the amplifier input node is negative, which can reduce the overall capacitance at the input node.

Based upon the above circuit concept, the node capacitance $C2$ at the node 1(3) can be reduced by connecting the input of a positive-gain wideband voltage amplifier to the node 1(3) and keeping its output floating. The Miller capacitor CM is connected between the node 1(3) and the floating output node. The positive voltage gain of the amplifier can be adjusted to tune f_0 and Q.

The proposed positive-gain wideband voltage amplifier is shown in Fig. 6. The amplifier is constructed by cascading two NMOS common-source amplifiers. In the first (second) amplifier, the transistor $MN1$ ($MN3$) acts as the common-source stage and the transistor $MN2$ ($MN4$) serves as the enhancement load. The voltage gain of the single-stage voltage amplifier is the transconductance ratio of the transistors $MN1$ ($MN3$) and $MN2$ ($MN4$). The triode-operated transistor MNR ($MNR1$) which is connected between the source of the transistor $MN1$ ($MN3$) and the power supply V_{ss}, acts as a tunable resistor with the control gate voltage V_{cq}. By varying V_{cq}, the g_m value

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} \cong \frac{-(G_{m5} + g_{d2})(g_{m1} + g_{d1})}{s^2 C_2(C_3 + C_6) + s(g_{m1} + g_{d1} + g_{d3})C_2 + (G_{m3} + g_{d2})(g_{m1} + g_{d1})} \quad (27)$$



	MNR	MN1	MN2	MNR1	MN3	MN4
W (um)	400	98	49	400	250	80
L (um)	1.0	1.0	1.0	1.0	1.0	1.0

Fig. 6. The amplifier used to enhance the maximum-gain frequency f_M and maximum-gain quality factor Q_M.

of the transistor *MN*1 (*MN*3) is changed and the gain of the amplifier is also changed. Thus, the gain of the voltage amplifier is adjustable by varying the control gate voltage V_{cq}.

The special Q-enhancement circuit of Fig. 5 is applied to the nodes 1 and 3 of the current amplifier shown in Fig. 1. Thus the current filter with f_0 and Q enhancement is constructed. According to HSPICE simulation results, if $V_{dd} = -V_{ss} = 2.5$ V and V_{cq} changes from 0 V to 2.5 V, the dc gain of the voltage amplifier varies from 1.30 to 1.74, the -3 dB frequency varies from 1.56 GHz to 1.27 GHz, and the power dissipation of the Q-enhancement circuits varies from 190 mW to 200 mW.

When the control voltage V_{cq} changes from 0 Volt to 2.5 Volt and the Miller capacitance CM = 1.5 pF, the HSPICE simulated maximum-gain frequency f_M (center frequency f_0) changes from 144 MHz (166.2 MHz) to 205.6 MHz (207 MHz) whereas the maximum-gain quality factor Q_M (pole quality factor Q_p) from 1.44 (1.429) to 14.2 (14.1). With suitable transistor geometric ratio of the voltage amplifiers in the Q-enhancement circuits, the gain of the amplifiers can be as high as 1.87 and the -3 dB frequency as high as 1.3 GHz under 218 mW power dissipation. Thus, the maximum-gain quality factor Q_M of the current filter with Q enhancement can be as high as 145.54. If the gain of the amplifier is increased further, the effect of the Q-enhancement circuit will overcompensate the node capacitances. In this case, the RHP poles will be generated and the system will be unstable. However, suitable choosing *CM* can avoid the unstability. Fig. 7 shows the HSPICE simulation results of the maximum-gain frequency f_M and the maximum-gain quality factor Q_M of the current filter with Q enhancement versus the power dissipation of the Q-enhancement circuits. Note that both V_{cq} and $V_{cn}(V_{cp})$ can be used to iteratively tune f_M and Q_M of the filter so that the desired values can be reached.

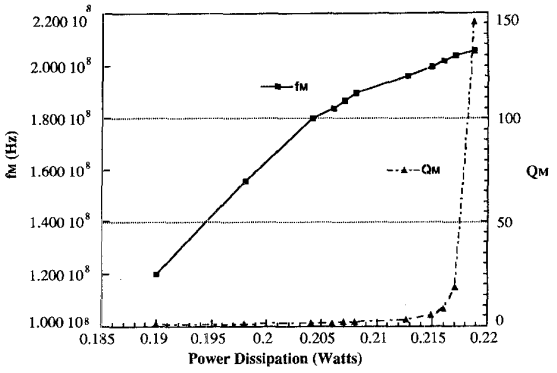


Fig. 7. The HSPICE simulation results of the f_M and Q_M of the current filter with Q enhancement versus the power dissipation of the Q-enhancement circuits.

D. High-Order Filter Design

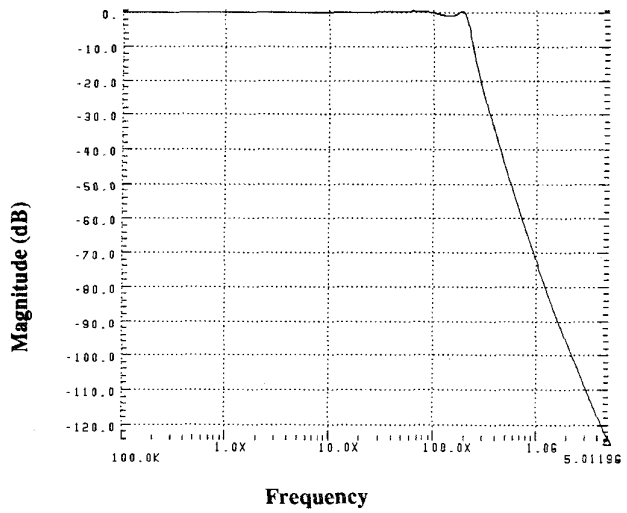
Since the ratio of r_{out}/r_{in} is large (small) enough, the proposed current (voltage) biquads can be cascaded directly to form the high-order current (voltage) filters. As a demonstrative example, a fourth-order Chebyshev current lowpass filter is designed by using the proposed VHF current biquadratic lowpass filter as the basic building block. Here, the current filter with Q enhancement is used as the basic block since this kind of filter is controlled by the two independent tuning control voltages V_{cq} and $V_{cn}(V_{cp})$. Thus, the desired values of f_0 and Q can be reached by iterative tuning.

The fourth-order Chebyshev lowpass filter has 0.5 dB ripple in the passband and a cut-off frequency 190 MHz. From the filter handbook, the transfer function of the fourth order lowpass Chebyshev filter is

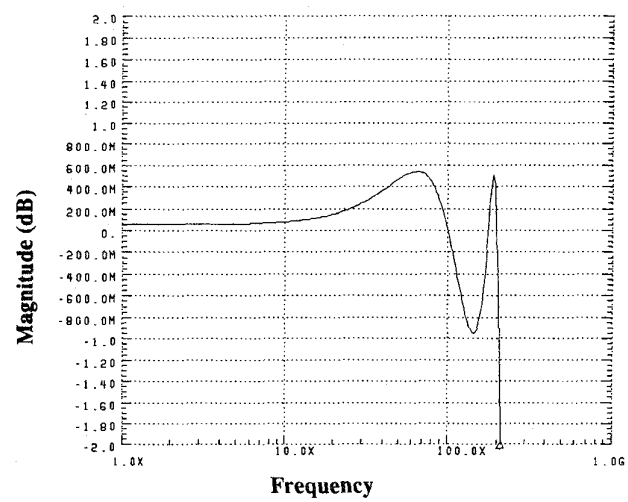
$$H_4(s) = H_{cf1}(s)H_{cf2}(s) = \left(\frac{1.063563\omega_0^2}{s^2 + 0.350706\omega_0 s + 1.063563\omega_0^2}\right) \cdot \left(\frac{0.356461\omega_0^2}{s^2 + 0.846796\omega_0 s + 0.356461\omega_0^2}\right). \quad (30)$$

In the implementation of the transfer function $H_{cf1}(s)$, a biquadratic lowpass filter with $Q = 2.94$ and $f_0 = 196$ MHz is needed. Similarly, for the transfer function $H_{cf2}(s)$, a lowpass biquad with $Q = 0.705$ and $f_0 = 113.4$ MHz is designed. In designing the two biquads, (25) and (26) are used to determine the device dimensions of the current filters. Then tuning is used to obtain the desired f_0 and Q.

With $V_{cn} = -V_{cp} = 1.0$ V and $V_{cq} = 1.3$ V, the HSPICE simulated center frequency f_0 of the current filter with Q enhancement is 197 MHz and the pole quality factor Q is 3.0. Thus this biquad can be used to implement the transfer function $H_{cf1}(s)$. With $V_{cn} = -V_{cp} = -0.65$ V and $V_{cq} = -0.3$ V, the HSPICE simulated center frequency f_0 is 114.6 MHz and the pole quality factor Q is



(a)



(b)

Fig. 8. (a) The HSPICE simulated frequency response of the fourth-order Chebyshev lowpass filter. (b) The passband frequency response of the fourth-order Chebyshev filter.

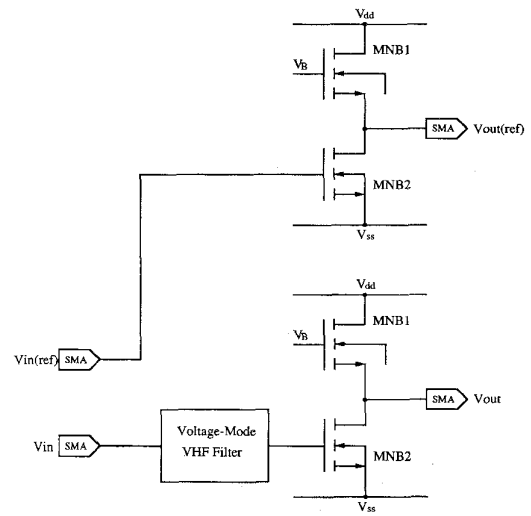


Fig. 9. The on-chip measurement circuit schemes for the fabricated VHF voltage filter.

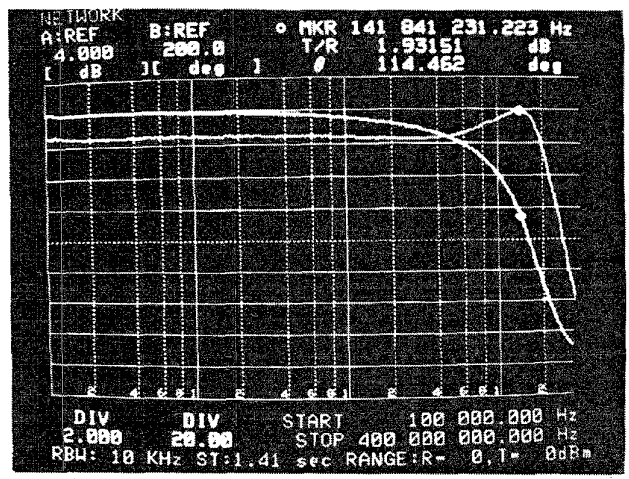


Fig. 10. The measured frequency response (gain and phase) of the fabricated VHF voltage lowpass biquad filter with $CL = 0.2$ pF, when the control voltages $V_{cn} = -V_{cp} = 2.5$ V.

0.694. This biquad is used to implement the transfer function $H_{cf2}(s)$. Finally, these two lowpass biquads are cascaded directly and then the fourth-order Chebyshev lowpass filter with the cut-off frequency 190 MHz is designed. The HSPICE simulated frequency response of the fourth-order Chebyshev lowpass filter is shown in Fig. 8(a) where the passband frequency response is separately shown in Fig. 8(b).

IV. Experimental Results

The proposed lowpass current and voltage biquads have been designed and fabricated in 0.8 μm N-well double-poly-double-metal CMOS technology. Suitable layout techniques have been used to reduce the extra circuit parasitics. Also some extra on-chip circuits have been added to ease the measurement of the fabricated filters in the VHF range.

The on-chip measurement circuit schemes of the fabricated voltage-mode lowpass filters are shown in Fig. 9. Here, a CMOS wide-band gain stage serving as an output buffer for the VHF filters is used to decrease the loading effect of the parasitic capacitances at the output pad. Besides, the on-chip reference path with a single output buffer is designed. Thus its frequency response can be measured for the compensation of the measured frequency response of the filters and the buffer so that the real filter response can be obtained. After compensating the response of the reference path, the measured frequency response of the VHF voltage lowpass biquad is shown in Fig. 10. For $CL = 0.2$ pF and $V_{cn} = -V_{cp} = 2.5$ V, the measured maximum-gain frequency f_M is about 141.8 MHz and the maximum-gain quality factor Q_M is 1.19. Compared with the HSPICE simulation results of f_M (sim) = 149.05 MHz and Q_M (sim) = 1.18, the deviations 5.15% and 0.84%, respectively. These deviations mainly

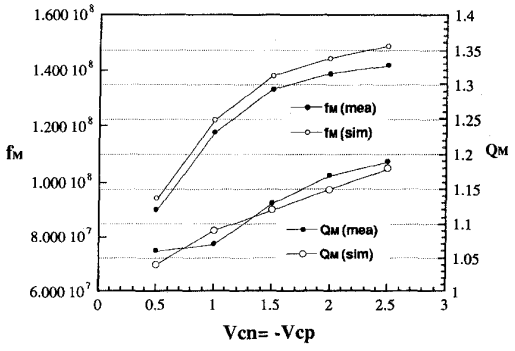


Fig. 11. Comparison of the simulated and measured results of the fabricated VHF voltage lowpass biquad with $CL = 0.2$ pF versus different control voltages V_{cn} and V_{cp}.

TABLE I
SIMULATED AND MEASURED RESULTS OF THE VHF VOLTAGE LOWPASS BIQUAD WITH ($V_{dd} = -V_{ss} = 2.5$ V)

	Simulated Values (HSPICE)	Experimental Values
Capacitance Loading	0.2 pF	0.2 pF
Max-gain Frequency fM (Vcn= -Vcp=2.5V)	149.05 MHz	141.8 MHz
Max-gain Quality Factor QM (Vcn= -Vcp=2.5V)	1.18	1.19
Tunable Range of fM (Vcn=-Vcp change from 2.5V to 0.2V)	149.05 / 94 MHz	141.8 / 92 MHz
Variations of QM (Vcn= -Vcp change from 2.5V to 0.2V)	1.18 / 1.04	1.19 / 1.05
Max. Output Swing for 1% THD (Vcn= -Vcp=2.5 V)		38.9 mVrms
Total Passband Noise		123 uVrms
Dynamic Range (Vcn=-Vcp=2.5V)		50 dB
Power Dissipation (Vcn=-Vcp=2.5V)		20 mW

result from the impreciseness in the parasitic capacitances estimation due to process variations.

The frequency deviations may be post-tuned by adjusting the control voltage $V_{cn}(V_{cp})$ of the unity-gain voltage amplifier. Fig. 11 shows the comparison of the simulated and measured f_M and Q_M of the fabricated VHF voltage lowpass biquad versus the control voltages V_{cn} and V_{cp}. The tuning range of the maximum-gain frequency is as high as 49 MHz. The equivalent maximum output signal of the biquad with $f_M = 141.8$ MHz is about 38.9 m Vrms. The measured total passband noise is about 123 uVrms. Therefore, the dynamic range is about 50 dB. The power consumption of the VHF voltage lowpass filter, not including the output buffer is about 20 mW for ± 2.5 V power supply. Table I summarizes the comparison results

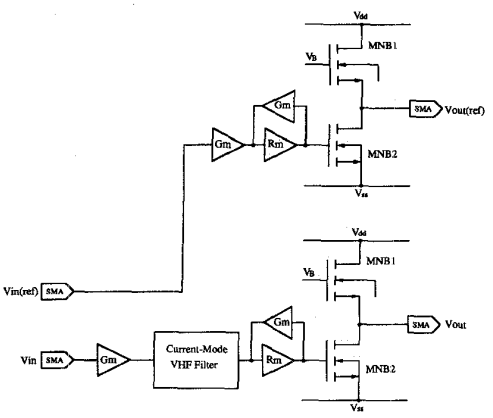


Fig. 12. The on-chip measurement circuit schemes of the fabricated current lowpass biquad filter.

between measured characteristics and HSPICE simulated results of the VHF voltage-mode lowpass biquad.

The on-chip measurement circuit schemes of the fabricated current-mode lowpass biquad are shown in Fig. 12. The voltage lowpass filter in Fig. 3(b) is used as the interface circuit to measure the fabricated VHF current filter. The voltage lowpass filter circuit can be separated into two parts. The first part is the G_m amplifier, and the second one is the close-loop R_m amplifier. The input voltage signal is converted to the current signal through the G_m amplifier and flows into the current filter. The filter output current is then converted to voltage signal by the close-loop R_m amplifier and the voltage signal is sent to the output pad through a CMOS voltage buffer.

Moreover, the on-chip reference interface circuit path constructed by voltage lowpass filter and voltage buffer is used to compensate the measured frequency response of the current filter and the interface circuits. After compensating the response of the reference path, the measured frequency response of the VHF current lowpass biquad is shown in Fig. 13. For $CL = 1.4$ pF and $V_{cn} = -V_{cp} = 2.5$ V, the measured maximum-gain frequency f_M is about 147.8 MHz and the maximum-gain quality factor Q_M is 1.49. As compared with the HSPICE simulation results of f_M (sim) = 153.7 MHz and Q_M (sim) = 1.15, the deviations are 3.84% and 29.5%, respectively.

Fig. 14 shows the comparison of the simulated and measured f_M and Q_M of the fabricated VHF current lowpass biquad versus the control voltages V_{cn} and V_{cp}. When $V_{cn} = -V_{cp}$ changes from 2.5 V to 0.2 V, the measured f_M (Q_M) of the fabricated VHF current lowpass biquad changes from 147.8 MHz (1.49) to 102.5 MHz (1.13). The tuning range of the maximum-gain frequency is as high as 45 MHz. Fig. 15 shows the total harmonic distortion measurement (1% THD) of the VHF current lowpass filter and the on-chip measurement circuit of Fig. 12. In Fig. 15, the measured maximum output voltage swing for 1% THD is 35.4 mVrms. Since the total transresistance of the close-loop R_m amplifier and the CMOS voltage buffer is about 384.8 ohm, the equivalent maximum output current signal of the biquad with $f_M = 147.8$ MHz

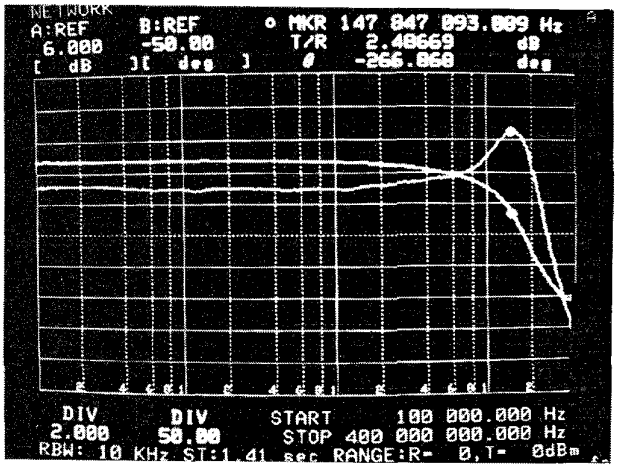


Fig. 13. The measured frequency response (gain and phase) of the fabricated VHF current lowpass with $CL = 1.4$ pF, when the control voltages $V_{cn} = -V_{cp} = 2.5$ V.

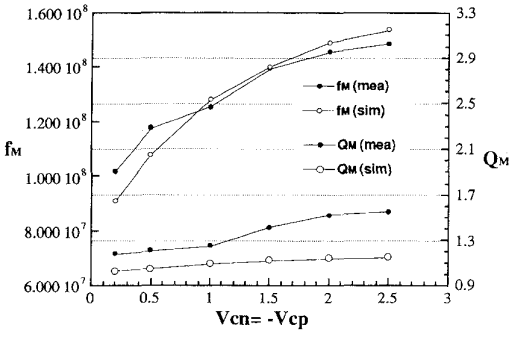


Fig. 14. Comparison of the simulated and measured results of the fabricated VHF current lowpass biquad with $CL = 1.4$ pF versus different control voltages V_{cn} and V_{cp}.

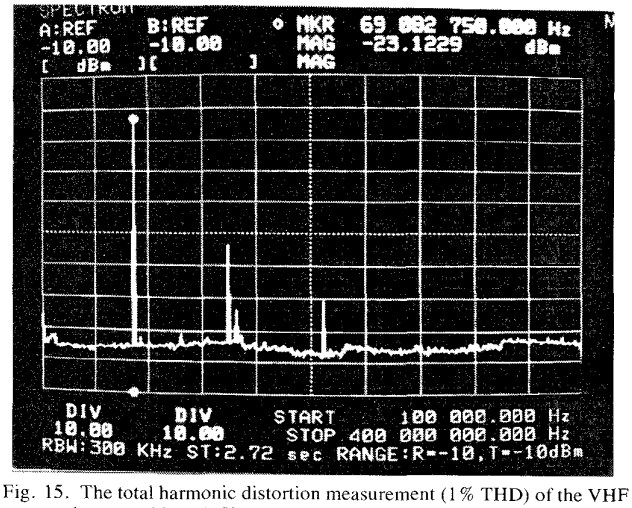


Fig. 15. The total harmonic distortion measurement (1% THD) of the VHF current lowpass biquad filter and the on-chip measurement circuit of Fig. 12.

is about 92 uArms. The distortion is partially generated by the output common-source amplifier whose linearity is not inherently high.

Fig. 16 shows the noise characteristics of the fabricated

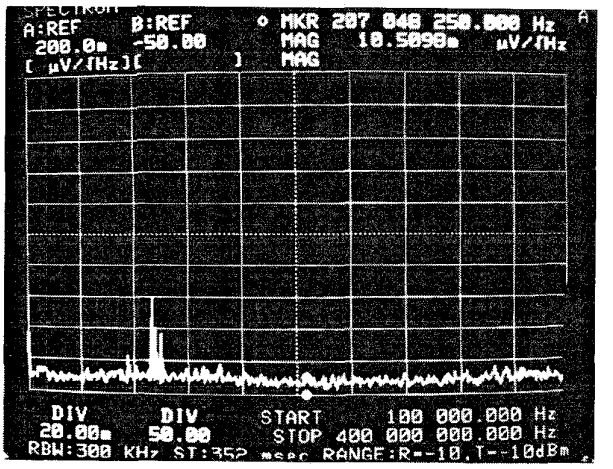


Fig. 16. Noise characteristics of the fabricated VHF current lowpass biquad filter and the on-chip measurement circuit of Fig. 12.

TABLE II
SIMULATED AND MEASURED RESULTS OF THE VHF CURRENT LOWPASS BIQUAD WITH ($V_{dd} = -V_{ss} = 2.5$ V)

	Simulated Values (HSPICE)	Experimental Values
Capacitance Loading	1.4 pF	1.4 pF
Max-gain Frequency fM (Vcn=-Vcp=2.5V)	153.7 MHz	147.8 MHz
Max-gain Quality Factor QM (Vcn= -Vcp=2.5V)	1.15	1.49
Tunable Range of fM (Vcn=-Vcp change from 2.5V to 0.2V)	153.7 / 107.9 MHz	147.8 / 102.5 MHz
Variations of QM (Vcn= -Vcp change from 2.5V to 0.2V)	1.15 / 1.05	1.49 / 1.13
Max. Output Swing for 1% THD (Vcn= -Vcp=2.5 V)		92 uArms
Total Passband Noise		347.8 nArms
Dynamic Range (Vcn=-Vcp=2.5V)		48.5 dB
Power Dissipation (Vcn=-Vcp=2.5V)		21.8 mW

VHF current lowpass biquad and the on-chip measurement circuit of Fig. 12. The total passband noise including that in the on-chip measurement circuit is about 347.8 nArms and the filter dynamic range should be larger than 48.5 dB. The power consumption of the VHF current lowpass biquad is about 21.8 mW for ± 2.5 V power supply. The measured characteristics and the simulation results of the VHF current lowpass biquad filter are summarized in Table II.

Using the same on-chip measurement circuit schemes for the current-mode lowpass biquad, the characteristics of the fabricated current biquad with the Q enhancement circuit can be measured. The measured frequency re-

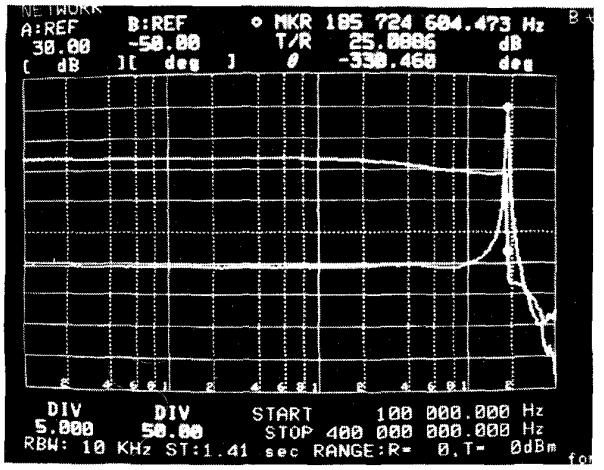


Fig. 17. The measured frequency response (gain and phase) of the fabricated VHF current lowpass with Q enhancement biquad filter with CL = 1.4 pF, when the control voltages $V_{cq} = V_{cn} = -V_{cp} = 2.5$ V.

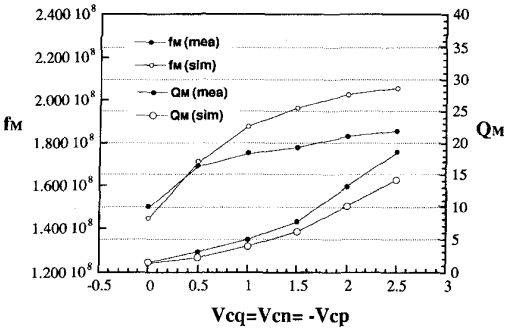


Fig. 18. Comparison of the simulated and measured results of the fabricated VHF current lowpass with Q enhancement biquad filter with CL = 1.4 pF versus different control voltages V_{cn}, V_{cp}, and V_{cq}.

sponse of the VHF current filter with Q enhancement is shown in Fig. 17. For CL = 1.4 pF, CM = 1.5 pF, and $V_{cq} = V_{cn} = -V_{cp} = 2.5$ V, the measured maximum-gain frequency f_M is about 185.7 MHz and the maximum-gain quality factor Q_M can be enhanced to be 18.5. As compared with the HSPICE simulation results f_M (sim) = 205.6 MHz and Q_M (sim) = 14.2, the deviations are 9.68% and 30%, respectively. Fig. 18 shows the comparison of simulated and measured f_M and Q_M of the fabricated VHF current lowpass biquad with Q enhancement versus the control voltage V_{cq}, V_{cn}, and V_{cp}. When $V_{cq} = V_{cn} = -V_{cp}$ changes from 2.5 V to 0 V, the measured $f_M(Q_M)$ of the fabricated VHF current lowpass biquad with Q enhancement changes from 185.7 MHz (18.5) to 150.7 MHz (1.44), with the tuning range of the maximum-gain frequency as high as 35 MHz. The equivalent maximum output current signal with f_M = 185.7 MHz is about 87.3 uArms. The total passband noise is about 441.5 nArms and the dynamic range is about 45.9 dB. The power consumption of the VHF current filter with Q enhancement is about 221.4 mW for ± 2.5 power supply which is much larger than the current filter without Q enhancement. The increased power consumption is mainly due to the two

TABLE III
SIMULATED AND MEASURED RESULTS OF THE VHF CURRENT Q ENHANCEMENT LOWPASS BIQUAD WITH ($V_{dd} = -V_{ss} = 2.5$ V)

	Simulated Values (HSPICE)	Experimental Values
Capacitance Loading	1.4 pF	1.4 pF
Max-gain Frequency fM (Vcn=-Vcp=Vcq=2.5V)	205.6 MHz	185.7 MHz
Max-gain Quality Factor QM (Vcn=-Vcp=Vcq=2.5V)	14.2	18.5
Tunable Range of fM (Vcn=-Vcp=Vcq change from 2.5V to 0 V)	205.6 / 144.5 MHz	185.7 / 150.7 MHz
Variations of QM (Vcn = -Vcp=Vcq change from 2.5V to 0 V)	14.2 / 1.61	18.5 / 1.44
Max. Output Swing for 1% THD (Vcn= -Vcp =Vcq=2.5V)		87.3 uArms
Total Passband Noise		441.5 nArms
Dynamic Range (Vcn = -Vcp=Vcq=2.5V)		45.9 dB
Power Dissipation (Vcn=-Vcp=Vcq=2.5V)		221.4 mW

Q-enhancement circuits. The measured characteristics and the simulation results of the VHF current filter with Q enhancement are summarized in Table III.

V. CONCLUSIONS

CMOS tunable VHF current-mode and voltage-mode lowpass biquadratic filters designed by using unity-gain or finite-gain amplifiers have been proposed, analyzed, and fabricated. Both experimental and simulation results of the VHF lowpass biquadratic filters have successfully verified the performance. A new Q-enhancement circuit consisting of a wideband tunable positive-gain voltage amplifier and a Miller capacitor is also proposed to enhance both maximum-gain quality factor Q_M and maximum-gain frequency f_M of the filters. Experimental results have been shown that the fabricated lowpass biquad with the Q-enhancement circuit has a high f_M around 185 MHz and a Q_M near 18. A fourth-order Chebyshev current-mode lowpass filter has been successfully designed by cascading two current-mode biquads. Further research on other applications of the biquads will be conducted in the future.

REFERENCES

[1] C. S. Park and R. Schaumann, "Design of a 4-MHz analog integrated CMOS transconductance-C bandpass filter," *IEEE J. Solid-State Circuits*, vol. 23, pp. 987–996, Aug. 1988.

[2] H. Khorramabadi and P. R. Gray, "High frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939–948, Dec. 1984.

[3] J. M. Khoury, "Design of a 15-MHz CMOS continuous-time filter with on-chip tuning," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1988–1997, Dec. 1991.

[4] Y. P. Tsividis, "Integrated continuous-time filter design—An overview," *IEEE J. Solid-State Circuits*, vol. 29, pp. 166–176, Mar. 1994.
[5] L. J. Pu and Y. P. Tsividis, "Transistor-only frequency-selective circuits," *IEEE J. Solid-State Circuits*, vol. 25, pp. 821–832, June 1990.
[6] B. Nauta, "A CMOS transconductance-C filter technique for very high frequency," *IEEE J. Solid-State Circuits*, vol. 27, pp. 142–153, Feb. 1992.
[7] F. Krummencher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–758, June 1988.
[8] Y. T. Wang and A. A. Abidi, "CMOS active filter design at very high frequencies," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1562–1574, Dec. 1990.
[9] F. J. Fernandez, "Linear CMOS transconductance elements," US Patent No. 4, 734, 654, Mar. 29, 1988.
[10] M. A. Tan and R. Schaumann, "Simulating general-parameter LC ladder filters for monolithic realizations with only transconductance element and grounded capacitors," *IEEE Trans. Circuits Syst.*, vol. 36, pp. 299–307, Feb. 1989.
[11] S. S. Lee, R. H. Zele, and D. J. Allstot, "CMOS continuous-time current-mode filters for high-frequency applications," *IEEE J. Solid-State Circuits*, vol. 28, pp. 323–329. Mar. 1993.
[12] R. H. Zele, S. S. Lee, and D. J. Allstot, "A 3V-125 MHz CMOS continuous-time filter," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1993, pp. 1164–1167.
[13] T. S. Fiez, G. Liang, and D. J. Allstot, "Switched-currents circuit design issues," *IEEE J. Solid-State Circuits*, vol. 26, pp. 192–202, Mar. 1991.
[14] J. Ramirez-Angulo, M. Robinson, and E. Sanchez-Sinencio, "Current-mode continuous-time filters: Two design approaches," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 337–341, June 1992.
[15] S. L. Smith and E. Sanchez-Sinencio, "3V high-frequency current mode filters," in *Proc. IEEE Int. Symp. Circuits and Syst.*, May 1993, pp. 1459–1462.
[16] J. Ramirez-Angulo and E. Sanchez-Sinencio, "High frequency compensated current-mode ladder filters using multiple output OTAs," in *Proc. IEEE Int. Symp. Circuits and Syst.*, May 1993, pp. 1412–1415.
[17] H. Khorramabadi and P. R. Gray, "High frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939–948, Dec. 1984.
[18] J. Ramirez-Angulo, E. Sanchez-Sinencio, and M. Howe, "Large f_0Q second-order filters using multiple OTAS," *IEEE Trans. Circuits Syst.*, vol. 41, pp. 587–592, Sept. 1994.
[19] P. H. Lu, C. Y. Wu, and M. K. Tsai, "VHF bandpass filter design using CMOS transresistance amplifier," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1993, pp. 990–993.
[20] ——, "Design techniques for tunable transresistance-C VHF bandpass filters," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1058–1066, Sept. 1994.
[21] C. Y. Wu and H. S. Hsu, "The continuous-time VHF lowpass filter design using finite-gain current and voltage amplifiers and special Q-enhancement circuit," in *Proc. IEEE Int. Symp. Circuits and Syst.*, vol. 5, May 1994, pp. 771–774.

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