A Novel Vertical Bottom-Gate Polysilicon Thin Film Transistor with Self-Aligned Offset

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***Abstract*— A novel device structure for the vertical bottom polysilicon gate thin film transistor (TFT) with a self-align offset drain is proposed and demonstrated. The new VTFT allows a deep-submicron channel length, which is determined by the thickness of the active polysilicon film, not by the lithographic system resolution. The self-alignment offset drain reduces the leakage current, as a result, it exhibits good device performance.**

I. Introduction

VERTICAL thin film transistors (VTFT's) are suitable for high density integration since their channel length are determined by the thicknesses of SiO_2 or polysilicon films instead of the photolithographic limitation. Much work had been devoted to developing and studying VTFT's [1]–[3]. The inverted TFT structure is more advantageously used in an integrated circuit for increasing integration density and improving the topography [4]. For inverted TFT's which have the gate below the channel, the conventional self-aligned structure cannot be achieved. Another problem for TFT's is that its leakage current, which is caused by the off-state drain field, is relatively large since it is a short channel device. The leakage current can be reduced by drain engineering such as by adding an offset structure [4]–[6]. However the offset structure needs an additional masking step which makes the fabrication for the device rather complicated and difficult.

In this letter, we propose and demonstrate a novel VTFT structure which has the inherent off-set drain structure. The self-aligned feature eliminates the additional photolithographic step and the fabricated device exhibited submicron device characteristics.

II. Device Structure and Fabrication

The device structure is illustrated in Fig. 1(c) with its fabrication steps in Fig. 1(a)–(c). The device has two vertical channels with the source at the top and the offset drains at the two sides of the isolation oxide. The key processing steps are as follows:

A silicon wafer was first oxidized to form 800 nm of isolation oxide. Then a 800 nm polysilicon film was deposited by a low-pressure chemical vapor deposition (LPCVD) system at 625°C and doped with $POCl_3$. The film was photolithographically defined to obtain the polysilicon bottom gate. After that, the wafer was loaded into an oxide etcher to etch the isolation oxide to form the offset structure [Fig. 1(a)]. The wafer was then deposited with a TEOS oxide and annealed in O_2 at 850°C for 30 min to form the gate oxide. Another undoped 450 Å amorphous silicon was deposited again by LPCVD to form the active channel of the device. The wafer was annealed at 600°C for 24 h to transform the amorphous silicon into polysilicon. A 300 Å pad-oxide was deposited by LPCVD and an Arsenic implantation of a dose of $2\times10^{15}/cm^2$ was performed vertically to form source/drain regions which were activated at 850°C for 1 h in nitrogen. After source/drain regions were defined and etched [Fig. 1(b)], isolation oxide was deposited and contact holes were opened. Finally, Al was deposited and defined for electrodes.

For comparison, a device (control sample) without etching the offset drain structure during the step of isolation oxide etching of Fig. 1(a) was also fabricated.

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TABLE I
The Measured Values of the Device Parameters of VTFT's with and Without the Drain Offset Before and After they Hydrogenated

Devices		S (mV/dec)	V_{th} (V)	Mobility ($cm^2/V\cdot s$)	I_{min} (pA)	I_D (V_G=-5V) (pA)
Control sample	unhydrogenated	990	3.9	1.95	18	500
	hydrogenated	310	1.5	2.13	4.15	180
Offset sample	unhydrogenated	960	3.8	3.15	6.56	39
	hydrogenated	240	1.3	3.20	2.10	13

III. Results and Discussion

The channel length of this device was determined by the thickness of bottom poly-Si gate and the length of the offset region was determined by the etching of the isolation oxide. Fig. 2 shows the I_D–V_G characteristics, unhydrogenated and hydrogenated, of this VTFT with a W/L of $10\,\mu m/0.8\,\mu m$, along with those of the control device. The subthreshold swings were 0.96 V/decade and 0.24 V/decade for the unhydrogenated and hydrogenated cases respectively. For the control device, they were 0.99 V/decade and 0.30 V/decade, respectively. The dynamic ranges of both the offset and control hydrogenated devices were greater than six decades. However, due to the corners of poly-Si gate, the gate oxide will be

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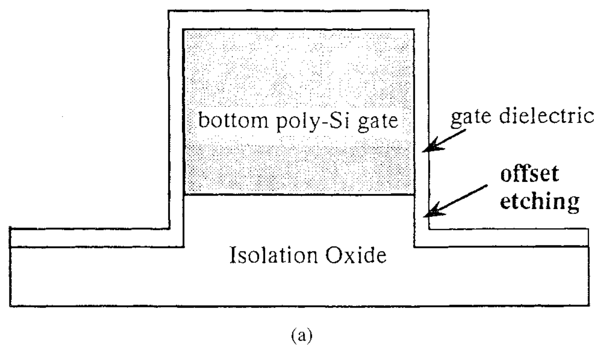
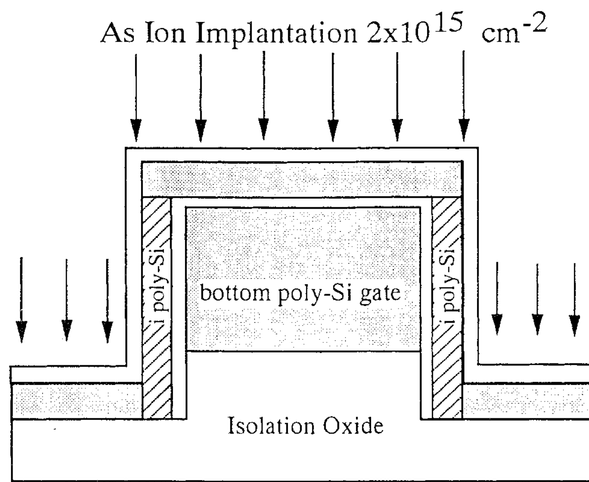
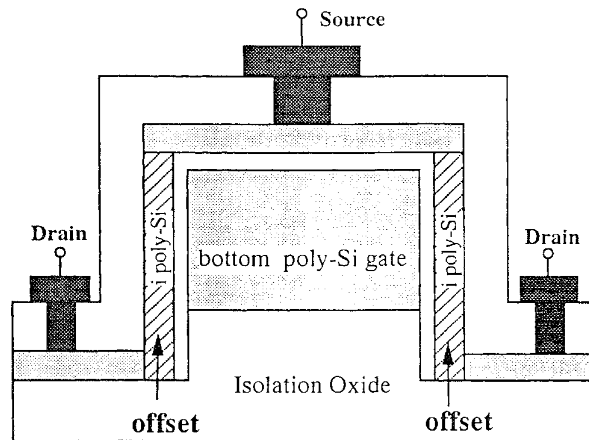


(a)



(b)



(c)

Fig. 1. The main fabrication steps and the cross-sectional schematic of the proposed VTFT. (a) 1. Wet-oxidation 800 nm, deposit poly-Si 800 nm and dope. 2. Define bottom poly-Si gate, etch isolation oxide (100 nm) to form offset region. 3. Deposit oxide as gate dielectric. (b) 4. Deposit α-Si and recrystalize. 5. Deposit pad oxide and ion implant. (c) 6. Deposit passivation oxide. 7. Etch contact hole and Al metalize.

subjected to high electric field and result in early breakdown of gate oxide.

When an off-set structure is introduced, several changes are observed in Fig. 2. First, compared to the control device, the

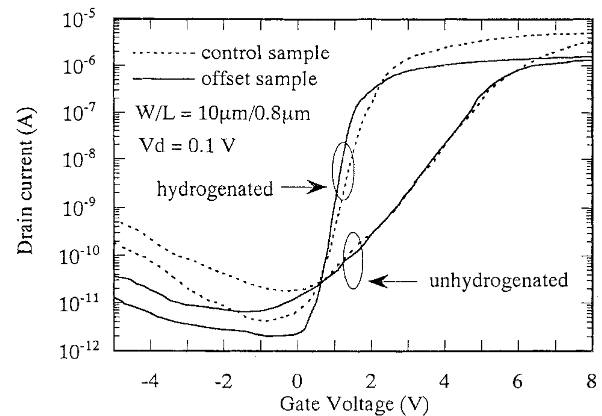


Fig. 2. The $I_D - V_G$ characteristics at the drain voltage $V_D = 0.1$ V of VTFT's, unhydrogenated and hydrogenated, with and without the drain offset.

leakage current is effectively reduced as the offset structure is introduced. The leakage current was due to field enhanced carrier emission via trap states near the drain junction [7], [8]. The offset region reduces the electric field at the drain junction, and controls the leakage current. Second, a reduction of the saturation current is observed, as a series resistance is added by the offset region on the drain side.

Table I compiles the subthreshold swing (S), threshold voltage (V_{th}), mobility, the minimum leakage current ($I_{\min}$) and leakage current at $V_G = -5$ V (I_D) of two devices. The table shows that both devices exhibit submicron characteristics and the offset device had even better characteristics in terms of all the above parameters.

IV. Conclusion

This letter reports a novel VTFT structure with a self-aligned offset drain. This VTFT exhibited good characteristics and allows a deep-submicron channel length without the photolithographic system limitation. The source and drain of this bottom gate vertical TFT were self-aligned by ion implantation and the channel length was determined by thicknesses of bottom polysilicon films. The leakage current was reduced by the self-aligned offset drain structure without an additional lithography step.

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