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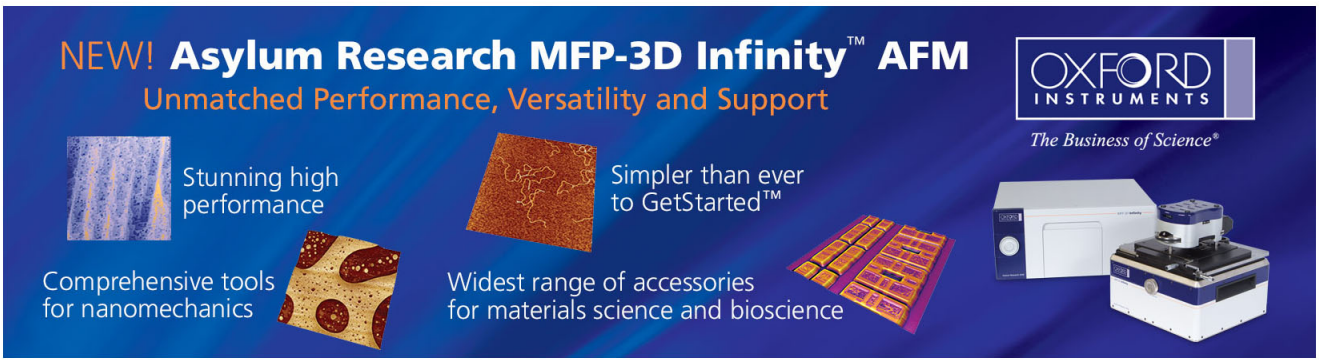

Mobility enhancement of polycrystalline-Si thin-film transistors using nanowire channels by pattern-dependent metal-induced lateral crystallization

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This work presents a method for enhancing the mobility of polycrystalline-Si (poly-Si) thin-film transistors (TFTs) by pattern-dependent metal-induced-lateral-crystallization (PDMILC) using nanowire channels. Experimental results indicate that the field-effect mobility of PDMILC TFT was enhanced as the channel width decreased, because the lateral length of the poly-Si grains increased. The PDMILC poly-Si TFT with ten nanowire channels (M10) had the greatest field-effect mobility, 109.34 $cm^2/V\,s$ and the lowest subthreshold swing, 0.23 V/dec, at a gate length of 2 μm. The field-effect mobility also increased as the gate length in the M10 PDMILC poly-Si TFT device declined, because the number of poly-Si grain-boundary defects was reduced. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2076436]

The primary advantages of using polycrystalline-Si (poly-Si) thin-film transistors (TFTs) in an active matrix liquid crystal display are the greatly improved carrier mobility (larger than 10 $cm^2/V\,s$) in the poly-Si film, the capacity to integrate the pixel switching elements, and the capacity to integrate the panel array and the peripheral driving circuit on the same substrates.[1–3] These capabilities have led to the era of the system-on-panel (SOP). Low-temperature recrystallization is required to make high-performance poly-Si TFTs, for realizing commercial flat-panel displays (FPD) on inexpensive glass substrates, as the maximum process temperature is less than 600 °C. Three major low-temperature amorphous-Si crystallization methods are available for fabricating high-performance poly-Si thin films. These are solid phase crystallization (SPC),[4] excimer laser crystallization (ELC),[5] and metal-induced lateral crystallization (MILC).[6–10] MILC technology was originally developed as a low-temperature crystallization technique. It is superior because, unlike ELC, it is a low-cost batch process, and it yields poly-Si thin film of higher quality than SPC.

However, few reports on MILC poly-Si TFTs have addressed the effects of device dimensions on field-effect mobility. Besides, applications of TFTs are limited to low-temperature FPDs because the grain boundaries in the channel region greatly degrade performance. The electrical characteristics of TFTs can be improved by enlarging the grains, which reduces the number of grain boundaries in the channel region.[11,12] Therefore, this work develops a series of pattern-dependent MILC (PDMILC) TFTs with a multichannel of various widths, to study the relationship between the device dimensions and the field-effect mobility.

In this work, a series of PDMILC TFTs, with a gate length of 2 μm, consisting of ten strips of 67 nm wire channels (M10) TFT, five strips of 0.18 μm channels (M5) TFT, two strips of 0.5 μm channels (M2) TFT and a single-channel structure (S1) with a width of 1 μm TFT, were fabricated, as listed in Table I. Figure 1(a) shows a schematic plot of a PDMILC TFT with the source, drain, gate, nanowire channels, contact holes, and MILC seeding window. Figure 1(b) shows a cross-sectional view of a PDMILC TFT, which was a conventional top-gate offset metal-oxide-semiconductor field-effect transistor (MOSFET) structure.

6 in. *p*-type single-crystal silicon wafers were coated with 400 nm thick SiO_2 as the starting materials. Undoped 50 nm thick amorphous-Si layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the active islands, including source, drain, and ten nanowire channels, were patterned by electron-beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 25 nm thick tetra-ethyl-ortho-silicate oxide (TEOS-SiO_2) was deposited by LPCVD as the gate insulator. Then, 150 nm thick undoped poly-Si

TABLE I. Devices dimension of S1, M2, M5, and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm, gate TEOS-oxide thickness, of 25 nm, and gate length of 2 μm.

Device name	Gate length (L)	Channel number	Each channel width (W)	Effective channel width (W_{eff})
S1	2 μm	1	1 μm	1 μm
M2	2 μm	2	0.5 μm	1 μm
M5	2 μm	5	0.18 μm	0.9 μm
M10	2 μm	10	67 μm	0.67 μm

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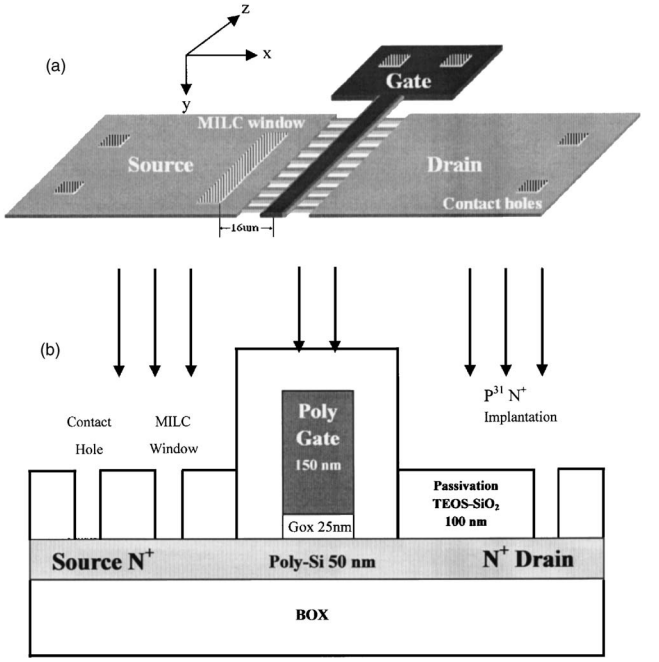

FIG. 1. (a) Schematic plot of PDMILC M10 poly-Si TFT with source, drain, gate, ten nanowire channels, contact holes, and MILC seeding window. The distance between the MILC seeding window edge and middle of active channel is 16 μm. (b) Cross-sectional view of PDMILC TFT, which was a conventional MOSFET with offset structure.

films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100 nm thick TEOS-SiO_2 layer as the passivation layer was deposited by LPCVD. Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Next, a thin 10 nm thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 °C for 48 h in an N_2 ambient. The average lateral crystallization length was about 30 μm [Fig. 2(b)]. After long time annealing, the unreacted Ni on passivative TEOS-SiO_2 was removed by a H_2SO_4 solution at 120 °C for 10 min. Phosphorus ions at a dose of 5×10^{15} cm^{-2} implanted through the passivative TEOS-SiO_2 to form the n^+ gate, source/drain regions, and the self-aligned offset region of 0.1 μm width—were formed in the same process step [Fig. 1(b)]. Then, the dopants were activated by rapid thermal annealing (RTA) at 850 °C with 30 s. The 300 nm thick aluminum (Al) layer was deposited by PVD and patterned for source, drain, and gate metal pads. Then, the finished devices were sintered at 400 °C for 30 min in an N_2 ambient. Finally, each device was passivated by NH_3 plasma treatment for 2 h at 300 °C.

Figure 2(a) shows a scanning electron microscope (SEM) image of the active pattern from an M10 TFT with the source, the drain, ten nanowire channels, and MILC seeding window. The inset SEM photograph presents a magnified area of the ten nanowire channels in the TFT, each of which is 67 nm wide. Figure 2(b) presents an SEM photograph of the active channel of a single-channel MILC poly-Si TFT grain structure following Secco etching.[13] The average poly-Si lateral grain size is around 250 nm. The inset optical microscopy photograph in Fig. 2(b) presents a MILC length of 30 μm, which is longer than 16 μm [Fig. 1(a)], indicating that the entire active channel was crystallized by MILC process. Figure 2(c) presents SEM photograph of a grain structure in one of the ten nanowire MILC poly-Si TFTs (M10) following Secco solution etching. The average poly-Si lateral grain size in M10 TFT is around 520 nm, which is larger than that of those in S1 TFT. This result reveals that the nanowire of M10 TFT enhanced lateral poly-Si grain growth during the MILC process. Figure 3 compares the transfer curves and the field-effect mobility of a series of PDMILC multichannel TFTs with various widths at a gate length (L) of 2 μm. The field-effect mobility (μ_{FE}) was extracted from the peak linear transconductance (g_m) at V_d=0.1 V:

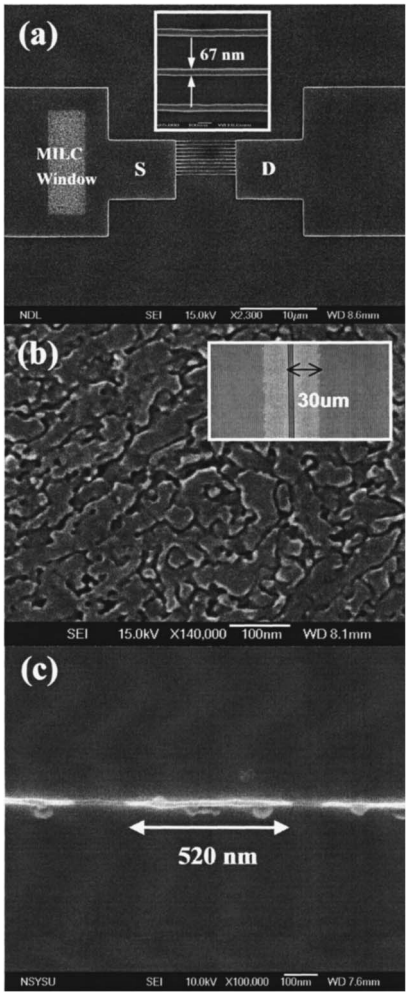

FIG. 2. (a) SEM photograph of active pattern with the source, the drain, ten nanowire channels, and MILC seeding window. The inset SEM photograph shows the each nanowire width of 67 nm. (b) SEM photograph of poly-Si grain structure in active channel of S1 MILC poly-Si TFT following Secco solution etching. The average poly-Si lateral grain size is 250 nm. The inset optical microscopy photograph depicts a MILC length of 30 μm. (c) SEM photograph of grain structure in one of ten nanowire MILC poly-Si TFTs (M10) following Secco etching. The poly-Si lateral grain length is 520 nm.

$$\mu_{FE} = \frac{L}{C_{ox}\cdot W\cdot V_d} g_m. \tag{1}$$

The results in Fig. 3 reveal that the μ_{FE} of PDMILC TFT was enhanced as the width of each channel declined. The M10 TFT had the highest μ_{FE} value of 107.79 cm^2/V s, which was almost triple that of the S1 TFT, 46.62 cm^2/V s. According to the poly-Si TFT mobility model,[14] the effective field-effect mobility (μ_{FE}) is given by

$$\mu_{FE} = \mu_G \frac{1}{1+(\mu_G/\mu_{GB})[(nL_{GB})/L]\exp(qV_b/kT)}, \tag{2}$$

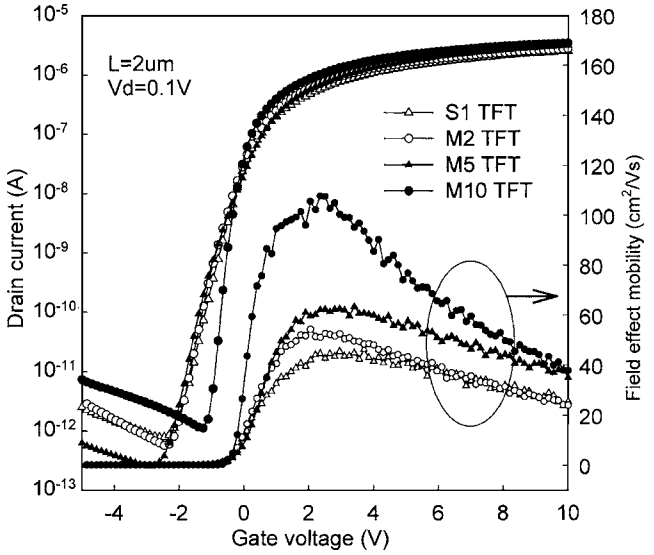

FIG. 3. Transfer I_d-V_g curves (left) and field-effect mobility (μ_{FE}) (right) of a series of PDMILC TFT of a multichannel with various widths at the gate length of 2 μm.

where μ_{FE} is the effective field-effect mobility, L_{GB} is the average grain-boundary length, $n=L/L_G$ is the average grain-boundary number, and L_G is the average intragrain length.

The results reveal that during the MILC process, the poly-Si grain lateral length (L_G) increased as the each channel width declined. Therefore, the average grain-boundary number (n) was reduced, and the mobility increased. Moreover, M10 TFT had the highest μ_{FE}. During the MILC process, a nanowire width of 67 nm strongly limited the growth of poly-Si grains in the z direction [Fig. 1(a)] than that of the other TFTs. Therefore, the poly-Si grains tended to grow laterally in the x direction, becoming large, as shown in Fig. 2(c). All dimensions, including those of the three TFTs, in different areas on the 6 in. wafer, were characterized to study the uniformity of device performance. Table II lists all of the parameters of the poly-Si TFTs as, average and standard deviation, including the field-effect mobility (μ_{FE}), the threshold voltage (V_{th}) and the subthreshold swing (SS). The values in Table II indicate that the μ_{FE} of this PDMILC fabrication is uniformly distributed. Notably, enlarging of the poly-Si grains in M10 TFT not only increased μ_{FE}, but also reduced SS to 0.23 V/dec. The parameter SS is directly related to the total density of trap states (N_T):[15]

$$SS = \left(\frac{kT}{q}\right)\ln 10\left(1+\frac{q^2 t_{Si} N_T}{C_{OX}}\right), \tag{3}$$

where kT is the thermal energy, C_{ox} is the gate oxide capacitance per unit area, and t_{Si} is the thickness of the poly-Si

TABLE II. Device parameters average and standard deviation value of M10, M5, M2, and S1 TFTs with gate length (L) of 2 μm. The V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_d/(W/L)=10^{-8}$ A at $V_d=0.1$ V.

Device name	μ_{FE} ($cm^2/V\,s$)	V_{th} (V)	SS (V/dec)
S1	46.41±0.41	−0.55±0.20	0.73±0.13
M2	53.79±1.16	−0.59±0.41	0.63±0.06
M5	65.69±1.99	−0.37±0.14	0.70±0.15
M10	109.34±1.46	−0.34±0.03	0.23±0.02

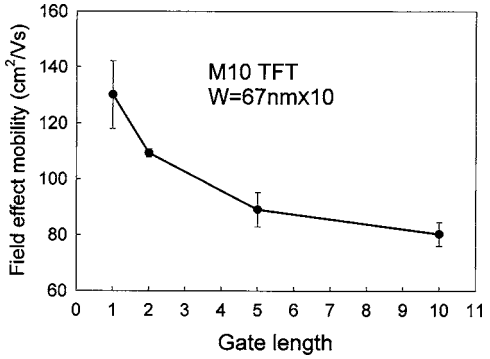

FIG. 4. Field-effect mobility (μ_{FE}) average and standard deviation vs the gate length, for a particular M10 TFT ($W=67$ nm$\times 10$) structure.

layer. Therefore, the decline in SS as the channel width decreased reveals that increasing the lateral size of the poly-Si grain reduced N_T.

Figure 4 plots the average μ_{FE} and standard deviation versus the gate length, for a particular M10 TFT structure. When the widths of the channels in the TFTs were equal, the mobility increased significantly as the gate length declined. These results indicate that the number of poly-Si grain-boundary defects decreased, as the gate length declined.[7]

A method for enhancing the mobility of poly-Si TFTs using nanowire channels by PDMILC was developed. The PDMILC poly-Si TFTs increased the field-effect mobility by reducing the channel width. The PDMILC poly-Si TFT with ten nanowire channels (M10) had the highest field-effect mobility and the lowest subthreshold swing. This method for fabricating PDMILC TFTs with enhanced mobility is easily implemented. It involves no additional mask and is compatible with complementary metal-oxide-semiconductor technology. Such a PDMILC TFT is highly suitable for use in SOP applications and three-dimensional integrated circuit applications in the future.

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