In-Process Functional Testing of Pixel Circuit in AM-OLEDs

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***Abstract*—This paper presents a functional testing scheme using a two-thin-film-transistor (TFT) pixel circuit of an active-matrix organic light-emitting display (AM-OLED). This pixel circuit and the co-operative electrical testing scheme can not only evaluate the characteristics of each TFT, but also determine the location of line and point defects in the TFT array. Information on defects can be used in a unique repair system that cutting and repairing these defects. Furthermore, the functional testing scheme can be applied as a part of yield management of the AM-OLED array process.**

***Index Terms*—Active-matrix (AM), active-matrix organic light-emitting display (AM-OLED), light-emitting diode (LED), organic light-emitting display (OLED), pixel, testing, thin-film transistor (TFT).**

I. Introduction

In THIN-FILM transistor (TFT) processes of not only active-matrix liquid crystal display (AM-LCD) but also AM organic light-emitting display (AM-OLED) [1]–[4], TFT array inspection and yield management are important to ensure the reliability of display applications [5], [6]. In-line testing of TFT array in manufacturing processes is beneficial for yield improvement because the faulty TFT array can be repaired or scrapped before encapsulation and external driver assembly. Likewise, utilizing TFT array testing for failure analysis can detect the locations of the faults and identify the categories of faults in TFT array.

In conventional AM-LCD industry, several inspection technologies have been developed and applied for the TFT array testing, including: 1) the voltage imaging scheme [7]; 2) the electron beam scheme [8]; and 3) the electrical testing scheme [9]. The voltage imaging and electron beam schemes can inspect all TFT devices on entire substrate regardless of the circuitry configuration, but only a few kinds of faults can be detected. Besides, demands of high stability of the instruments and long working time also limit the performance of them. Although the electrical testing scheme requires a large number of contact pins, direct contact and measurement can perform the speedy functional testing and evaluate more parameters of the TFT than others.

The conventional AM-OLED pixel circuit does not provide for fully functional testing with electrical testing scheme as the AM-LCD pixel does [10], unless an additional component can be added in. We propose the modified pixel circuit with cooperating electrical testing scheme to measure the characteristics of TFT and detect defects. The proposed TFT array testing scheme is simulated and demonstrated to be a good tool for managing the yield of the array process of AM-OLED.

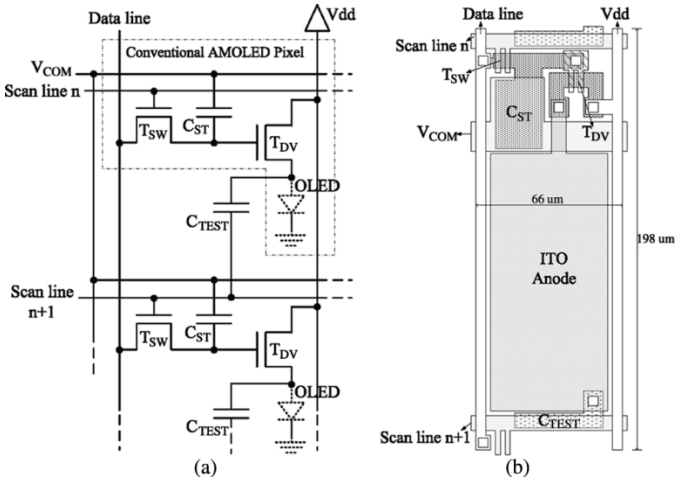

Fig. 1. (a) 2-T pixel circuit for AMOLED TFT array testing and (b) layout view of the modified pixel circuit.

II. Full Function Testing for AM-OLED Pixels

A. Schematic of Pixel Circuit

A conventional two-transistor (2-T) pixel circuit, in which the transistor $T_{\rm SW}$ acts as a switch and the transistor $T_{\rm DV}$ controls the driving current of the pixel, is encircled by dash line in Fig. 1(a). Before OLED process is performed, the ITO anode connected to the source/drain of the $T_{\rm DV}$ of each pixel is in a "floating" state so that not only the source/drain voltage of the $T_{\rm DV}$ can not be confirmed, but also no path is available for conducting the driving current. Therefore, the incomplete pixel circuit limits the testability of TFT array.

An improved 2-T pixel circuit with an additional testing capacitor $(C_{\rm TEST})$ is proposed to enhance the testability of the pixel circuit. The $C_{\rm TEST}$ completes the pixel circuit before OLED material is deposited onto the glass substrate and prevents the floating source/drain of the $T_{\rm DV}$. One electrode of the $C_{\rm TEST}$ is connected to the source/drain of the $T_{\rm DV}$ via the transparent anode, and the other is connected to the neighboring scan line, as schematically shown in Fig. 1(a). The corresponding layout of proposed 2-T pixel circuit is also depicted in Fig. 1(b).

The storage capacitor $C_{\rm ST}$ is used to store the display voltage signal during the entire frame period until next programming.

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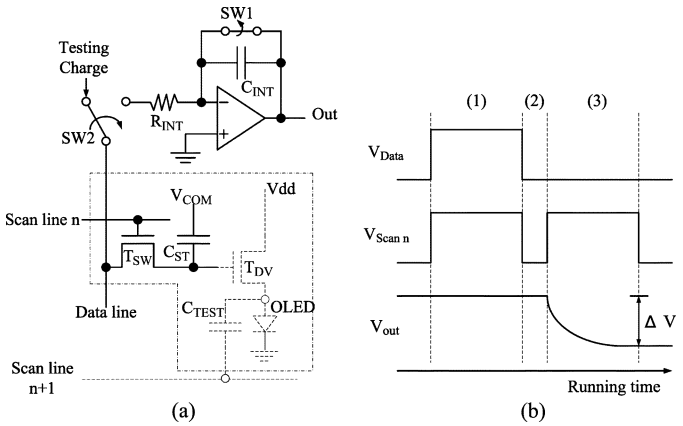

Fig. 2. (a) System diagram with charge detection circuit and (b) timing diagrams for $T_{\rm SW}$ testing. [(1) Writing, (2) holding, and (3) reading period].

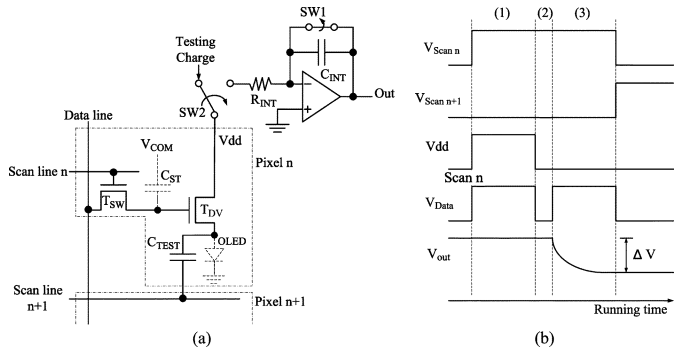

Fig. 3. (a) System diagram with charge detection circuit and (b) the timing diagrams for $T_{\rm DV}$ testing. [(1) Writing, (2) holding, and (3) reading period].

In the AM-LCD pixel circuit, an alternating voltage should be applied to one node of the $C_{\rm ST}$ to achieve an inversion operation of liquid crystal cell. Therefore, an additional electrode $V_{\rm COM}$ is needed for the pixel circuit. Since AM-OLED is driven with dc current, in conventional 2-T pixel circuit, the voltage signal is kept to positive level permanently in the $C_{\rm ST}$. Hence, the $C_{\rm ST}$ can be connected to the $V_{\rm dd}V_{\rm dd}$ to reduce the $V_{\rm COM}$ electrode. However, a changeable voltage will be supplied to $V_{\rm dd}$ electrode during the testing process of the $T_{\rm DV}$ and the voltage stored in $C_{\rm ST}$ can be affected according to the feed-through effect of the $C_{\rm ST}$. In order to improve the accuracy of $T_{\rm DV}$ testing, the $C_{\rm ST}$ is connected to an additional $V_{\rm COM}$ electrode instead of $V_{\rm dd}$. Consequently, the testing process can be performed flexibly but the aperture ratio of pixel circuit is slightly decreased.

B. Detection Circuit and Operation of Functional Testing

The pixel electrode circuit, functioning like a sample and hold circuit, is driven to sample analog data and store them until the following sampling period. Also, by connecting the pixel to an external detection circuit, the stored data can be retrieved. The principle that underlies the proposed electrical testing scheme is to write and read the charges of the pixel. An operational amplifier, configured as an integrator, is used as a detection circuit to receive the charge from the pixel circuit. The detection circuit constructed by an integrator with virtual ground configuration can maintain the voltage of 0 V at the input of detection circuit while the testing is performed. The $T_{\rm SW}$ and the $T_{\rm DC}$ in pixel circuit must be examined individually because of the functional differences. For testing either $T_{\rm SW}$ or $T_{\rm DV}$, the; 1) writing; 2) holding; and 3) reading periods must be achieved sequentially. The details of the testing approach for $T_{\rm SW}$ and $T_{\rm DV}$ is illustrated in the following sections.

1) Functional Testing for $T_{\rm SW}$: The functions of $T_{\rm SW}$ and $C_{\rm ST}$ in an AM-OLED pixel circuit are similar to that in an AM-LCD pixel. Since the amount of charge in the $C_{\rm ST}$ is directly controlled by data line signal, the detection circuit, in which the switch SW1 is used to initialize the output voltage, is connected to the data line of the pixel through a switch SW2. The simplified equivalent circuit and corresponding waveforms for testing $T_{\rm SW}$ are shown in Fig. 2(a) and (b), respectively. In the $T_{\rm SW}$ testing, a constant voltage is supplied to $V_{\rm COM}$ electrode as a reference and the $V_{\rm dd}$ electrode is connected to ground. The operation of pixel circuit is only controlled by the data line and the scan line.

When in the writing period (1), the signal at scan line n is HIGH to turn on the $T_{\rm SW}$, and the SW2 connects the data line to an external power supply which can provide testing charge $Q_{\rm ST} = V_{\rm Data}{\cdot}C_{ST}$ to storage capacitor $C_{\rm ST}$. In the meanwhile, the SW1 connects the output and negative input of amplifier together to initial the output voltage of 0 V. In the following holding period (2), the signal at scan line *n* becomes LOW to turn off the $T_{\rm SW}$. When $T_{\rm SW}$ is OFF, the resistance of which must be large enough to prevent a significant leakage current from $C_{\rm ST}$ to data line. Therefore, the charge $Q_{\rm ST}$ is maintained in the $C_{\rm ST}$ during the entire holding period.

Now consider the reading period (3), the SW2 switches the data line from power supply to the detection circuit, and the SW1 is open to actuate the detection circuit. After that, the scan line signal turns $T_{\rm SW}$ on once again and the charge in $C_{\rm ST}$ is released and redistributes into the detection circuit due to the low resistance of $T_{\rm SW}$. While collecting the charge $Q_{\rm ST}$ by the feedback capacitor $C_{\rm INT}$, the detection circuit is still holding the data line at 0 V simultaneously, therefore no charge is lost. After the charge is collected, the output voltage of the integrator is decreased by an offset voltage $\Delta V_{\rm Out}$, defined as $\Delta V_{\rm Out} = -Q_{\rm ST}/C_{\rm INT}$. Since $\Delta V_{\rm Out}$ is proportional to the amount of charge $Q_{\rm ST}$ stored in $C_{\rm ST}$, holding more charges in $C_{\rm ST}$ makes the output more negative after finishing the detection process.

2) Functional Testing for $T_{\rm DV}$: The $T_{\rm DV}$ works as a voltage-to-current converter to provide a stable current signal to the OLED during whole frame period. Variations of $T_{\rm DV}$ characteristics directly affect the OLED current and result in brightness nonuniformity and inferior image quality. Therefore the functional testing for the $T_{\rm DV}$ is more important than $T_{\rm SW}$. Since the $T_{\rm DV}$ is modulated by the voltage signal at the storage node and the testing charge is applied from Vdd electrode, the detection circuit should be connected to the Vdd instead of the data line and thereby collect the charge in $C_{\rm TEST}$. The simplified equivalent circuit and corresponding waveforms for testing $T_{\rm DV}$ are shown in Fig. 3(a) and (b), respectively.

During the writing period (1), the switch SW2 connects the $V_{\rm dd}$ electrode of pixel circuit to an external power supply and the SW1 is closed to initial the detection circuit. At this time, signal at scan line n is turning $T_{\rm SW}$ on and the data line signal $V_{\rm Data}$ is HIGH to turn $T_{\rm DV}$ on as well. Afterward an amount of charge

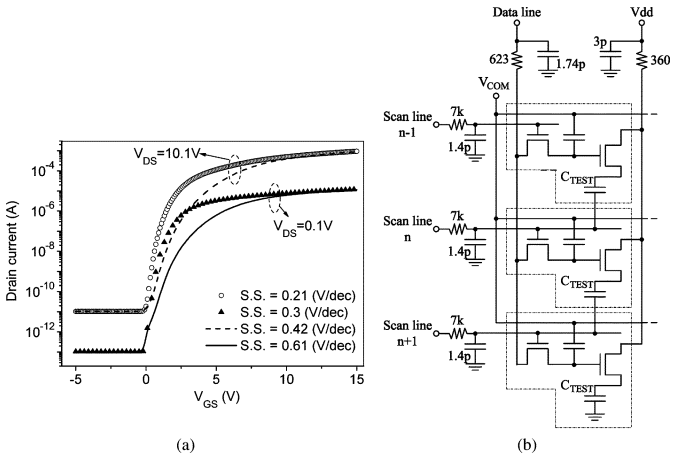

Fig. 4. (a) I_D–V_G characteristics of TFTs and (b) the equivalent schematic diagram used for SPICE simulation.

$Q_{\rm TEST} = V_{dd} \cdot C_{\rm TEST}$ is stored in the $C_{\rm TEST}$ through the $T_{\rm DV}$. When the pixel electrode circuit changes to the holding period (II), $V_{\rm Data}$ becomes LOW to turn off $T_{\rm DV}$ hence the charge $Q_{\rm TEST}$ is retained in the $C_{\rm TEST}$. Meanwhile, the SW2 switches the Vdd electrode of pixel circuit to the detection circuit, nevertheless, the SW1 still keeps output and negative input of amplifier connected together. Because the detection circuit maintains the initial state, the charge in the parasitic capacitance of the Vdd electrode flowing into the detection circuit is removed without disturbing $V_{\rm Out}$.

When the pixel circuit is working in the following reading period (3), the $V_{\rm Data}$ is HIGH to turn on $T_{\rm DV}$ again and the SW1 is open to enable the charge detection circuit simultaneously. The charge in the $C_{\rm TEST}$ is completely collected by detection circuit until the voltage at $C_{\rm TEST}$ becomes 0 V. The output voltage of the integrator is decreased by an offset voltage $\Delta V_{\rm Out}$, as plotted in Fig. 3(b) after the charge is collected in the reading period. $\Delta V_{\rm Out}$, defined as $\Delta V_{\rm Out} = -Q_{\rm TEST}/C_{\rm INT}$, is related to the amount of charge stored in $C_{\rm TEST}$. When $T_{\rm DV}$ of the selected pixel is tested, the signal at next scan line is 0 V as a reference voltage to prevent "floating" of the transparent anode. The output waveform of the integrator can determine whether the TFT array is functioning. If the panel has defects, such like short or discontinuous electrode, the pixel can not be controlled well so that no charge can be stored, thus the detection circuit senses the incorrect data. Furthermore, the entire TFT array is scanned and tested to transform the results from the integrator into a fault map which can be used to locate and classify defects.

III. Simulation Results and Discussion

A. Simulation Environment

The simulation was performed with the Synopsis H-SPICE simulation tool from Rensselaer Polytechnic Institute (RPI) Troy, NY, poly-Si TFT model. The characteristics of $I_{\rm D} - V_G$ of the TFT used for simulation are demonstrated in Fig. 4(a) in which the subthreshold slope (SS) for each curve is listed. In order to imitate the *RC* loading of the practical panel, the parasitic resistance and capacitance of the conducting wires are taken into account, as shown in Fig. 4(b). Other parameters, such as the geometric size of TFT, mobility, threshold voltage, storage and test capacitance, and driving voltage, are also listed in Table I. In the simulation, an ideal operational amplifier with an open loop gain of 10^6 is used to design the charge detection circuit. The resistance $R_{\rm INT}$ and the capacitance $C_{\rm INT}$ of charge detection circuit are designed with a value of 100 kΩ and 10 pF, respectively.

TABLE I
Parameters Used for Simulation

Pixel size (um^2)	66 x 198
W/L of T_{SW}(μm)	7/5
W/L of T_{DV}(μm)	10/5 ~ 50/5
V_{th} of N-TFT (V)	1.0
μ of N-TFT (cm^2/s-V)	77.1
C_{ST} (fF)	100 ~ 1000
C_{TEST} (fF)	10 ~ 90
R_{INT} (Ω), C_{INT} (pF)	100k,10p
R_{para}(Ω), C_{para}(F) of data line	623, 1.74p
R_{para}(Ω), C_{para}(F) of scan line	7000, 1.4p
R_{para}(Ω), C_{para}(F) of Vdd line	360, 3p
V_{Scan} (V)	0, 15
V_{Data} (V)	3 ~ 13
Vdd (V)	0 ~ 15
V_{COM} (V)	15

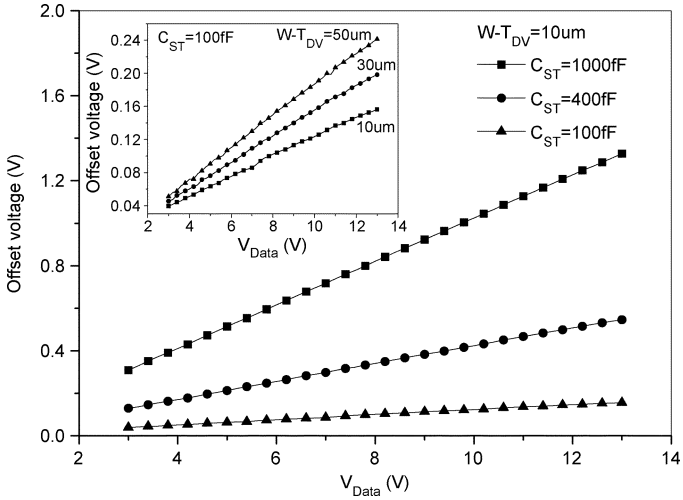

Fig. 5. Offset voltage versus data voltage at different storage capacitance $C_{\rm ST}$ in $T_{\rm SW}$ testing. The inset shows the effect of width of $T_{\rm DV}$ (W-$T_{\rm DV}$) in $T_{\rm SW}$ testing.

B. Results of $T_{\rm SW}$ and $T_{\rm DV}$ Testing

The increases of $V_{\rm Data}$ and $C_{\rm ST}$ result in the corresponding increase of offset voltage when testing the $T_{\rm SW}$, as shown in Fig. 5. As in the previous discussion, the offset is proportional to $Q_{\rm ST}/C_{\rm INT}$, consequently, the more charges can be stored in the $C_{\rm ST}$, the more offset voltage is observed. The geometric size of $T_{\rm DV}$ also affects the offset voltage while testing the $T_{\rm SW}$, as shown in the inset of Fig. 5. The $V_{\rm Data}$ stored in the $C_{\rm ST}$ can induce a channel of $T_{\rm DV}$ and result in an additional parasitic capacitance $C_{\rm DV}$. The stored charges can be written as

$$Q'_{\rm ST} = (C_{\rm ST} + C_{\rm DV}) \cdot V_{\rm Data}. \quad (1)$$

Therefore, the larger the geometric size of $T_{\rm DV}$ is, the more offset voltage can be detected. Since the ground is shorted to the

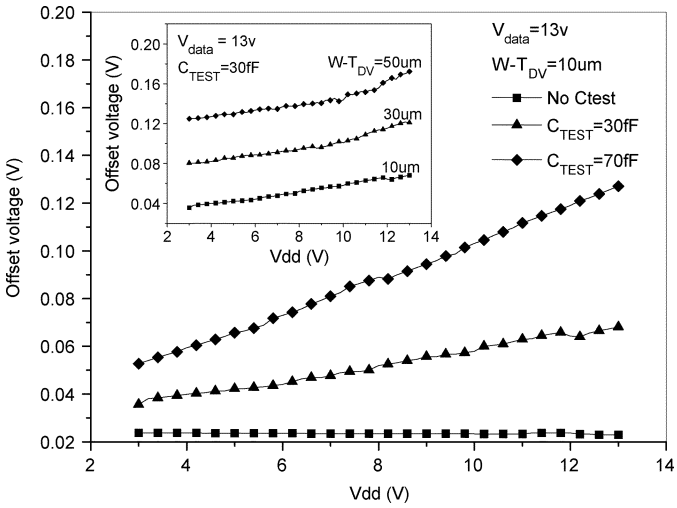

Fig. 6. Offset voltage versus $V_{\rm dd}$ voltage at different $C_{\rm TEST}$ in $T_{\rm DV}$ testing. The inset shows the effect of width of $T_{\rm DV}$ varied from 10 to 50 μm in $T_{\rm DV}$ testing.

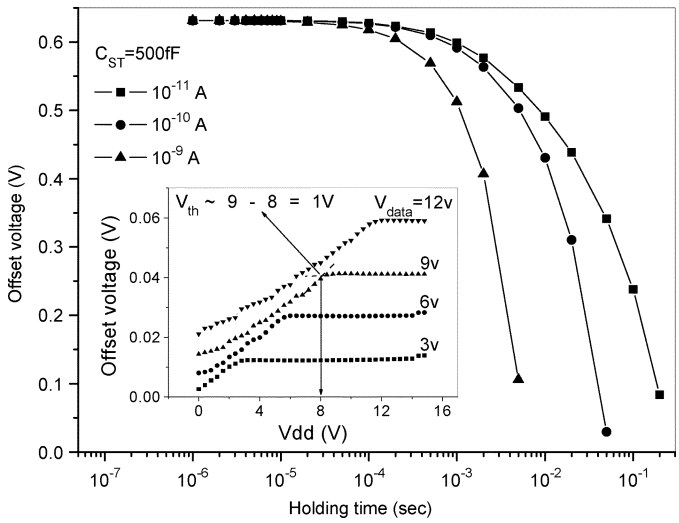

Fig. 7. Offset voltage versus holding time at a leakage current varied from 10^{-11} to 10^{-9} A in $T_{\rm SW}$ testing. The inset demonstrates the transfer curve of TFT for $V_{\rm th}$ evaluation.

$V_{\rm dd}$ electrode, various size of $C_{\rm TEST}$ does not affect the offset voltage in $T_{\rm SW}$ testing.

The function of $T_{\rm DV}$ can also be inspected by writing and reading the charges in the $C_{\rm TEST}$ with proposed testing scheme. The testing charge is written into the $C_{\rm TEST}$ through the $V_{\rm dd}$ electrode, and the ON–OFF state of $T_{\rm DV}$ is controlled directly by a digital data signal with a high level of 13 V and low level of 0 V. The simulation result plotted in Fig. 6 demonstrates that the additional $C_{\rm TEST}$ actually improve the testability of $T_{\rm DV}$. On the other hand, the offset voltage is less than that of the $T_{\rm SW}$ testing because of the small $C_{\rm TEST}$ which must be kept small to minimize the *RC* delay of scan line signal. In contrast, the offset voltage cannot be detected in the pixel without $C_{\rm TEST}$ even though the $T_{\rm DV}$ is functioning perfectly in simulation.

The offset voltage in the $T_{\rm DV}$ testing is also related to the geometric size of $T_{\rm DV}$. The larger size of $T_{\rm DV}$ leads to larger parasitic capacitance $C_{\rm DV}$ which can keep an additional amount of charge within it. At $C_{\rm TEST}$ of 30 fF, increase of the size of $T_{\rm DV}$ results in the shift of the simulated curve, as shown in the inset of Fig. 6, consequently implying that the digital $V_{\rm Data}$ in $T_{\rm DV}$ testing induces the constant $C_{\rm DV}$ as the width of $T_{\rm DV}$ is fixed regardless of the $V_{\rm dd}$ voltage.

C. Threshold Voltage, Leakage Current, and SS

Charge collected by the external detection circuit can be used to evaluate the characteristics such as threshold voltage and leakage current of the pixel circuit. The leakage current induced by process variations causes the charge in $C_{\rm ST}$ to leak out even though the $T_{\rm SW}$ is a turnoff, ultimately affecting the gray level of display. In the above discussion, the write-in data are held in the storage capacitance for a certain period between the writing and reading processes. The write-in data voltage probably decreases during the holding period due to the leakage current of $T_{\rm SW}$. The degree of leakage current of $T_{\rm SW}$ can be monitored by the offset voltage with various holding periods $T_{\rm hold}$, as expressed in (2)

$$\Delta V = \frac{Q'_{\rm ST} - I_{\rm leak} \cdot T_{\rm hold}}{C_{\rm INT}}. \tag{2}$$

The simulation is conditioned by connecting an ideal current source of 10 p to 1 nA between source/drain nodes of the $T_{\rm SW}$ to simulate the leakage current. The simulation result reveals that the longer holding time is performed, the less offset voltage can be detected, as shown in Fig. 7.

In the AM-OLED operation, the $T_{\rm DV}$ is used to convert voltage into current hence the variation of threshold voltage of $T_{\rm DV}$ must be sufficiently small to ensure the uniform brightness. When testing the $T_{\rm DV}$, the transfer characteristic of $T_{\rm DV}$, plotted in the inset of Fig. 7, can be derived by scanning various voltage signals to both the data line and the $V_{\rm dd}$ electrode and measuring the offset voltage in turn. When the $V_{\rm dd}$ voltage is higher than $V_{\rm Data}$, the pixel circuit is driven into OFF state and no more charge can be written into $C_{\rm TEST}$. Therefore the offset voltage is kept contact and the linear region of the simulated offset voltage curve can be distinguished from the flat region. Therefore, the threshold voltage can be simply derived from the intersections of two asymptotes. The threshold voltage obtained by this functional testing scheme is an approximate value due to numerous parasitic resistance and capacitance, yet can be used to monitor the threshold variation in general.

An important parameter SS indicates how effectively the TFT can be turned off when gate to source voltage is decreased below threshold voltage. In the TFT process, the increase of grain boundary trap densities or the random grain size and orientation can result in the increase of subthreshold slope. Usually, the variation of subthreshold slope can be used to monitor the uniformity of characteristics of TFT. In the proposed pixel circuit, a significant effect of subthreshold slope can be found while performing the pixel testing. A decrease of offset voltage of about 5 mV in $T_{\rm DV}$ testing is shown in Fig. 8 when the subthreshold slope varies from 0.21 to 0.61 V/dec. The reason is that a large SS attributed to the increase of grain boundary trap densities results in the weak inversion in the channel region of TFT, thus the lesser charge can be retrieved. However, in $T_{\rm SW}$ testing, the decrease of offset voltage is not evident because the channel charge difference caused by the variation of subthreshold slope is neg-

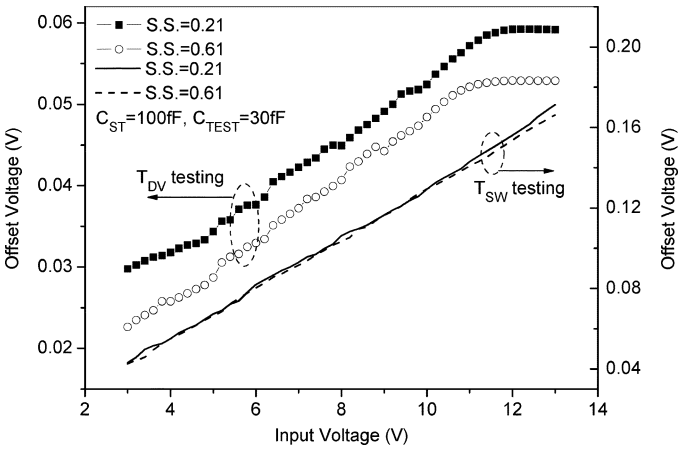

Fig. 8. Offset voltage versus input voltage at different SS from 0.21 to 0.61 V/dec in $T_{\rm DV}$ and $T_{\rm SW}$ testing.

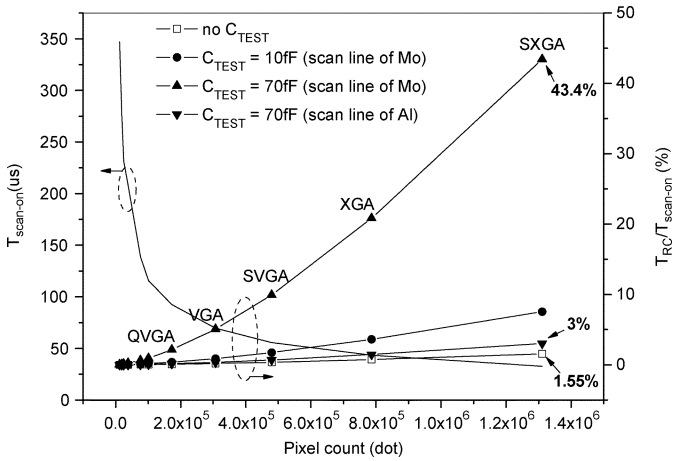

Fig. 9. $T_{\rm scan-on}$ and $T_{\rm RC}/T_{\rm scan-on}$ versus dot resolution of display panel.

ligible compared to the great amount of charge in $C_{\rm ST}$. On the other hand, in $T_{\rm DV}$ testing, the small $C_{\rm TEST}$ is beneficial to observe the effect of subthreshold slope as well as the uniformity of characteristics of $T_{\rm DV}$.

D. Issues of Time Constant and Aperture Ratio

The additional $C_{\rm TEST}$ directly increases the *RC* time constant $T_{\rm RC}$ of the scan line and decreases the aperture ratio of pixel, even though the $C_{\rm TEST}$ can enhance the testability of $T_{\rm DV}$. In this design, the area of contact hole is only 6×6 μm. However, in order to ensure that the contact hole can have perfect contact with the metal underlayer, the metal layer under the contact hole is 14×14 μm. Therefore, an area of about 200 μm^2 is expended for the contact hole area so that the aperture ratio slightly decreases from 43.1% to 41.4%.

In order to evaluate the $T_{\rm RC}$ of the scan line, the parasitic resistance and capacitance of a scan line per pixel ($R_{\rm scan}$, $C_{\rm scan}$) are set to be 13.2 Ω and 2.6 fF, respectively, for the pixel without $C_{\rm TEST}$. In the proposed pixel circuit, the $C_{\rm scan}$ increases from 2.6 to 72.6 fF as $C_{\rm TEST}$ of 10, 30, 50, and 70 fF are used. Besides, the frame rate of 30 Hz is used to calculate the turn-on period of the scan line ($T_{\rm scan-on}$) for the comparison between $T_{\rm RC}$ and $T_{\rm scan-on}$.

$T_{\rm RC}$ is much smaller than $T_{\rm scan-on}$ for the conventional panel without $C_{\rm TEST}$. Even though in high resolution such as $1280 \times {\rm RGB} \times 1024$ (SXGA), $T_{\rm RC}$ is merely 1.55% of $T_{\rm scan-on}$, as shown in Fig. 9. However, $T_{\rm RC}$ is increased when the proposed pixel is implemented into a panel. For example, in the resolution such as $480 \times {\rm RGB} \times 320$ (Half VGA), $C_{\rm TEST}$ of 70 fF for each pixel can increase $T_{\rm RC}$ to 1.98 μs, 28 times larger than that of the conventional panel. However, $T_{\rm RC}$ to $T_{\rm scan-on}$ ratio of 2.15% is still smaller than 5% which is a generally acknowledged limitation in display panel design. In other words, from small to moderate resolution, $C_{\rm TEST}$ can be useful for testability enhancement without seriously impacting on the programming time of the signal. Unfortunately, if the dot resolution is from VGA to SXGA, $T_{\rm RC}$ is dramatically increased by $C_{\rm TEST}$ of 70 fF from 3.53 to 14.13 μs, almost 5.1% to 43.4% of $T_{\rm scan-on}$. The long $T_{\rm RC}$ results in slow switching behavior of $T_{\rm SW}$ as well as inaccurate data write-in. In order to reduce $T_{\rm RC}$, an intuitive approach is to use a small $C_{\rm TEST}$ in the pixel circuit, however, the accuracy of charge detection is limited.

Using high conductivity material such as aluminum to fabricate the scan line instead of molybdenum is another approach to reduce $T_{\rm RC}$. The sheet resistance of aluminum is 70 mΩ/square, merely 7% of that of molybdenum. In contrast with molybdenum, the scan line made by aluminum can achieve the lower $R_{\rm scan}$ of 0.924 Ω in the proposed dimension. $T_{\rm RC}$ to $T_{\rm scan-on}$ ratio as a function of dot resolution with aluminum scan line is also plotted in Fig. 9. Evidentially, the scan line of aluminum dramatically reduces the $T_{\rm RC}$ to $T_{\rm scan-on}$ ratio to 3% even in SXGA resolution. Therefore, $C_{\rm TEST}$ of up to 70 fF can still be utilized to ensure the accuracy of TFT array inspection.

IV. Conclusion

An effective electrical testing scheme and corresponding pixel circuit were designed to enhance the testability of TFT array of AM-OLED. By using an additional $C_{\rm TEST}$, the function of all devices such as TFT and storage capacitance can be examined with electrical signal before the OLED process is performed. The proposed functional testing scheme can be performed without any mechanical motion during testing, and an *in situ* measurement can be taken in real time with high stability. Two side effects: an increase of *RC* time constant can be restrained by fabricating with aluminum; while the reduction of aperture ratio is within acceptable for operation. The simulated and calculated results presented herein including leakage, time constant, and threshold voltage, are useful in identifying the causes of array defects on the panels *in situ*. Furthermore, the array testing can be integrated into the in-line process as a batch job.

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